NXP USA Inc. - KMPC8349EZUAJDB Datasheet

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349ezuajdb

- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- or 64-bit data interface, up to 400 MHz data rate
  - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
  - DRAM chip configurations from 64 Mbits to 1 Gbit with ×8/×16 data ports
  - Full error checking and correction (ECC) support
  - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep-mode support for SDRAM self refresh
  - Auto refresh
  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 820.3x™, 802.3z™, 802.3ac™ standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- Dual PCI interfaces
  - Designed to comply with *PCI Specification Revision 2.3*
  - Data bus width options:
    - Dual 32-bit data PCI interfaces operating at up to 66 MHz
    - Single 64-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities on both interfaces
  - PCI agent mode on PCI1 interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol [1]	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
4. t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

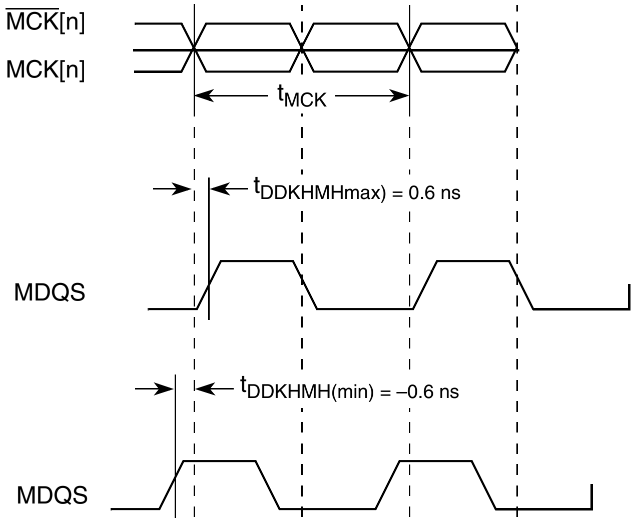


Figure 6. Timing Diagram for t_{DDKHMH}

Table 26. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the GMII receive AC timing diagram.

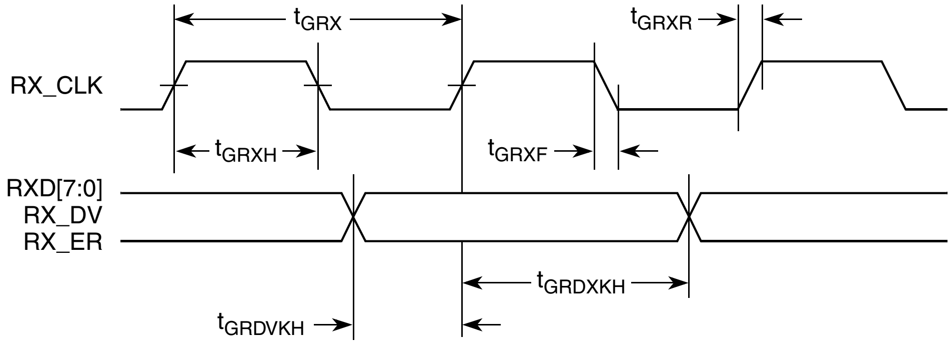


Figure 10. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 27 provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load for TSEC.

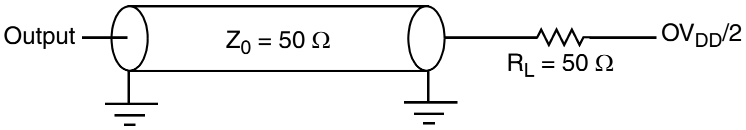


Figure 12. TSEC AC Test Load

Figure 13 shows the MII receive AC timing diagram.

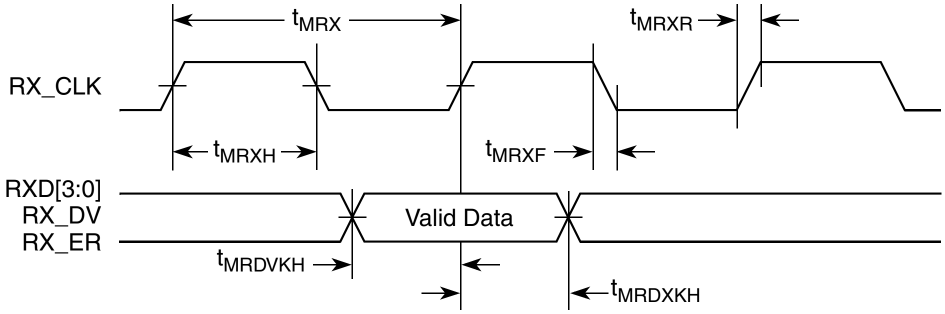


Figure 13. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

Table 31. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver)[2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration[3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T[4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX[3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.
5. Duty cycle reference is $LV_{DD}/2$.

Figure 16 shows the RBMII and RTBI AC timing and multiplexing diagrams.

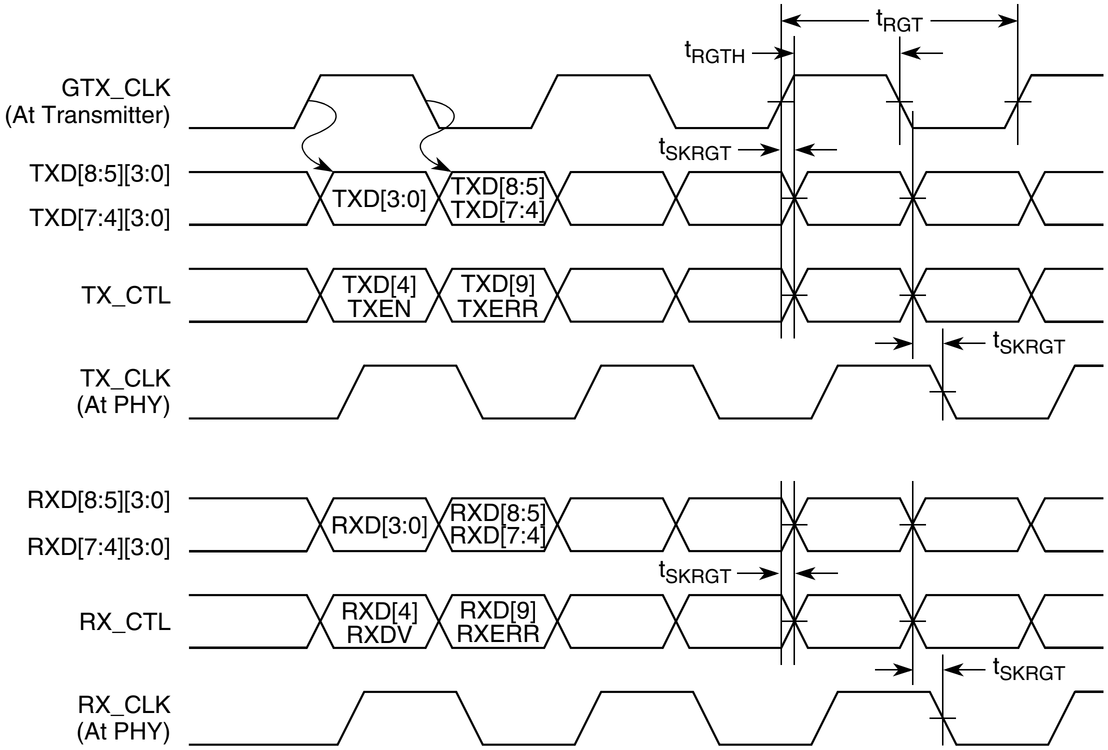


Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, “Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 32 and Table 33.

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.00	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND – 0.3	0.40	V
Input high voltage	V_{IH}	—	LV_{DD} = Min	1.7	—	V
Input low voltage	V_{IL}	—	LV_{DD} = Min	–0.3	0.70	V

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8349EA.

9.1 USB DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the USB interface.

Table 35. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 36 describes the general timing parameters of the USB interface of the MPC8349EA.

Table 36. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2–5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2–5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8349EA.

Table 38. Local Bus General Timing Parameters—DLL On

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	t_{LBKHLR}	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	t_{LBKHOZ}	—	3.8	ns	8

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC_IN.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of LSYNC_IN to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. $t_{LBOTOT1}$ should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6. $t_{LBOTOT2}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7. $t_{LBOTOT3}$ should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 21 through Figure 26 show the local bus signals.

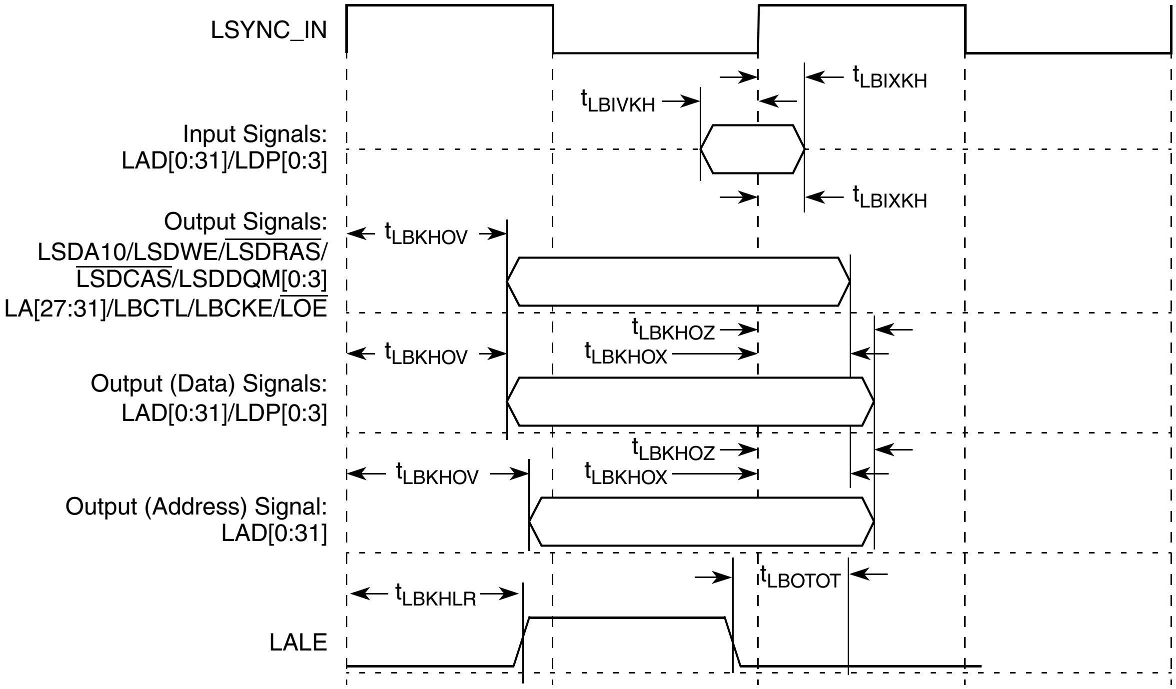


Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

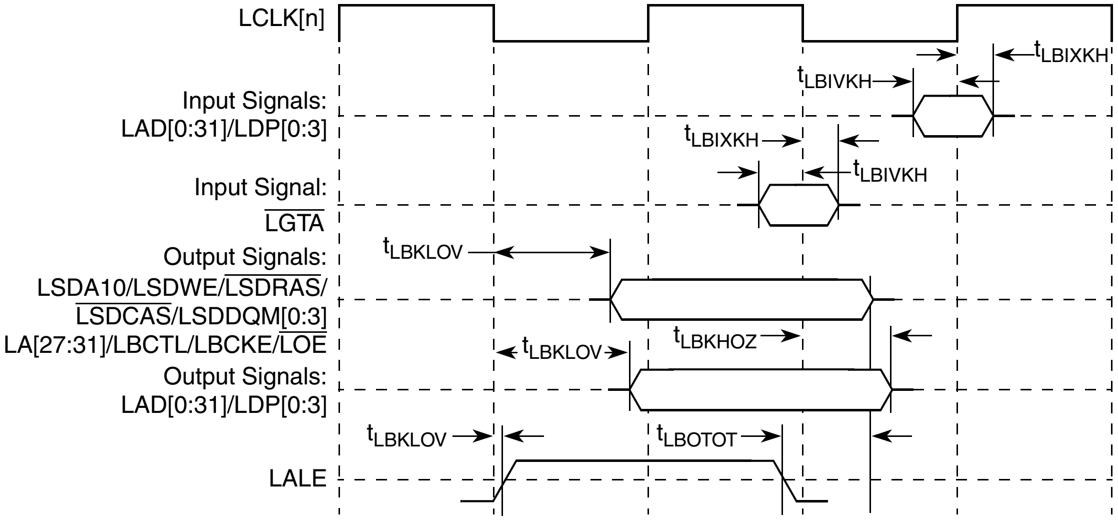


Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

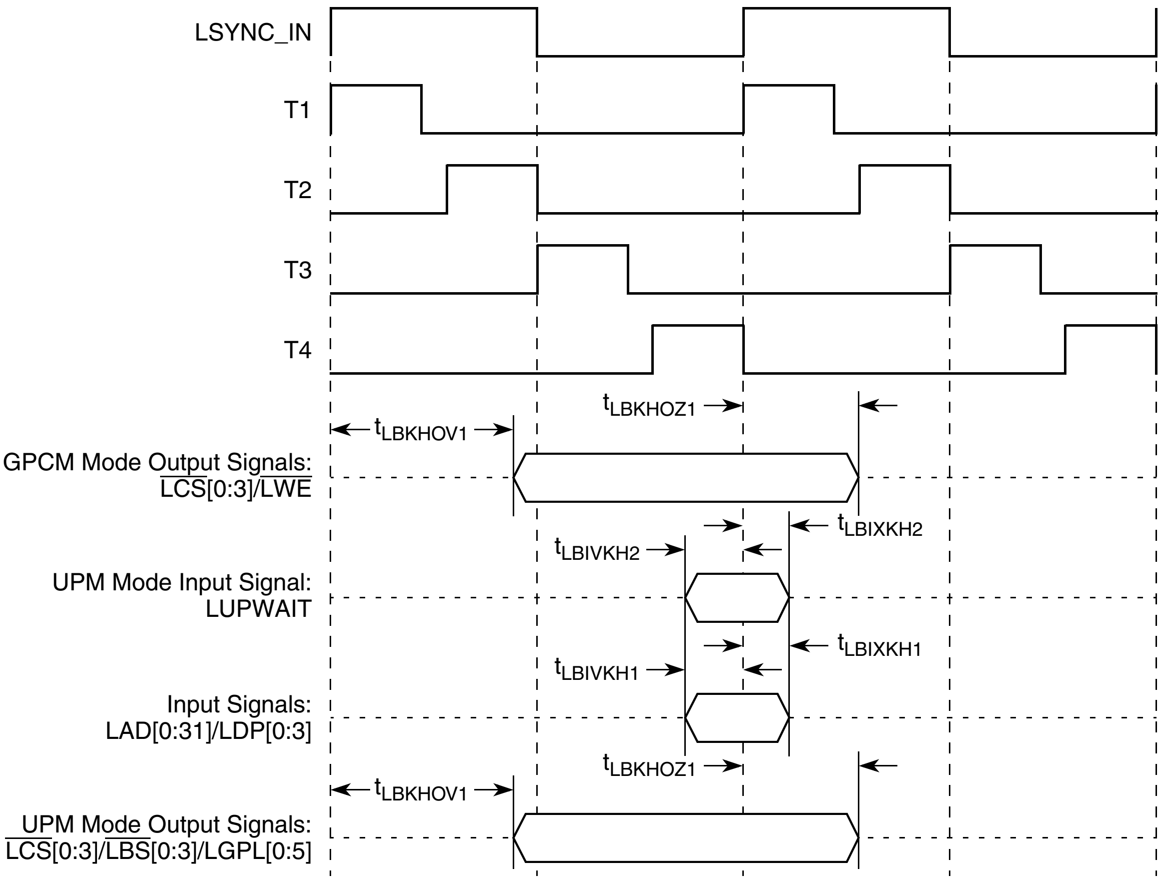


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)

11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA.

11.1 JTAG DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA.

Table 40. JTAG Interface DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	OV_{DD} – 0.3	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V

Table 43. I^{2}C AC Electrical Specifications (continued)

Parameter	Symbol[1]	Min	Max	Unit
Fall time of both SDA and SCL signals[5]	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I^{2}C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I^{2}C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I^{2}C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
5.)The device does not follow the “I2C-BUS Specifications” version 2.1 regarding the t_{I2CF} AC parameter.

Figure 32 provides the AC test load for the I^{2}C.

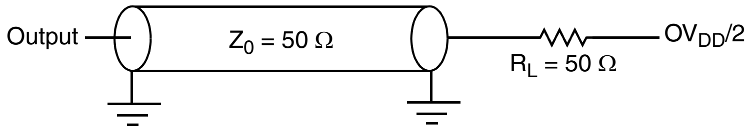


Figure 32. I^{2}C AC Test Load

Figure 33 shows the AC timing diagram for the I^{2}C bus.

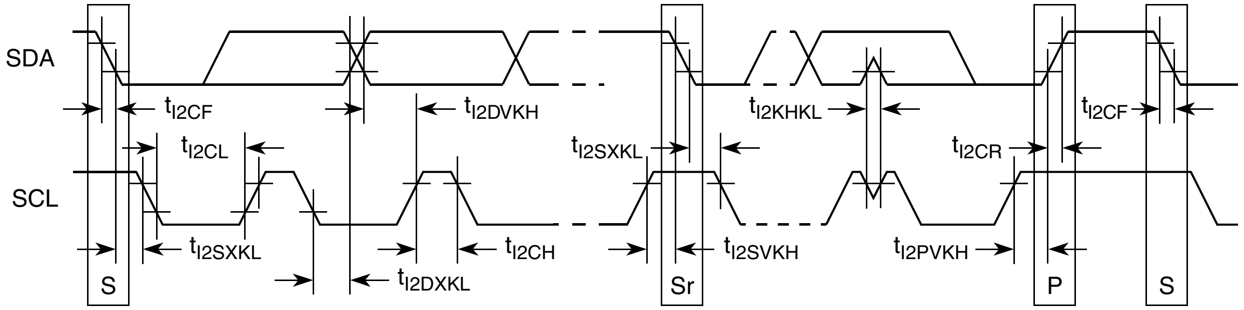


Figure 33. I^{2}C Bus AC Timing Diagram

18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	B20	O	OV_{DD}	3
TMS	A20	I	OV_{DD}	4
$\overline{\text{TRST}}$	B19	I	OV_{DD}	4
Test				
TEST	D22	I	OV_{DD}	6
TEST_SEL	AL13	I	OV_{DD}	6
PMC				
$\overline{\text{QUIESCE}}$	A18	O	OV_{DD}	—
System Control				
$\overline{\text{PORESET}}$	C18	I	OV_{DD}	—
$\overline{\text{HRESET}}$	B18	I/O	OV_{DD}	1
$\overline{\text{SRESET}}$	D18	I/O	OV_{DD}	2
Thermal Management				
THERM0	K32	I	—	8
Power and Ground Signals				
$AV_{DD}1$	L31	Power for e300 PLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}1$	—
$AV_{DD}2$	AP12	Power for system PLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}2$	—
$AV_{DD}3$	AE1	Power for DDR DLL (1.2 V nominal, 1.3 V for 667 MHz)	—	—
$AV_{DD}4$	AJ13	Power for LBIU DLL (1.2 V nominal, 1.3 V for 667 MHz)	$AV_{DD}4$	—

19 Clocking

Figure 41 shows the internal distribution of the clocks.

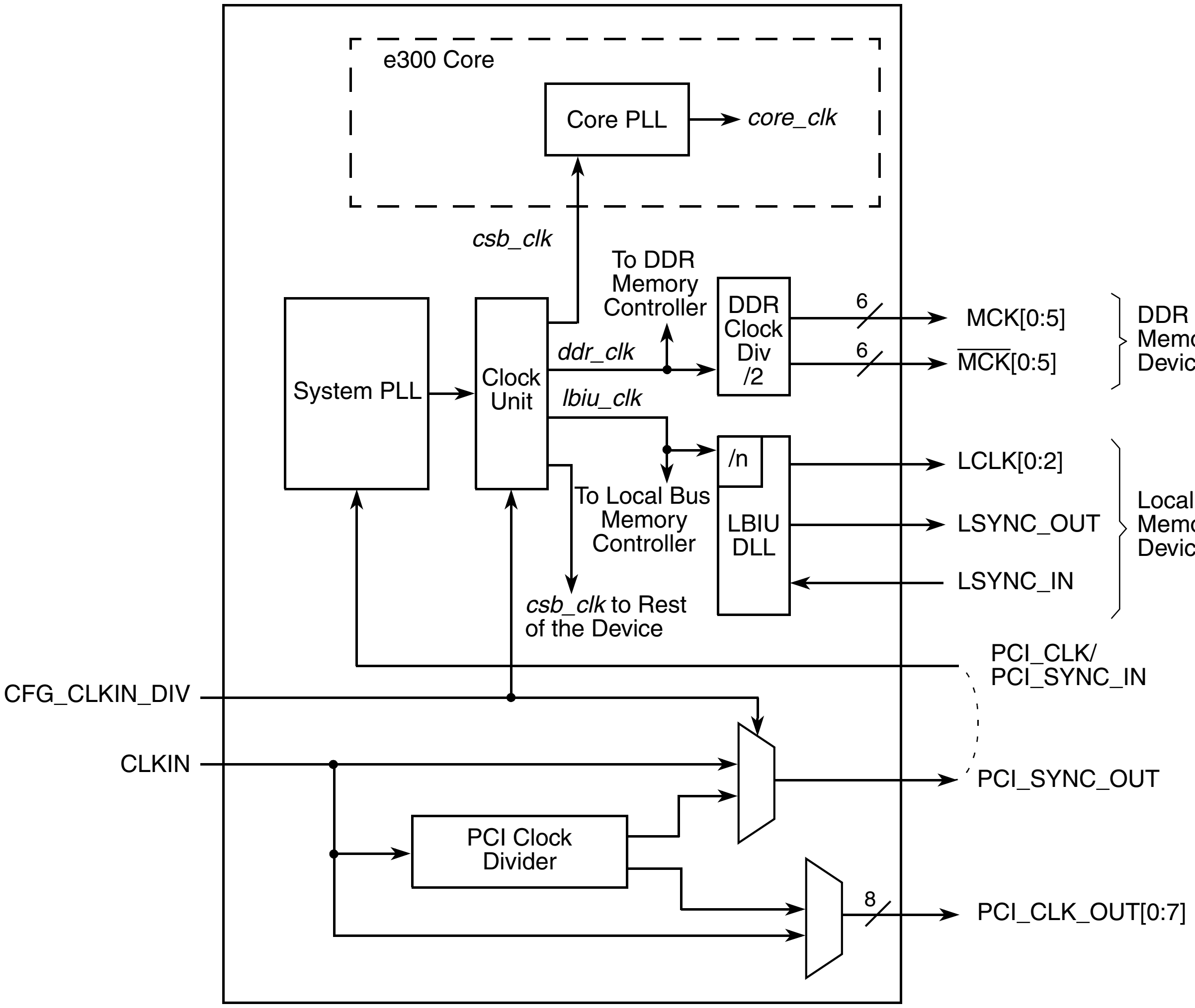


Figure 41. MPC8349EA Clock Subsystem

The primary clock source can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the MPC8349EA is configured as a PCI host device, CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The CFG_CLKIN_DIV configuration input selects whether CLKIN or CLKIN/2 is driven out on the PCI_SYNC_OUT signal. The OCCR[PCICD*n*] parameters select whether CLKIN or CLKIN/2 is driven out on the PCI_CLK_OUT*n* signals.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the MPC8349EA to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock and the CLKIN signal should be tied to GND.

Table 58. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in Section 19, “Clocking,” the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59 and Table 60 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333

Table 62. Suggested PLL Configurations (continued)

Ref No.[1]	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
306	**0011**	**0000110**	—			—			66	200	600
405	**0100**	**0000101**	—			—			66	266	667
504	**0101**	**0000100**	—			—			66	333	667

[1] The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

[2] The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

20 Thermal

This section describes the thermal specifications of the MPC8349EA.

20.1 Thermal Characteristics

Table 63 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8349EA.

Table 63. Package Thermal Characteristics for TBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.7	°C/W	5

Table 63. Package Thermal Characteristics for TBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	ψ_{JT}	1	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

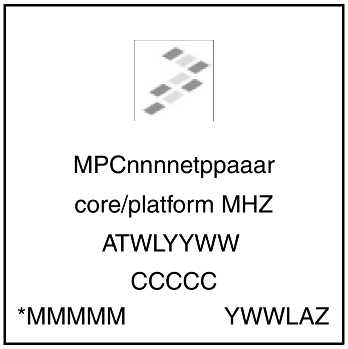
The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

22.2 Part Marking

Parts are marked as in the example shown in Figure 44.



TBGA

Notes:
ATWLYYWW is the traceability code.
CCCCC is the country code.
MMMMM is the mask number.
YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA Devices

23 Document Revision History

This table provides a revision history of this document.

Table 68. Document Revision History

Rev. Number	Date	Substantive Change(s)
13	09/2011	• In Section 2.2, “Power Sequencing,” added Section 2.2.1, “Power-Up Sequencing” and Figure 4. • In Table 25, Table 29 and Table 31, removed the GTX_CLK125. • In Table 34, updated t_{MDKHDX} Max value from 170ns to 70ns.
12	11/2010	• In Table 55 added note for pin LGPL4. • In Section 21.7, “Pull-Up Resistor Requirements, updated the list of open drain type pins.
11	05/2010	• In Table 25 through Table 30, changed V_{IL}(min) to V_{IH}(max) to (20%–80%). • Added Table 8, “EC_GTX_CLK125 AC Timing Specifications.”
10	5/2009	• In Table 57, updated frequency for max csb_clk to 333 MHz and DDR2, from 100-200 to 100-133 at core frequency = 533MHz. • In Section 18.1, “Package Parameters for the MPC8349EA TBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. • In Table 66, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.

Table 68. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
9	2/2009	• Added footnote 6 to Table 7. • In Section 9.2, “USB AC Electrical Specifications,” clarified that AC table is for ULPI only. • In Table 39, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 22, Figure 24, and Figure 25 for output signals. • Added footnote 11 to Table 55. • Added footnote 4 to Table 66. • In Section 21.1, “System Clocking,” removed “(AVDD1)” and “(AVDD2”) from bulleted list. • In Section 21.2, “PLL Power Supply Filtering,” in the second paragraph, changed “provide five independent filter circuits,” and “the five AVDD pins” to provide four independent filter circuits,” and “the four AVDD pins.” • In Table 57, corrected the max csb_clk to 266 MHz. • In Table 62, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz • In Table 66, updated note 1 to say the following: “For temperature range = C, processor frequency is limited to 533 with a platform frequency of 266.”
8	4/2007	• In Table 3, “Output Drive Capability,” changed the values in the Output Impedance column and added USB to the seventh row. • In Section 21.7, “Pull-Up Resistor Requirements,“deleted last two paragraphs and after first paragraph, added a new paragraph. • Deleted Section 21.8, “JTAG Configuration Signals,” and Figure 43, “JTAG Interface Connection.”
7	3/2007	• In Table 57, “Operating Frequencies for TBGA,” in the ‘Coherent system bus frequency (*csb_clk*)’ row, changed the value in the 533 MHz column to 100-333. • In Table 63, “Suggested PLL Configurations,” under the subhead, ‘33 MHz CLKIN/PCI_CLK Options,’ added row A03 between Ref. No. 724 and 804. Under the subhead ‘66 MHz CLKIN/PCI_CLK Options,’ added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. • In Section 23, “Ordering Information,” replaced first paragraph and added a note. • In Section 23.1, “Part Numbers Fully Addressed by this Document,” replaced first paragraph.
6	2/2007	• Page 1, updated first paragraph to reflect PowerQUICC II Pro information. • In Table 18, “DDR and DDR2 SDRAM Input AC Timing Specifications,” added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. • In Figure 41, “JTAG Interface Connection,” updated with new figure. • In Section 23.1, “Part Numbers Fully Addressed by This Document,” replaced third sentence of first paragraph directing customer to product summary page for available frequency configuration parts.
5	1/2007	• In Table 1, “Absolute Maximum Ratings,” added (1.36 max for 667-MHz core frequency) to max V_{DD} and Av_{DD} values. • In Table 2, “Recommended Operating Conditions,” added a row showing nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts. • In Table 4, “MPC8349EA Power Dissipation,” added two footnotes to 667-MHz row showing nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts. • In Table 54, “MPC83479EA (TBGA) Pinout Listing,” updated V_{DD} nd AV_{DD} rows to show nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts.
4	12/2006	Table 19, “DDR and DDR2 SDRAM Output AC Timing Specifications,” modified T_{ddkhds} for 333 MHz from 900 ps to 775 ps.

Table 68. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
3	11/2006	• Updated note in introduction. • In the features list in Section 1, “Overview,” updated DDR data rate to show 400 MHz for DDR2 for TBGA parts for silicon 3.x and 400 MHz for DDR2 for TBGA parts for silicon 3.x. • In Section 23, “Ordering Information,” replicated note from document introduction.
2	8/2006	• Changed all references to revision 2.0 silicon to revision 3.0 silicon. • Changed VIH minimum value in Table 40, “JTAG Interface DC Electrical Characteristics,” to OV_{DD} – 0.3. • In Table 44, “PCI DC Electrical Characteristics,” changed high-level input voltage values to min = 2 and max = OV_{DD} + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8. • Updated DDR2 I/O power values in Table 5, “MPC8347EA Typical I/O Power Dissipation.” • In Table 66, “Suggested PLL Configurations,” deleted reference-number rows 902 and 703.
1	4/2006	• Removed Table 20, “Timing Parameters for DDR2-400.” • Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, “DDR and DDR2 SDRAM Output AC Timing Specifications,” rows 2 and 3, and in Figure 2, “DDR SDRAM Output Timing Diagram. • Changed Min and Max values for V_{IH} and VIL in Table 40Table 44,“PCI DC Electrical Characteristics.” • In Table 55, “MPC8349EA (TBGA) Pinout Listing,” and Table 52, “MPC8347EA (PBGA) Pinout Listing,” modified rows for MDICO and MDIC1 signals and added note ‘It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor.’ • Table 55, “MPC8349EA (TBGA) Pinout Listing,” in row AVDD3 changed power supply from “AVDD3” to ‘—.’
0	3/2006	Initial public release