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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349ezuajf

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

- Double data rate, DDR1/DDR2 SDRAM memory controller
 - Programmable timing supporting DDR1 and DDR2 SDRAM
 - 32- or 64-bit data interface, up to 400 MHz data rate
 - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
 - DRAM chip configurations from 64 Mbits to 1 Gbit with $\times 8/\times 16$ data ports
 - Full error checking and correction (ECC) support
 - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
 - Contiguous or discontiguous memory mapping
 - Read-modify-write support
 - Sleep-mode support for SDRAM self refresh
 - Auto refresh
 - On-the-fly power management using CKE
 - Registered DIMM support
 - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3TM, 802.3uTM, 820.3xTM, 802.3zTM, 802.3acTM standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- Dual PCI interfaces
 - Designed to comply with PCI Specification Revision 2.3
 - Data bus width options:
 - Dual 32-bit data PCI interfaces operating at up to 66 MHz
 - Single 64-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities on both interfaces
 - PCI agent mode on PCI1 interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV _{REF}	I _{MVREF}		500	μA	1

Note:

1. The voltage regulator for MV_{REF} must supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	_	MV _{REF} – 0.25	V	_
AC input high voltage	V _{IH}	MV _{REF} + 0.25	—	V	_

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V	—

Figure 7 shows the DDR SDRAM output timing diagram.



Figure 8 provides the AC test load for the DDR bus.



Figure 8. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8349EA.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface of the MPC8349EA.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current (0.8 V \leq V _{IN} \leq 2 V)	I _{IN}	_	±5	μA

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	_	4.0	ns
RX_CLK clock fall time (80%-20%)	t _{MRXF}	1.0	_	4.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

Figure 12 provides the AC test load for TSEC.



Figure 12. TSEC AC Test Load

Figure 13 shows the MII receive AC timing diagram.



Figure 13. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
GTX_CLK clock period	t _{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t _{TTXH} /t _{TTX}	40	_	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t _{TTKHDX}	1.0	_	5.0	ns
GTX_CLK clock rise (20%–80%)	t _{TTXR}	—	_	1.0	ns
GTX_CLK clock fall time (80%–20%)	t _{TTXF}	—		1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 14 shows the TBI transmit AC timing diagram.



Figure 14. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
PMA_RX_CLK clock period	t _{TRX}		16.0		ns
PMA_RX_CLK skew	t _{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t _{TRXH} /t _{TRX}	40	_	60	%

Table 30. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t _{TRDVKH} 2	2.5	—	_	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t _{тRDXKH} ²	1.5	—	_	ns
RX_CLK clock rise time (20%–80%)	t _{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time (80%-20%)	t _{TRXF}	0.7	_	2.4	ns

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
</sub>

2. Setup and hold time of even numbered RCG are measured from the riding edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the riding edge of PMA_RX_CLK0.

Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram

8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

Table 31. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
Data to clock output skew (at transmitter)	t _{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t _{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t _{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t _{RGTH} /t _{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t _{RGTH} /t _{RGT}	40	50	60	%
Rise time (20%–80%)	t _{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t _{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).

2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.

3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns \pm 40 ns and 40 ns \pm 4 ns, respectively.

4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.

5. Duty cycle reference is $LV_{DD}/2$.

Ethernet: Three-Speed Ethernet, MII Management

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V	(continued)
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Parameter	Symbol	Conditions	Min	Мах	Unit
Input high current	I _{IH}	$V_{IN}^{1} = LV_{DD}$	-	10	μA
Input low current	IIL	$V_{IN} = LV_{DD}$	-15	_	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Parameter	Symbol	Conditions		Min	Мах	Unit		
Supply voltage (3.3 V)	LV _{DD}	—		_		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	$LV_{DD} = Min$	2.10	LV _{DD} + 0.3	V		
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND	0.50	V		
Input high voltage	V _{IH}	—		2.00	—	V		
Input low voltage	V _{IL}	—		—		-	0.80	V
Input high current	I _{IH}	LV _{DD} = Max	$V_{IN}^{1} = 2.1 V$	_	40	μA		
Input low current	۱ _{IL}	LV _{DD} = Max	V _{IN} = 0.5 V	-600	—	μA		

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 34 provides the MII management AC timing specifications.

Table 34. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	_	2.5		MHz	2
MDC period	t _{MDC}		400		ns	_
MDC clock pulse width high	t _{MDCH}	32	—	_	ns	—
MDC to MDIO delay	t _{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t _{MDDVKH}	5	—	_	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0	—	_	ns	—
MDC rise time	t _{MDCR}	_		10	ns	

Local Bus

Figure 21 through Figure 26 show the local bus signals.



Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)



Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)





Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)



Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8349EA.

13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8349EA.

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	$V_{OUT} \le V_{OL}$ (max)	-0.3	0.8	V
Input current	I _{IN}	$V_{IN}^{1} = 0 V \text{ or } V_{IN} = OV_{DD}$	_	±5	μA
High-level output voltage	V _{OH}	OV _{DD} = min, I _{OH} = -100 μA	OV _{DD} – 0.2	_	V
Low-level output voltage	V _{OL}	OV _{DD} = min, I _{OL} = 100 μA	_	0.2	V

Table 44. PCI DC Electrical Characteristics

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8349EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing	Specifications at 66 MHz ¹
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Parameter	Symbol ²	Min	Мах	Unit	Notes
Clock to output valid	^t PCKHOV	—	6.0	ns	3
Output hold from clock	t _{PCKHOX}	1		ns	3
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t _{PCIVKH}	3.0	_	ns	3, 5
Input hold from clock	t _{PCIXKH}	0	_	ns	3, 5
REQ64 to PORESET setup time	t _{PCRVRH}	5	—	clocks	6

Table 45. PCI AC Timing Specifications at 66 MHz ¹	(continued)
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Parameter	Symbol ²	Min	Max	Unit	Notes
PORESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	6

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.}
- 3. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.
- 6. The setup and hold time is with respect to the rising edge of PORESET.

Table 46 provides the PCI AC timing specifications at 33 MHz.

Table 46. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	^t PCKHOV	—	11	ns	2
Output hold from clock	t _{PCKHOX}	2		ns	2
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	-	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	_	ns	2, 4
REQ64 to PORESET setup time	t _{PCRVRH}	5	_	clocks	5
PORESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	5

Notes:

2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.

3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4. Input timings are measured at the pin.

5. The setup and hold time is with respect to the rising edge of PORESET.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

Figure 37 provides the AC test load for the SPI.



Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 38 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.



Figure 39 shows the SPI timings in master mode (internal clock).



Figure 39. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8349EA is available in a tape ball grid array (TBGA). See Section 18.1, "Package Parameters for the MPC8349EA TBGA" and Section 18.2, "Mechanical Dimensions for the MPC8349EA TBGA.

18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is $35 \text{ mm} \times 35 \text{ mm}$, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

Package and Pin Listings

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV _{DD}	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	0	OV _{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	0	OV _{DD}	—
MPH1_CLK/DR_CLK	B29	I	OV _{DD}	—
	USB Port 0			
MPH0_D0_ENABLEN/ DR_D8_CHGVBUS	C29	I/O	OV _{DD}	—
MPH0_D1_SER_TXD/ DR_D9_DCHGVBUS	A30	I/O	OV _{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	E28	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	B30	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	C30	I/O	OV _{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	A31	I/O	OV _{DD}	—
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV _{DD}	—
MPH0_D7_DRVVBUS/ DR_D15_IDPULLUP	C31	I/O	OV _{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	B32		OV _{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	A32	I/O	OV _{DD}	—
MPH0_STP_SUSPEND/ DR_TX_READY	A33	I/O	OV _{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	C32	I	OV _{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	D31	I/O	OV _{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	E30	I/O	OV _{DD}	_
MPH0_CLK/DR_RX_VALID	B33	I	OV _{DD}	—
	Programmable Interrupt Controller			
MCP_OUT	AN33	0	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	C19	I/O	OV _{DD}	—
IRQ[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV _{DD}	—
IRQ[6]/GPIO2[18]/CKSTOP_OUT	A21	I/O	OV _{DD}	—
IRQ[7]/GPIO2[19]/CKSTOP_IN	C20	I/O	OV _{DD}	
	Ethernet Management Interface			
EC_MDC	A7	0	LV _{DD1}	
EC_MDIO	E9	I/O	LV _{DD1}	11

As shown in Figure 41, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (csb_clk), the internal clock for the DDR controller (ddr_clk), and the internal clock for the local bus interface unit ($lbiu_clk$).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

 $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

 $ddr_clk = csb_clk \times (1 + RCWL[DDRCM])$

 ddr_clk is not the external memory bus frequency; ddr_clk passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as ddr_clk .

The internal *lbiu_clk* frequency is determined by the following equation:

 $lbiu_clk = csb_clk \times (1 + RCWL[LBIUCM])$

lbiu_clk is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 56 specifies which units have a configurable clock frequency.

Unit	Default Frequency	Options
TSEC1	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
TSEC2, I ² C1	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
Security core	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
USB DR, USB MPH	csb_clk/3	Off, csb_clk, csb_clk/2, <i>csb_clk/3</i>
PCI1, PCI2 and DMA complex	csb_clk	Off, csb_clk

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
Low	0110	6:1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		1
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2:1				133
High	0011	3:1			100	200
High	0100	4 : 1			133	266
High	0101	5:1			166	333
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				

Table 59. CSB Frequency Options for Host Mode (continued)

¹ CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 60. CSB Frequency Options for Agent Mode

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333

			In) ²		
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

Table 60. CSB Frequency Options for Agent Mode (continued)

¹ CFG_CLKIN_DIV doubles csb_clk if set high.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 61 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 61 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

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20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

 T_J = junction temperature (°C) T_C = case temperature of the package (°C) $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W) P_D = power dissipation (W)

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8349EA.

21.1 System Clocking

The MPC8349EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in Section 19.1, "System PLL Configuration."

have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8349EA.

21.5 Output Buffer DC Impedance

The MPC8349EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 43). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.



Figure 43. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is