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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | PowerPC e300 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 400MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | USB 2.0 + PHY (2) |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 105°C (TA) |
| Security Features | - |
| Package / Case | 672-LBGA |
| Supplier Device Package | 672-LBGA (35x35) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349vvagdb |

**NOTE**

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications.*

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

# 1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8349EA.

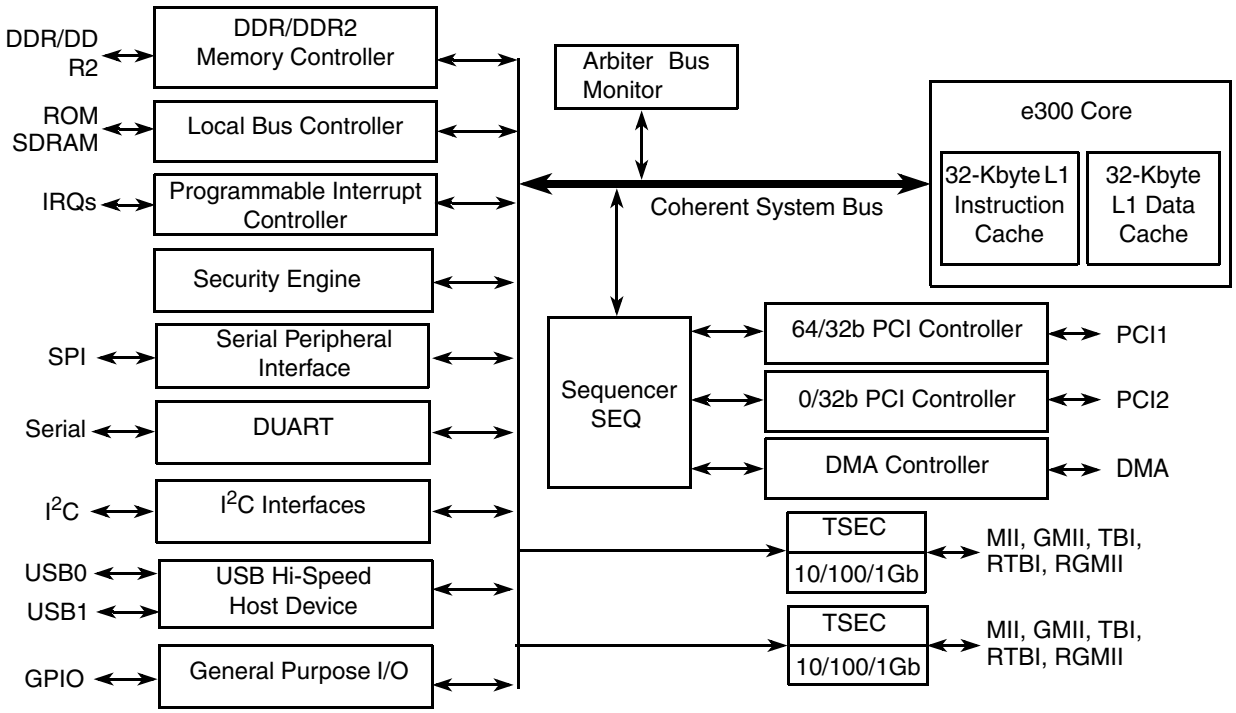



**Figure 1. MPC8349EA Block Diagram**

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology

### 2.1.2 Power Supply Voltage Specification

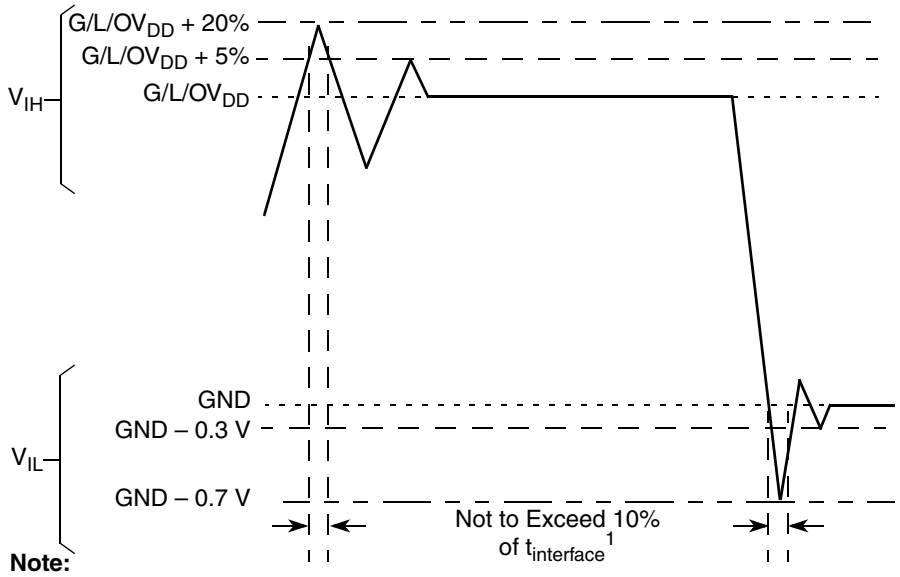
Table 2 provides the recommended operating conditions for the MPC8349EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

**Table 2. Recommended Operating Conditions**

| Parameter | Symbol | Recommended Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage for 667-MHz core frequency | $V_{DD}$ | 1.3 V ± 60 mV | V | 1 |
| Core supply voltage | $V_{DD}$ | 1.2 V ± 60 mV | V | 1 |
| PLL supply voltage for 667-MHz core frequency | $AV_{DD}$ | 1.3 V ± 60 mV | V | 1 |
| PLL supply voltage | $AV_{DD}$ | 1.2 V ± 60 mV | V | 1 |
| DDR and DDR2 DRAM I/O voltage | $GV_{DD}$ | 2.5 V ± 125 mV<br>1.8 V ± 90 mV | V | — |
| Three-speed Ethernet I/O supply voltage | $LV_{DD1}$ | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | V | — |
| Three-speed Ethernet I/O supply voltage | $LV_{DD2}$ | 3.3 V ± 330 mV<br>2.5 V ± 125 mV | V | — |
| PCI, local bus, DUART, system control and power management, $I^2C$, and JTAG I/O voltage | $OV_{DD}$ | 3.3 V ± 330 mV | V | — |

**Note:**
1 $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, $AV_{DD}$, and $V_{DD}$ must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8349EA.




**Note:**
1. $t_{interface}$ refers to the clock period associated with the bus clock interface.

**Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}$**

### 8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

**Table 23. GMII/TBI and MII DC Electrical Characteristics**

| Parameter | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 3.3 V | $LV_{DD}$[2] | — | | 2.97 | 3.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –4.0 mA | $LV_{DD}$ = Min | 2.40 | $LV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 4.0 mA | $LV_{DD}$ = Min | GND | 0.50 | V |
| Input high voltage | $V_{IH}$ | — | — | 2.0 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | — | –0.3 | 0.90 | V |
| Input high current | $I_{IH}$ | $V_{IN}$[1] = $LV_{DD}$ | | — | 40 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$[1] = GND | | –600 | — | μA |

**Notes:**
1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.
2. GMII/MII pins not needed for RGMII or RTBI operation are powered by the $OV_{DD}$ supply.

**Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics**

| Parameters | Symbol | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage 2.5 V | $LV_{DD}$ | — | | 2.37 | 2.63 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –1.0 mA | $LV_{DD}$ = Min | 2.00 | $LV_{DD}$ + 0.3 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.0 mA | $LV_{DD}$ = Min | GND – 0.3 | 0.40 | V |
| Input high voltage | $V_{IH}$ | — | $LV_{DD}$ = Min | 1.7 | $LV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | $LV_{DD}$ = Min | –0.3 | 0.70 | V |
| Input high current | $I_{IH}$ | $V_{IN}$[1] = $LV_{DD}$ | | — | 10 | μA |
| Input low current | $I_{IL}$ | $V_{IN}$[1] = GND | | –15 | — | μA |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $LV_{IN}$ symbol referenced in Table 1 and Table 2.

## 8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

### 8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

**Table 34. MII Management AC Timing Specifications (continued)**

At recommended operating conditions with $LV_{DD}$ is 3.3 V ± 10% or 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| MDC fall time | $t_{MDHF}$ | — | — | 10 | ns | — |

**Notes:**

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MDKHDX}$ symbolizes management data timing (MD) for the time $t_{MDC}$ from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, $t_{MDDVKH}$ symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MDC}$ clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
3. This parameter is dependent on the csb_clk speed (that is, for a csb_clk of 267 MHz, the delay is 70 ns and for a csb_clk of 333 MHz, the delay is 58 ns).

Figure 17 shows the MII management AC timing diagram.

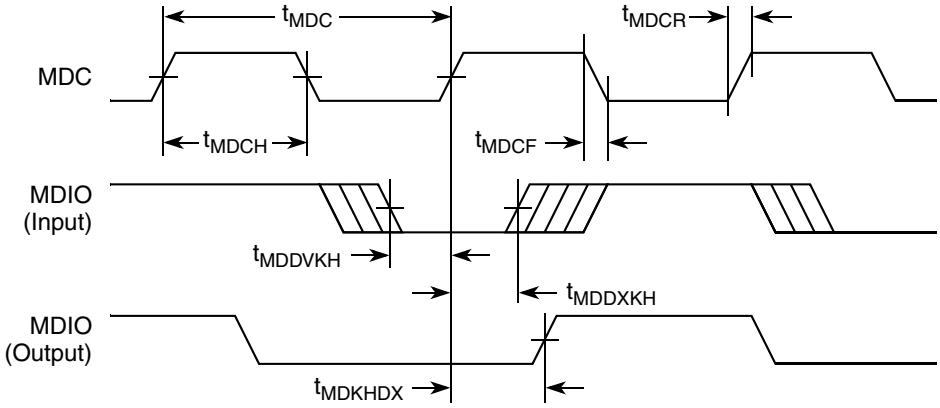



**Figure 17. MII Management Interface Timing Diagram**

Figure 21 through Figure 26 show the local bus signals.

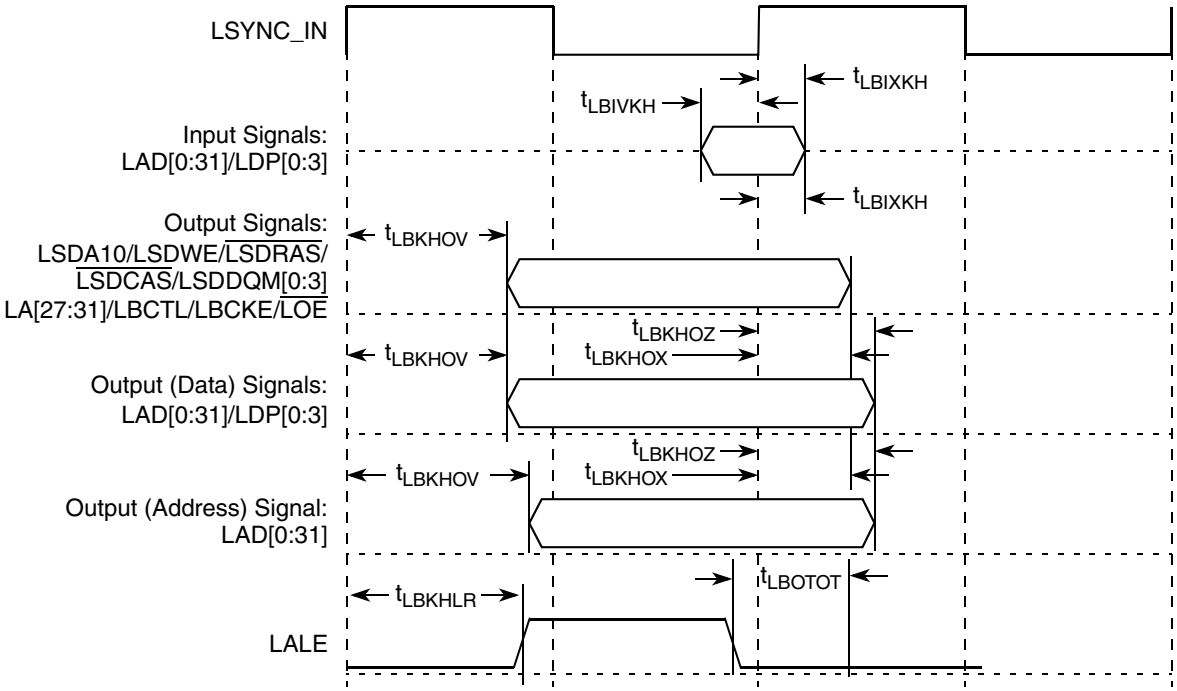



**Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)**

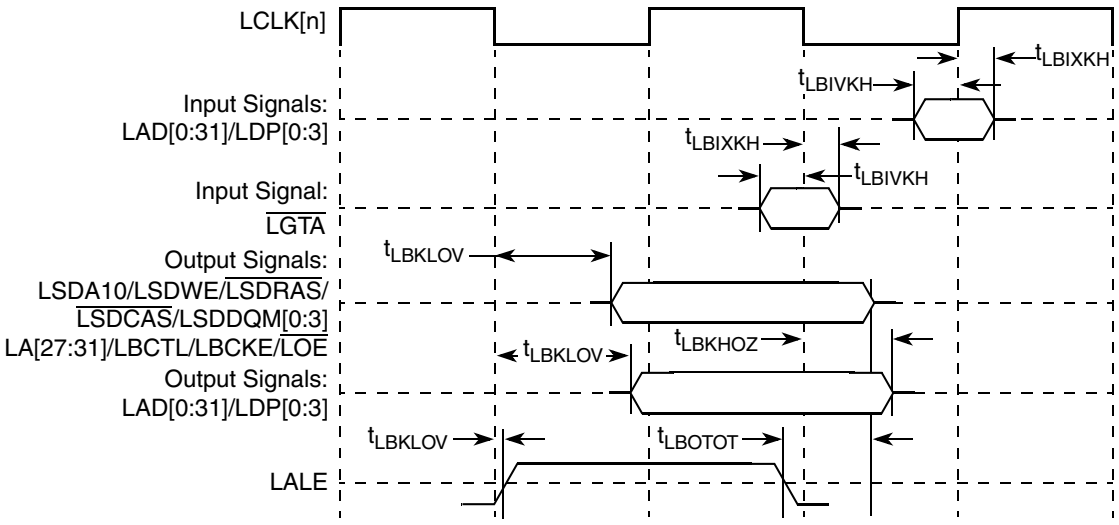



**Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)**

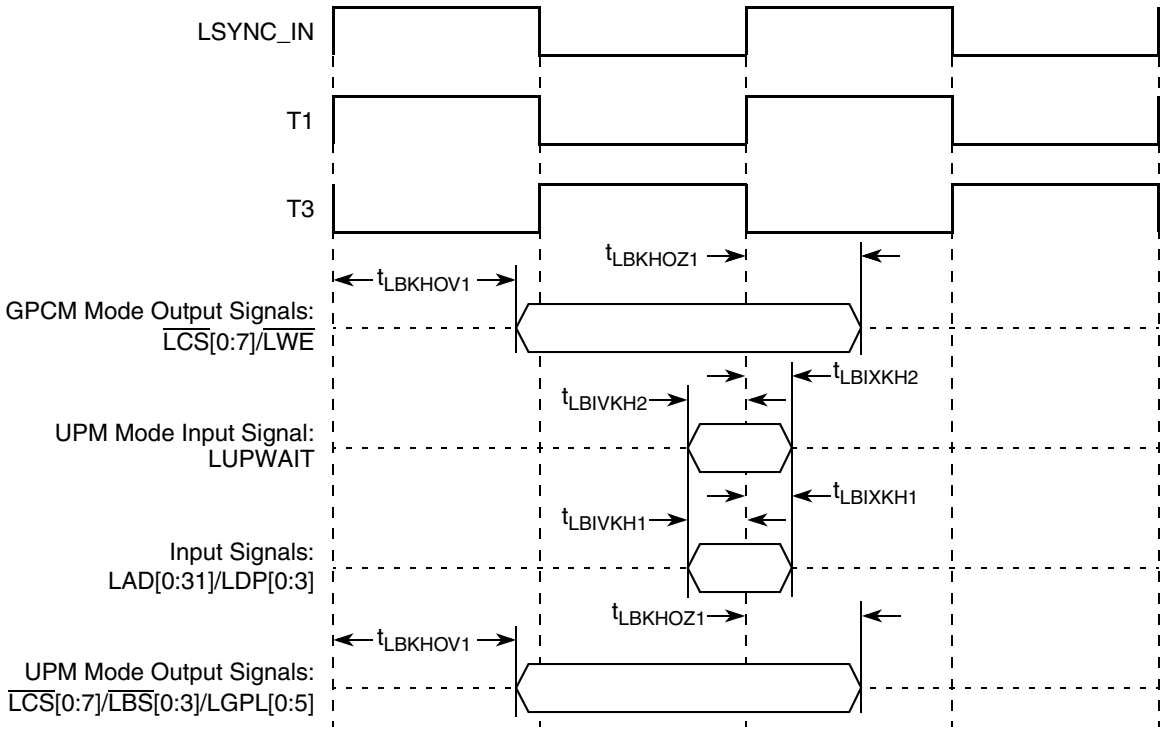



**Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)**

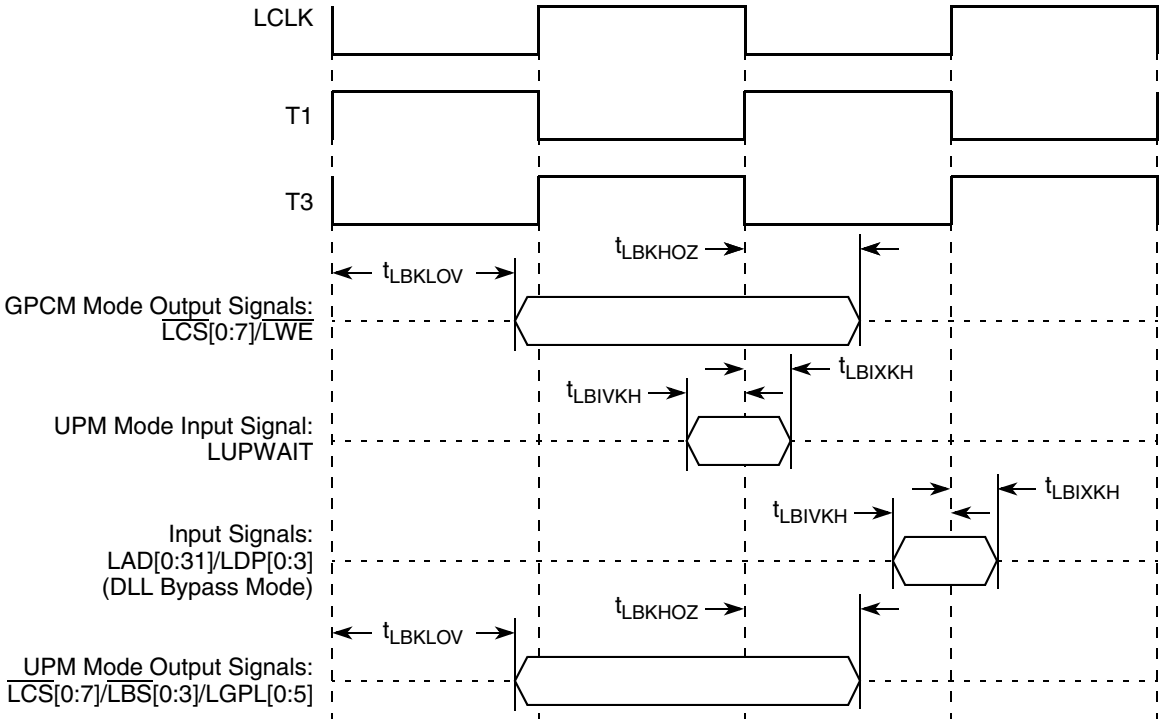



**Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)**

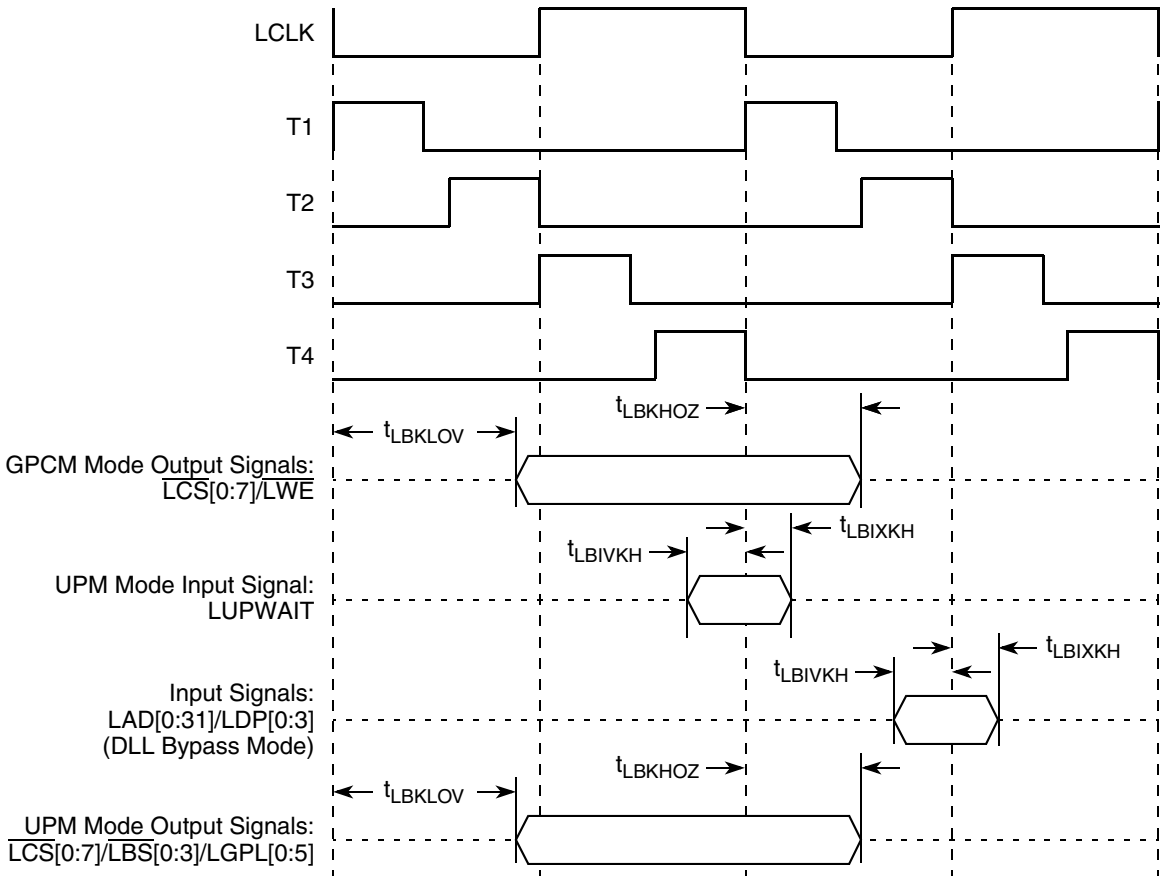



**Figure 25. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Bypass Mode)**

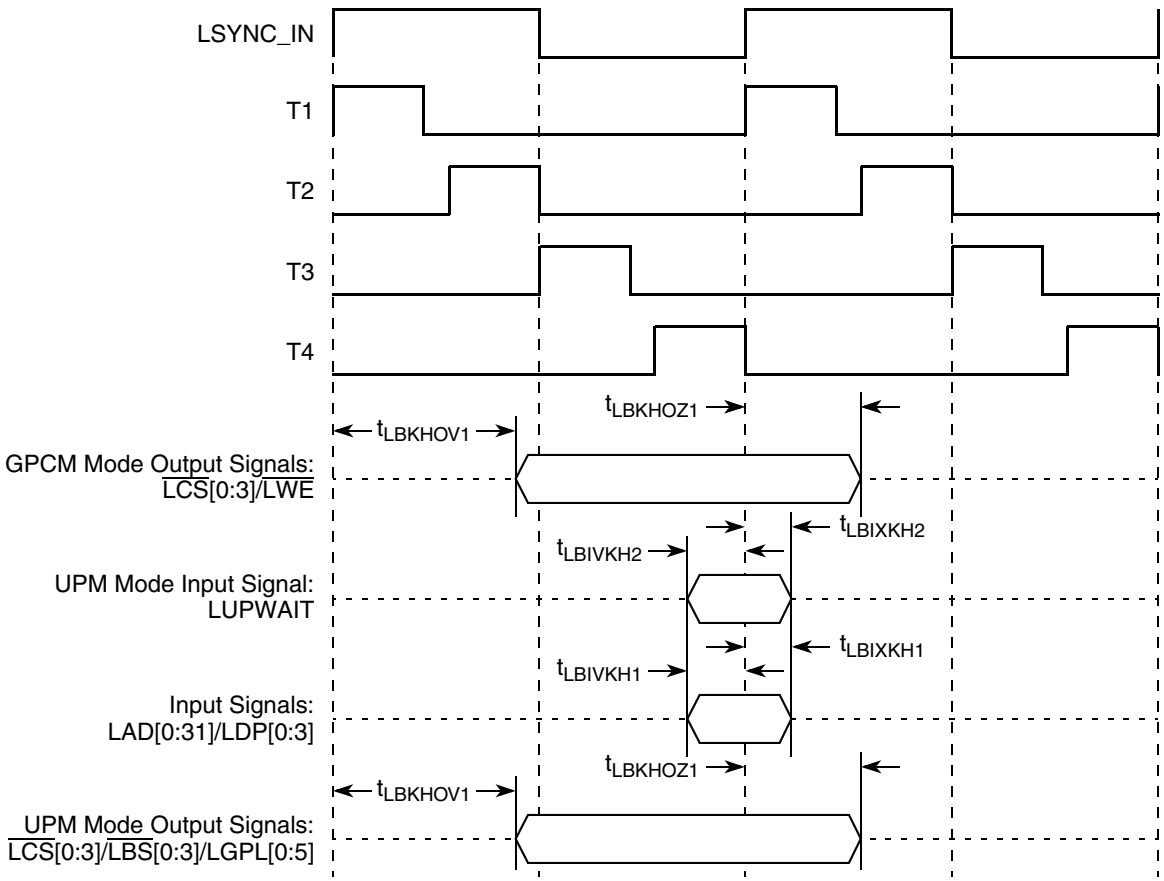



**Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (DLL Enabled)**

# 11 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA.

## 11.1 JTAG DC Electrical Characteristics

Table 40 provides the DC electrical characteristics for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA.

**Table 40. JTAG Interface DC Electrical Characteristics**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | $OV_{DD}$ – 0.3 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |

# 13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8349EA.

## 13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8349EA.

**Table 44. PCI DC Electrical Characteristics**

| Parameter | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | $V_{OUT} \geq V_{OH}$ (min) or | 2 | $OV_{DD}$ + 0.3 | V |
| Low-level input voltage | $V_{IL}$ | $V_{OUT} \leq V_{OL}$ (max) | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | $V_{IN}$[1]= 0 V or $V_{IN}$ = $OV_{DD}$ | — | ±5 | μA |
| High-level output voltage | $V_{OH}$ | $OV_{DD}$ = min, $I_{OH}$ = –100 μA | $OV_{DD}$ – 0.2 | — | V |
| Low-level output voltage | $V_{OL}$ | $OV_{DD}$ = min, $I_{OL}$ = 100 μA | — | 0.2 | V |

**Note:**
1. The symbol $V_{IN}$, in this case, represents the $OV_{IN}$ symbol referenced in Table 1.

## 13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8349EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

**Table 45. PCI AC Timing Specifications at 66 MHz[1]**

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Clock to output valid | $t_{PCKHOV}$ | — | 6.0 | ns | 3 |
| Output hold from clock | $t_{PCKHOX}$ | 1 | — | ns | 3 |
| Clock to output high impedance | $t_{PCKHOZ}$ | — | 14 | ns | 3, 4 |
| Input setup to clock | $t_{PCIVKH}$ | 3.0 | — | ns | 3, 5 |
| Input hold from clock | $t_{PCIXKH}$ | 0 | — | ns | 3, 5 |
| $\overline{REQ64}$ to $\overline{PORESET}$ setup time | $t_{PCRVRH}$ | 5 | — | clocks | 6 |

# 17 SPI

This section describes the SPI DC and AC electrical specifications.

## 17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

**Table 53. SPI DC Electrical Characteristics**

| Parameter | Symbol | Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | — | 2.0 | $OV_{DD}$ + 0.3 | V |
| Input low voltage | $V_{IL}$ | — | –0.3 | 0.8 | V |
| Input current | $I_{IN}$ | — | — | ±5 | μA |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = –8.0 mA | 2.4 | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 8.0 mA | — | 0.5 | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | — | 0.4 | V |

## 17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

**Table 54. SPI AC Timing Specifications[1]**

| Parameter | Symbol[2] | Min | Max | Unit |
|---|---|---|---|---|
| SPI outputs valid—Master mode (internal clock) delay | $t_{NIKHOV}$ | — | 6 | ns |
| SPI outputs hold—Master mode (internal clock) delay | $t_{NIKHOX}$ | 0.5 | — | ns |
| SPI outputs valid—Slave mode (external clock) delay | $t_{NEKHOV}$ | — | 8 | ns |
| SPI outputs hold—Slave mode (external clock) delay | $t_{NEKHOX}$ | 2 | — | ns |
| SPI inputs—Master mode (internal clock input setup time | $t_{NIIVKH}$ | 4 | — | ns |
| SPI inputs—Master mode (internal clock input hold time | $t_{NIIXKH}$ | 0 | — | ns |
| SPI inputs—Slave mode (external clock) input setup time | $t_{NEIVKH}$ | 4 | — | ns |
| SPI inputs—Slave mode (external clock) input hold time | $t_{NEIXKH}$ | 2 | — | ns |

**Notes:**

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{NIKHOX}$ symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

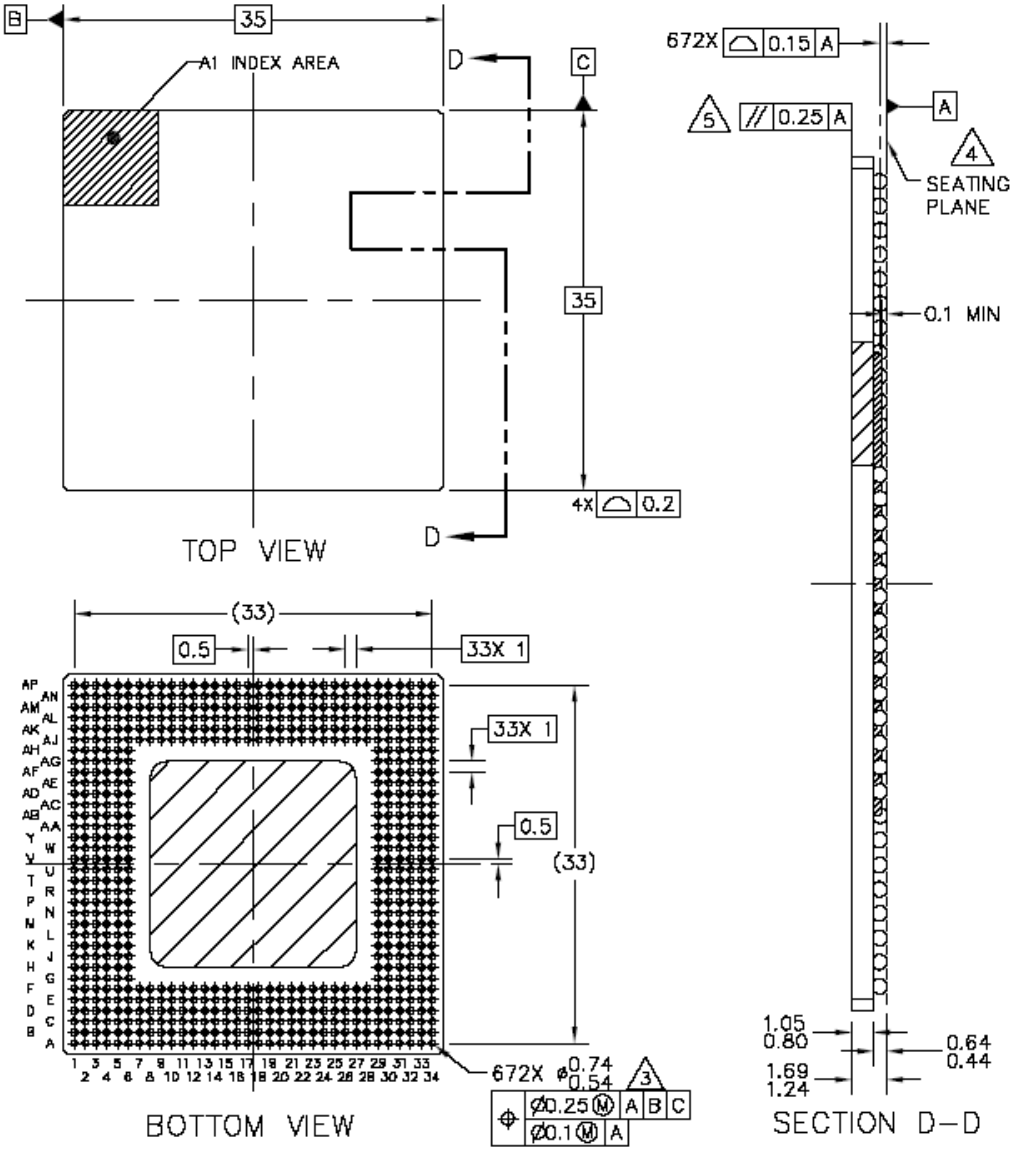
## 18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

| | |
|---|---|
| Package outline | 35 mm × 35 mm |
| Interconnects | 672 |
| Pitch | 1.00 mm |
| Module height (typical) | 1.46 mm |
| Solder balls | 62 Sn/36 Pb/2 Ag (ZU package)<br>96.5 Sn/3.5Ag (VV package) |
| Ball diameter (typical) | 0.64 mm |

## 18.2 Mechanical Dimensions for the MPC8349EA TBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8349EA, 672-TBGA package.




**Notes:**

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

**Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8349EA TBGA**

**Table 55. MPC8349EA (TBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| $\overline{\text{PCI2_FRAME}}$/GPIO2[1] | AE33 | I/O | $OV_{DD}$ | 5 |
| $\overline{\text{PCI2_TRDY}}$/GPIO2[2] | AF32 | I/O | $OV_{DD}$ | 5 |
| $\overline{\text{PCI2_IRDY}}$/GPIO2[3] | AE34 | I/O | $OV_{DD}$ | 5 |
| $\overline{\text{PCI2_STOP}}$/GPIO2[4] | AF34 | I/O | $OV_{DD}$ | 5 |
| $\overline{\text{PCI2_DEVSEL}}$/GPIO2[5] | AF33 | I/O | $OV_{DD}$ | 5 |
| $\overline{\text{PCI2_SERR}}$/$\overline{\text{PCI1_ACK}}$64 | AG33 | I/O | $OV_{DD}$ | 5 |
| $\overline{\text{PCI2_PERR}}$/$\overline{\text{PCI1_REQ}}$64 | AG32 | I/O | $OV_{DD}$ | 5 |
| $\overline{\text{PCI2_REQ}}$[0:2]/GPIO2[6:8] | Y32, Y34, AA32 | I/O | $OV_{DD}$ | — |
| $\overline{\text{PCI2_GNT}}$[0:2]/GPIO2[9:11] | Y31, Y33, AA31 | I/O | $OV_{DD}$ | — |
| M66EN | A19 | I | $OV_{DD}$ | — |
| **DDR SDRAM Memory Interface** | | | | |
| MDQ[0:63] | D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8 | I/O | $GV_{DD}$ | — |
| MECC[0:4]/MSRCID[0:4] | W4, W3, Y3, AA6, T1 | I/O | $GV_{DD}$ | — |
| MECC[5]/MDVAL | U1 | I/O | $GV_{DD}$ | — |
| MECC[6:7] | Y1, Y6 | I/O | $GV_{DD}$ | — |
| MDM[0:8] | B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4 | O | $GV_{DD}$ | — |
| MDQS[0:8] | B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2 | I/O | $GV_{DD}$ | — |
| MBA[0:1] | AD1, AA5 | O | $GV_{DD}$ | — |
| MA[0:14] | W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6 | O | $GV_{DD}$ | — |
| $\overline{\text{MWE}}$ | AF1 | O | $GV_{DD}$ | — |
| $\overline{\text{MRAS}}$ | AF4 | O | $GV_{DD}$ | — |
| $\overline{\text{MCAS}}$ | AG3 | O | $GV_{DD}$ | — |
| $\overline{\text{MCS}}$[0:3] | AG2, AG1, AK1, AL4 | O | $GV_{DD}$ | — |
| MCKE[0:1] | H3, G1 | O | $GV_{DD}$ | 3 |
| MCK[0:5] | U2, F4, AM3, V3, F2, AN3 | O | $GV_{DD}$ | — |
| $\overline{\text{MCK}}$[0:5] | U3, E3, AN2, V4, E1, AM4 | O | $GV_{DD}$ | — |
| MODT[0:3] | AH3, AJ5, AH1, AJ4 | O | $GV_{DD}$ | — |

**Table 55. MPC8349EA (TBGA) Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **Gigabit Reference Clock** | | | | |
| EC_GTX_CLK125 | C8 | I | $LV_{DD1}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 1)** | | | | |
| TSEC1_COL/GPIO2[20] | A17 | I/O | $OV_{DD}$ | — |
| TSEC1_CRS/GPIO2[21] | F12 | I/O | $LV_{DD1}$ | — |
| TSEC1_GTX_CLK | D10 | O | $LV_{DD1}$ | 3 |
| TSEC1_RX_CLK | A11 | I | $LV_{DD1}$ | — |
| TSEC1_RX_DV | B11 | I | $LV_{DD1}$ | — |
| TSEC1_RX_ER/GPIO2[26] | B17 | I/O | $OV_{DD}$ | — |
| TSEC1_RXD[7:4]/GPIO2[22:25] | B16, D16, E16, F16 | I/O | $OV_{DD}$ | — |
| TSEC1_RXD[3:0] | E10, A8, F10, B8 | I | $LV_{DD1}$ | — |
| TSEC1_TX_CLK | D17 | I | $OV_{DD}$ | — |
| TSEC1_TXD[7:4]/GPIO2[27:30] | A15, B15, A14, B14 | I/O | $OV_{DD}$ | — |
| TSEC1_TXD[3:0] | A10, E11, B10, A9 | O | $LV_{DD1}$ | 10 |
| TSEC1_TX_EN | B9 | O | $LV_{DD1}$ | — |
| TSEC1_TX_ER/GPIO2[31] | A16 | I/O | $OV_{DD}$ | — |
| **Three-Speed Ethernet Controller (Gigabit Ethernet 2)** | | | | |
| TSEC2_COL/GPIO1[21] | C14 | I/O | $OV_{DD}$ | — |
| TSEC2_CRS/GPIO1[22] | D6 | I/O | $LV_{DD2}$ | — |
| TSEC2_GTX_CLK | A4 | O | $LV_{DD2}$ | — |
| TSEC2_RX_CLK | B4 | I | $LV_{DD2}$ | — |
| TSEC2_RX_DV/GPIO1[23] | E6 | I/O | $LV_{DD2}$ | — |
| TSEC2_RXD[7:4]/GPIO1[26:29] | A13, B13, C13, A12 | I/O | $OV_{DD}$ | — |
| TSEC2_RXD[3:0]/GPIO1[13:16] | D7, A6, E8, B7 | I/O | $LV_{DD2}$ | — |
| TSEC2_RX_ER/GPIO1[25] | D14 | I/O | $OV_{DD}$ | — |
| TSEC2_TXD[7]/GPIO1[31] | B12 | I/O | $OV_{DD}$ | — |
| TSEC2_TXD[6]/ DR_XCVR_TERM_SEL | C12 | O | $OV_{DD}$ | — |
| TSEC2_TXD[5]/ DR_UTMI_OPMODE1 | D12 | O | $OV_{DD}$ | — |
| TSEC2_TXD[4]/ DR_UTMI_OPMODE0 | E12 | O | $OV_{DD}$ | — |
| TSEC2_TXD[3:0]/GPIO1[17:20] | B5, A5, F8, B6 | I/O | $LV_{DD2}$ | — |

As shown in Figure 41, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, PCI_SYNC_IN × (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr_clk = csb_clk \times (1 + RCWL[DDRCM])$$

*ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{MCK}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu_clk = csb_clk \times (1 + RCWL[LBIUCM])$$

*lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 56 specifies which units have a configurable clock frequency.

**Table 56. Configurable Clock Units**

| Unit | Default Frequency | Options |
|---|---|---|
| TSEC1 | *csb_clk/3* | Off, *csb_clk, csb_clk/2, csb_clk/3* |
| TSEC2, $I^2C1$ | *csb_clk/3* | Off, *csb_clk, csb_clk/2, csb_clk/3* |
| Security core | *csb_clk/3* | Off, *csb_clk,* csb_clk/2, *csb_clk/3* |
| USB DR, USB MPH | *csb_clk/3* | Off, csb_clk, csb_clk/2, *csb_clk/3* |
| PCI1, PCI2 and DMA complex | *csb_clk* | Off, *csb_clk* |

**Table 58. System PLL Multiplication Factors (continued)**

| RCWL[SPMF] | System PLL Multiplication Factor |
|---|---|
| 0111 | × 7 |
| 1000 | × 8 |
| 1001 | × 9 |
| 1010 | × 10 |
| 1011 | × 11 |
| 1100 | × 12 |
| 1101 | × 13 |
| 1110 | × 14 |
| 1111 | × 15 |

As described in Section 19, “Clocking,” the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59 and Table 60 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

**Table 59. CSB Frequency Options for Host Mode**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0010 | 2 : 1 | | | | 133 |
| Low | 0011 | 3 : 1 | | | 100 | 200 |
| Low | 0100 | 4 : 1 | | 100 | 133 | 266 |
| Low | 0101 | 5 : 1 | | 125 | 166 | 333 |

**Table 60. CSB Frequency Options for Agent Mode (continued)**

| CFG_CLKIN_DIV at Reset[1] | SPMF | *csb_clk* : Input Clock Ratio[2] | Input Clock Frequency (MHz)[2] | | | |
|---|---|---|---|---|---|---|
| | | | 16.67 | 25 | 33.33 | 66.67 |
| | | | *csb_clk* Frequency (MHz) | | | |
| Low | 0110 | 6 : 1 | 100 | 150 | 200 | |
| Low | 0111 | 7 : 1 | 116 | 175 | 233 | |
| Low | 1000 | 8 : 1 | 133 | 200 | 266 | |
| Low | 1001 | 9 : 1 | 150 | 225 | 300 | |
| Low | 1010 | 10 : 1 | 166 | 250 | 333 | |
| Low | 1011 | 11 : 1 | 183 | 275 | | |
| Low | 1100 | 12 : 1 | 200 | 300 | | |
| Low | 1101 | 13 : 1 | 216 | 325 | | |
| Low | 1110 | 14 : 1 | 233 | | | |
| Low | 1111 | 15 : 1 | 250 | | | |
| Low | 0000 | 16 : 1 | 266 | | | |
| High | 0010 | 4 : 1 | | 100 | 133 | 266 |
| High | 0011 | 6 : 1 | 100 | 150 | 200 | |
| High | 0100 | 8 : 1 | 133 | 200 | 266 | |
| High | 0101 | 10 : 1 | 166 | 250 | 333 | |
| High | 0110 | 12 : 1 | 200 | 300 | | |
| High | 0111 | 14 : 1 | 233 | | | |
| High | 1000 | 16 : 1 | 266 | | | |

1 CFG_CLKIN_DIV doubles csb_clk if set high.
2 CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

## 19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 61 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 61 should be considered as reserved.

**NOTE**

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

**Table 61. e300 Core PLL Configuration**

| RCWL[COREPLL] | | | *core_clk* : *csb_clk* Ratio | VCO Divider[1] |
|---|---|---|---|---|
| **0–1** | **2–5** | **6** | | |
| **nn** | **0000** | n | PLL bypassed<br>(PLL off, *csb_clk* clocks core directly) | PLL bypassed<br>(PLL off, *csb_clk* clocks core directly) |
| **00** | **0001** | 0 | 1:1 | 2 |
| **01** | **0001** | 0 | 1:1 | 4 |
| **10** | **0001** | 0 | 1:1 | 8 |
| **11** | **0001** | 0 | 1:1 | 8 |
| **00** | **0001** | 1 | 1.5:1 | 2 |
| **01** | **0001** | 1 | 1.5:1 | 4 |
| **10** | **0001** | 1 | 1.5:1 | 8 |
| **11** | **0001** | 1 | 1.5:1 | 8 |
| **00** | **0010** | 0 | 2:1 | 2 |
| **01** | **0010** | 0 | 2:1 | 4 |
| **10** | **0010** | 0 | 2:1 | 8 |
| **11** | **0010** | 0 | 2:1 | 8 |
| **00** | **0010** | 1 | 2.5:1 | 2 |
| **01** | **0010** | 1 | 2.5:1 | 4 |
| **10** | **0010** | 1 | 2.5:1 | 8 |
| **11** | **0010** | 1 | 2.5:1 | 8 |
| **00** | **0011** | 0 | 3:1 | 2 |
| **01** | **0011** | 0 | 3:1 | 4 |
| **10** | **0011** | 0 | 3:1 | 8 |
| **11** | **0011** | 0 | 3:1 | 8 |

[1] Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

$V_2 = (1 \div (1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1 \div V_2 - 1)$. The drive current is then $I_{source} = V_1 \div R_{source}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum $V_{DD}$, nominal $OV_{DD}$, 105°C.

**Table 65. Impedance Characteristics**

| Impedance | Local Bus, Ethernet, DUART, Control, Configuration, Power Management | PCI Signals (Not Including PCI Output Clocks) | PCI Output Clocks (Including PCI_SYNC_OUT) | DDR DRAM | Symbol | Unit |
|---|---|---|---|---|---|---|
| $R_N$ | 42 Target | 25 Target | 42 Target | 20 Target | $Z_0$ | W |
| $R_P$ | 42 Target | 25 Target | 42 Target | 20 Target | $Z_0$ | W |
| Differential | NA | NA | NA | NA | $Z_{DIFF}$ | W |

**Note:** Nominal supply voltages. See Table 1, $T_j$ = 105°C.

## 21.6 Configuration Pin Multiplexing

The MPC8349EA power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

## 21.7 Pull-Up Resistor Requirements

The MPC8349EA requires high resistance pull-up resistors (10 kΩ is recommended) on open-drain pins, including $I^2C$ pins, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, “PowerQUICC Design Checklist.”

# 22 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

**NOTE**

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8349EEC).

**Table 68. Document Revision History (continued)**

| Rev. Number | Date | Substantive Change(s) |
|---|---|---|
| 3 | 11/2006 | • Updated note in introduction.<br>• In the features list in Section 1, “Overview,” updated DDR data rate to show 400 MHz for DDR2 for TBGA parts for silicon 3.x and 400 MHz for DDR2 for TBGA parts for silicon 3.x.<br>• In Section 23, “Ordering Information,” replicated note from document introduction. |
| 2 | 8/2006 | • Changed all references to revision 2.0 silicon to revision 3.0 silicon.<br>• Changed VIH minimum value in Table 40, “JTAG Interface DC Electrical Characteristics,” to $OV_{DD}$ – 0.3.<br>• In Table 44, “PCI DC Electrical Characteristics,” changed high-level input voltage values to min = 2 and max = $OV_{DD}$ + 0.3; changed low-level input voltage values to min = (–0.3) and max = 0.8.<br>• Updated DDR2 I/O power values in Table 5, “MPC8347EA Typical I/O Power Dissipation.”<br>• In Table 66, “Suggested PLL Configurations,” deleted reference-number rows 902 and 703. |
| 1 | 4/2006 | • Removed Table 20, “Timing Parameters for DDR2-400.”<br>• Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, “DDR and DDR2 SDRAM Output AC Timing Specifications,” rows 2 and 3, and in Figure 2, “DDR SDRAM Output Timing Diagram.<br>• Changed Min and Max values for $V_{IH}$ and VIL in Table 40Table 44,“PCI DC Electrical Characteristics.”<br>• In Table 55, “MPC8349EA (TBGA) Pinout Listing,” and Table 52, “MPC8347EA (PBGA) Pinout Listing,” modified rows for MDICO and MDIC1 signals and added note ‘It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor.’<br>• Table 55, “MPC8349EA (TBGA) Pinout Listing,” in row AVDD3 changed power supply from “AVDD3” to ‘—.’ |
| 0 | 3/2006 | Initial public release |