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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349vvajf">https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349vvajf</a>

- Double data rate, DDR1/DDR2 SDRAM memory controller
  - Programmable timing supporting DDR1 and DDR2 SDRAM
  - 32- or 64-bit data interface, up to 400 MHz data rate
  - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
  - DRAM chip configurations from 64 Mbits to 1 Gbit with  $\times 8/\times 16$  data ports
  - Full error checking and correction (ECC) support
  - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep-mode support for SDRAM self refresh
  - Auto refresh
  - On-the-fly power management using CKE
  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual controllers designed to comply with IEEE 802.3<sup>TM</sup>, 802.3u<sup>TM</sup>, 802.3x<sup>TM</sup>, 802.3z<sup>TM</sup>, 802.3ac<sup>TM</sup> standards
  - Ethernet physical interfaces:
    - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
  - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- Dual PCI interfaces
  - Designed to comply with *PCI Specification Revision 2.3*
  - Data bus width options:
    - Dual 32-bit data PCI interfaces operating at up to 66 MHz
    - Single 64-bit data PCI interface operating at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities on both interfaces
  - PCI agent mode on PCI1 interface
  - PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Posting of processor-to-PCI and PCI-to-memory writes

- Complies with USB specification Rev. 2.0
- Can operate as a stand-alone USB device
  - One upstream facing port
  - Six programmable USB endpoints
- Can operate as a stand-alone USB host controller
  - USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
  - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
  - Can operate as a stand-alone USB host controller
    - USB root hub with one or two downstream-facing ports
    - Enhanced host controller interface (EHCI) compatible
    - Complies with *USB Specification Rev. 2.0*
  - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  - Direct connection to a high-speed device without an external hub
  - External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data operating at up to 133 MHz
  - Eight chip selects for eight external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
  - Three protocol engines on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user-programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external  $\overline{\text{INTA}}$  pin in core disable mode.
  - Unique vector number for each interrupt source

## 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings<sup>1</sup>**

Parameter		Symbol	Max Value	Unit	Notes
Core supply voltage		$V_{DD}$	–0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
PLL supply voltage		$AV_{DD}$	–0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
DDR and DDR2 DRAM I/O voltage		$GV_{DD}$	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		$LV_{DD}$	–0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I <sup>2</sup> C, and JTAG I/O voltage		$OV_{DD}$	–0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	$MV_{IN}$	–0.3 to ( $GV_{DD} + 0.3$ )	V	2, 5
	DDR DRAM reference	$MV_{REF}$	–0.3 to ( $GV_{DD} + 0.3$ )	V	2, 5
	Three-speed Ethernet signals	$LV_{IN}$	–0.3 to ( $LV_{DD} + 0.3$ )	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I <sup>2</sup> C, and JTAG signals	$OV_{IN}$	–0.3 to ( $OV_{DD} + 0.3$ )	V	3, 5
	PCI	$OV_{IN}$	–0.3 to ( $OV_{DD} + 0.3$ )	V	6
Storage temperature range		$T_{STG}$	–55 to 150	°C	—

**Notes:**

- <sup>1</sup> Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
- <sup>2</sup> **Caution:**  $MV_{IN}$  must not exceed  $GV_{DD}$  by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- <sup>3</sup> **Caution:**  $OV_{IN}$  must not exceed  $OV_{DD}$  by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- <sup>4</sup> **Caution:**  $LV_{IN}$  must not exceed  $LV_{DD}$  by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- <sup>5</sup> (M,L,O) $V_{IN}$  and  $MV_{REF}$  may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- <sup>6</sup>  $OV_{IN}$  on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.

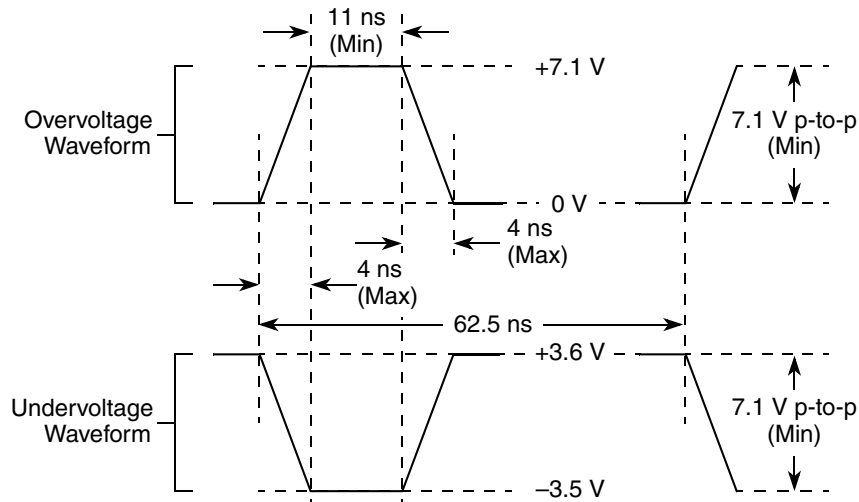


Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

### 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance ( $\Omega$ )	Supply Voltage
Local bus interface utilities signals	40	$OV_{DD} = 3.3\text{ V}$
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	$GV_{DD} = 2.5\text{ V}$
DDR2 signal	18 36 (half-strength mode)	$GV_{DD} = 1.8\text{ V}$
TSEC/10/100 signals	40	$LV_{DD} = 2.5/3.3\text{ V}$
DUART, system control, I <sup>2</sup> C, JTAG, USB	40	$OV_{DD} = 3.3\text{ V}$
GPIO signals	40	$OV_{DD} = 3.3\text{ V}$ , $LV_{DD} = 2.5/3.3\text{ V}$

## 2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8349EA.

### 2.2.1 Power-Up Sequencing

MPC8349EA does not require the core supply voltage ( $V_{DD}$  and  $AV_{DD}$ ) and I/O supply voltages ( $GV_{DD}$ ,  $LV_{DD}$ , and  $OV_{DD}$ ) to be applied in any particular order. During the power ramp up, before the power

supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage ( $V_{DD}$ ) before the I/O voltage ( $GV_{DD}$ ,  $LV_{DD}$ , and  $OV_{DD}$ ) and assert  $\overline{PORESET}$  before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

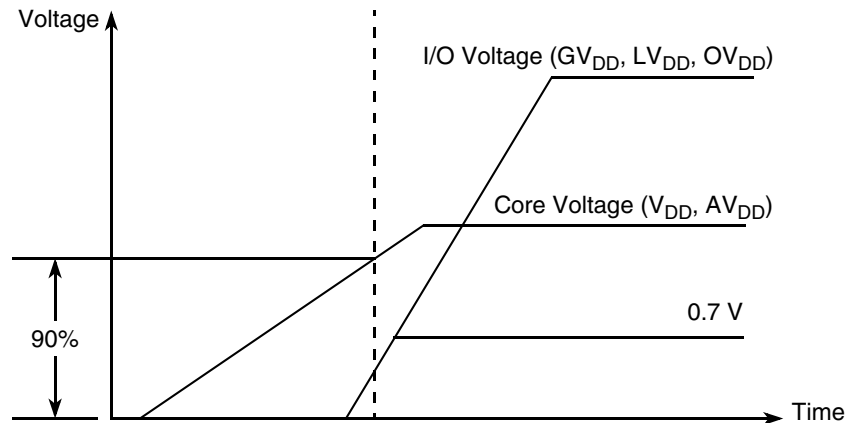


Figure 4. Power Sequencing Example

I/O voltage supplies ( $GV_{DD}$ ,  $LV_{DD}$ , and  $OV_{DD}$ ) do not have any ordering requirements with respect to one another.

### 3 Power Characteristics

The estimated typical power dissipation for the MPC8349EA device is shown in Table 4.

Table 4. MPC8349EA Power Dissipation<sup>1</sup>

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at $T_J = 65$	Typical <sup>2, 3</sup>	Maximum <sup>4</sup>	Unit
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W
	667 <sup>5, 6</sup>	333	3.5	4.6	5	W

<sup>1</sup> The values do not include I/O supply power ( $OV_{DD}$ ,  $LV_{DD}$ ,  $GV_{DD}$ ) or  $AV_{DD}$ . For I/O power values, see Table 5.

## 8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

**Table 31. RGMII and RTBI AC Timing Specifications**

At recommended operating conditions with  $LV_{DD}$  of  $2.5\text{ V} \pm 5\%$ .

Parameter/Condition	Symbol <sup>1</sup>	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	$t_{SKRGT}$	-0.5	—	0.5	ns
Data to clock input skew (at receiver) <sup>2</sup>	$t_{SKRGT}$	1.0	—	2.8	ns
Clock cycle duration <sup>3</sup>	$t_{RGT}$	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T <sup>4, 5</sup>	$t_{RGTH}/t_{RGTF}$	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX <sup>3, 5</sup>	$t_{RGTH}/t_{RGTF}$	40	50	60	%
Rise time (20%–80%)	$t_{RGTR}$	—	—	0.75	ns
Fall time (80%–20%)	$t_{RGTF}$	—	—	0.75	ns

**Notes:**

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of  $t_{RGT}$  represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps,  $t_{RGT}$  scales to  $400\text{ ns} \pm 40\text{ ns}$  and  $40\text{ ns} \pm 4\text{ ns}$ , respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three  $t_{RGT}$  of the lowest speed transitioned.
5. Duty cycle reference is  $LV_{DD}/2$ .

## 10.2 Local Bus AC Electrical Specification

Table 38 and Table 39 describe the general timing parameters of the local bus interface of the MPC8349EA.

**Table 38. Local Bus General Timing Parameters—DLL On**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Local bus cycle time	$t_{LBK}$	7.5	—	ns	2
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	1.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	2.2	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT Input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT1}$	1.5	—	ns	5
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT2}$	3	—	ns	6
LALE output fall to LAD output transition (LATCH hold time)	$t_{LBOTOT3}$	2.5	—	ns	7
Local bus clock to LALE rise	$t_{LBKHLR}$	—	4.5	ns	—
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	4.5	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	4.5	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	4.5	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	1	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	1	—	ns	3
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ}$	—	3.8	ns	8

**Notes:**

1. The symbols for timing specifications follow the pattern of  $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$  for inputs and  $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$  for outputs. For example,  $t_{LBIXKH1}$  symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the  $t_{LBK}$  clock reference (K) goes high (H), in this case for clock one (1). Also,  $t_{LBKHOX}$  symbolizes local bus timing (LB) for the  $t_{LBK}$  clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to the rising edge of LSYNC\_IN.
3. All signals are measured from  $OV_{DD}/2$  of the rising edge of LSYNC\_IN to  $0.4 \times OV_{DD}$  of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5.  $t_{LBOTOT1}$  should be used when RCWH[LALE] is not set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
6.  $t_{LBOTOT2}$  should be used when RCWH[LALE] is set and when the load on the LALE output pin is at least 10 pF less than the load on the LAD output pins.
7.  $t_{LBOTOT3}$  should be used when RCWH[LALE] is set and when the load on the LALE output pin equals the load on the LAD output pins.
8. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.



**Table 41. JTAG AC Timing Specifications (Independent of CLKIN)<sup>1</sup> (continued)**

At recommended operating conditions (see Table 2).

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	
Boundary-scan data	$t_{JTKLDZ}$	2	19		5, 6
TDO	$t_{JTKLOZ}$	2	9		

**Notes:**

1. All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50  $\Omega$  load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of  $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$  for inputs and  $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$  for outputs. For example,  $t_{JTDVXH}$  symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state or setup time. Also,  $t_{JTDVXH}$  symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the  $t_{JTG}$  clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3.  $\overline{TRST}$  is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to  $t_{TCLK}$ .
5. Non-JTAG signal output timing with respect to  $t_{TCLK}$ .
6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8349EA.

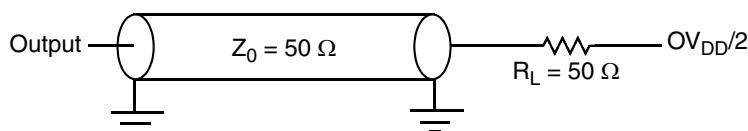
**Figure 27. AC Test Load for the JTAG Interface**

Figure 28 provides the JTAG clock input timing diagram.

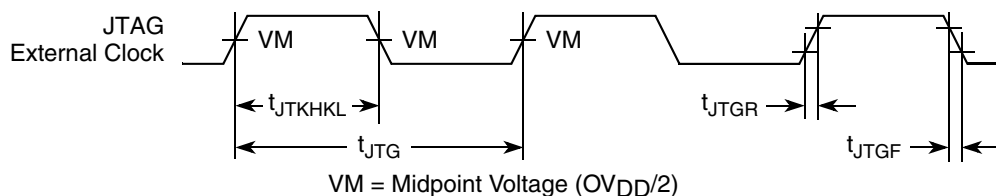
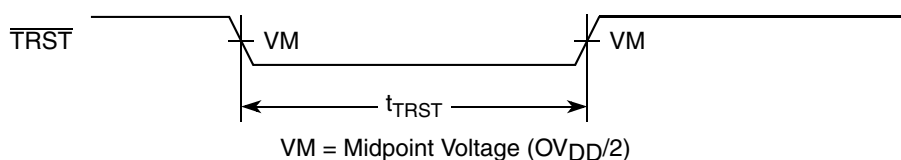
**Figure 28. JTAG Clock Input Timing Diagram**

Figure 29 provides the  $\overline{TRST}$  timing diagram.

**Figure 29.  $\overline{TRST}$  Timing Diagram**

## 13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8349EA.

### 13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8349EA.

**Table 44. PCI DC Electrical Characteristics**

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	$V_{IH}$	$V_{OUT} \geq V_{OH} \text{ (min) or } V_{OUT} \leq V_{OL} \text{ (max)}$	2	$OV_{DD} + 0.3$	V
Low-level input voltage	$V_{IL}$		-0.3	0.8	V
Input current	$I_{IN}$	$V_{IN}^1 = 0 \text{ V or } V_{IN} = OV_{DD}$	—	$\pm 5$	$\mu\text{A}$
High-level output voltage	$V_{OH}$	$OV_{DD} = \text{min, } I_{OH} = -100 \mu\text{A}$	$OV_{DD} - 0.2$	—	V
Low-level output voltage	$V_{OL}$	$OV_{DD} = \text{min, } I_{OL} = 100 \mu\text{A}$	—	0.2	V

**Note:**

1. The symbol  $V_{IN}$ , in this case, represents the  $OV_{IN}$  symbol referenced in Table 1.

### 13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8349EA. Note that the PCI\_CLK or PCI\_SYNC\_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

**Table 45. PCI AC Timing Specifications at 66 MHz<sup>1</sup>**

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
Clock to output valid	$t_{PCKHOV}$	—	6.0	ns	3
Output hold from clock	$t_{PCKHOX}$	1	—	ns	3
Clock to output high impedance	$t_{PCKHOZ}$	—	14	ns	3, 4
Input setup to clock	$t_{PCIVKH}$	3.0	—	ns	3, 5
Input hold from clock	$t_{PCIXKH}$	0	—	ns	3, 5
$\overline{\text{REQ64}}$ to $\overline{\text{PORESET}}$ setup time	$t_{PCRVRH}$	5	—	clocks	6

**Table 45. PCI AC Timing Specifications at 66 MHz<sup>1</sup> (continued)**

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
$\overline{\text{PORESET}}$ to $\overline{\text{REQ64}}$ hold time	$t_{\text{PCRHRX}}$	0	50	ns	6

**Notes:**

1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
2. The symbols for timing specifications follow the pattern of  $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$  for inputs and  $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$  for outputs. For example,  $t_{\text{PCIVKH}}$  symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock,  $t_{\text{SYS}}$ , reference (K) going to the high (H) state or setup time. Also,  $t_{\text{PCRHEV}}$  symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
3. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
5. Input timings are measured at the pin.
6. The setup and hold time is with respect to the rising edge of  $\overline{\text{PORESET}}$ .

Table 46 provides the PCI AC timing specifications at 33 MHz.

**Table 46. PCI AC Timing Specifications at 33 MHz**

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Clock to output valid	$t_{\text{PCKHOV}}$	—	11	ns	2
Output hold from clock	$t_{\text{PCKHOX}}$	2	—	ns	2
Clock to output high impedance	$t_{\text{PCKHOZ}}$	—	14	ns	2, 3
Input setup to clock	$t_{\text{PCIVKH}}$	3.0	—	ns	2, 4
Input hold from clock	$t_{\text{PCIXKH}}$	0	—	ns	2, 4
$\overline{\text{REQ64}}$ to $\overline{\text{PORESET}}$ setup time	$t_{\text{PCRVRH}}$	5	—	clocks	5
$\overline{\text{PORESET}}$ to $\overline{\text{REQ64}}$ hold time	$t_{\text{PCRHRX}}$	0	50	ns	5

**Notes:**

1. The symbols for timing specifications follow the pattern of  $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$  for inputs and  $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$  for outputs. For example,  $t_{\text{PCIVKH}}$  symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock,  $t_{\text{SYS}}$ , reference (K) going to the high (H) state or setup time. Also,  $t_{\text{PCRHEV}}$  symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.
5. The setup and hold time is with respect to the rising edge of  $\overline{\text{PORESET}}$ .

Figure 37 provides the AC test load for the SPI.

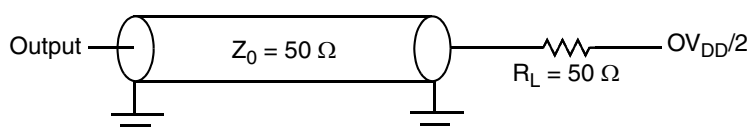
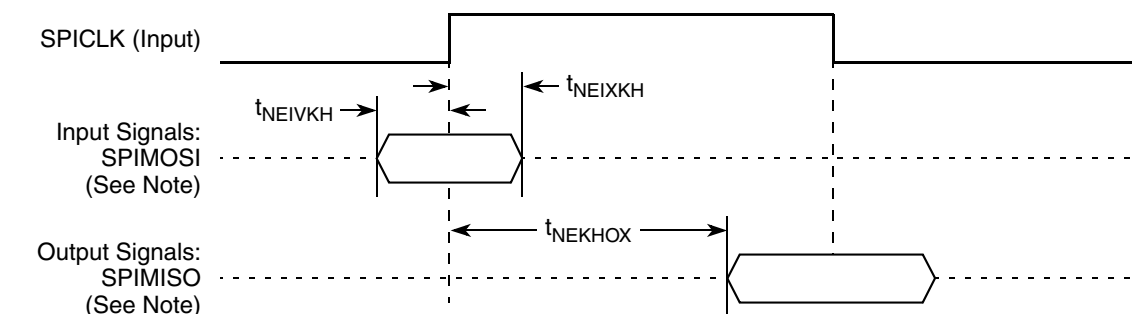


Figure 37. SPI AC Test Load

Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

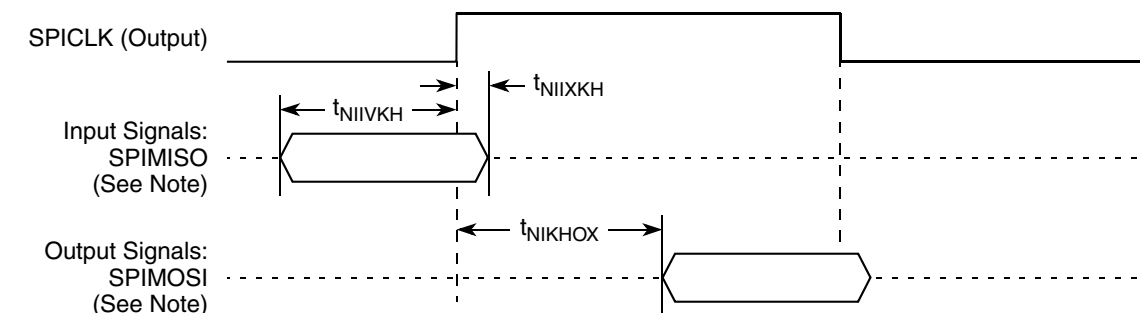
Figure 38 shows the SPI timings in slave mode (external clock).



**Note:** The clock edge is selectable on SPI.

Figure 38. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 39 shows the SPI timings in master mode (internal clock).



**Note:** The clock edge is selectable on SPI.

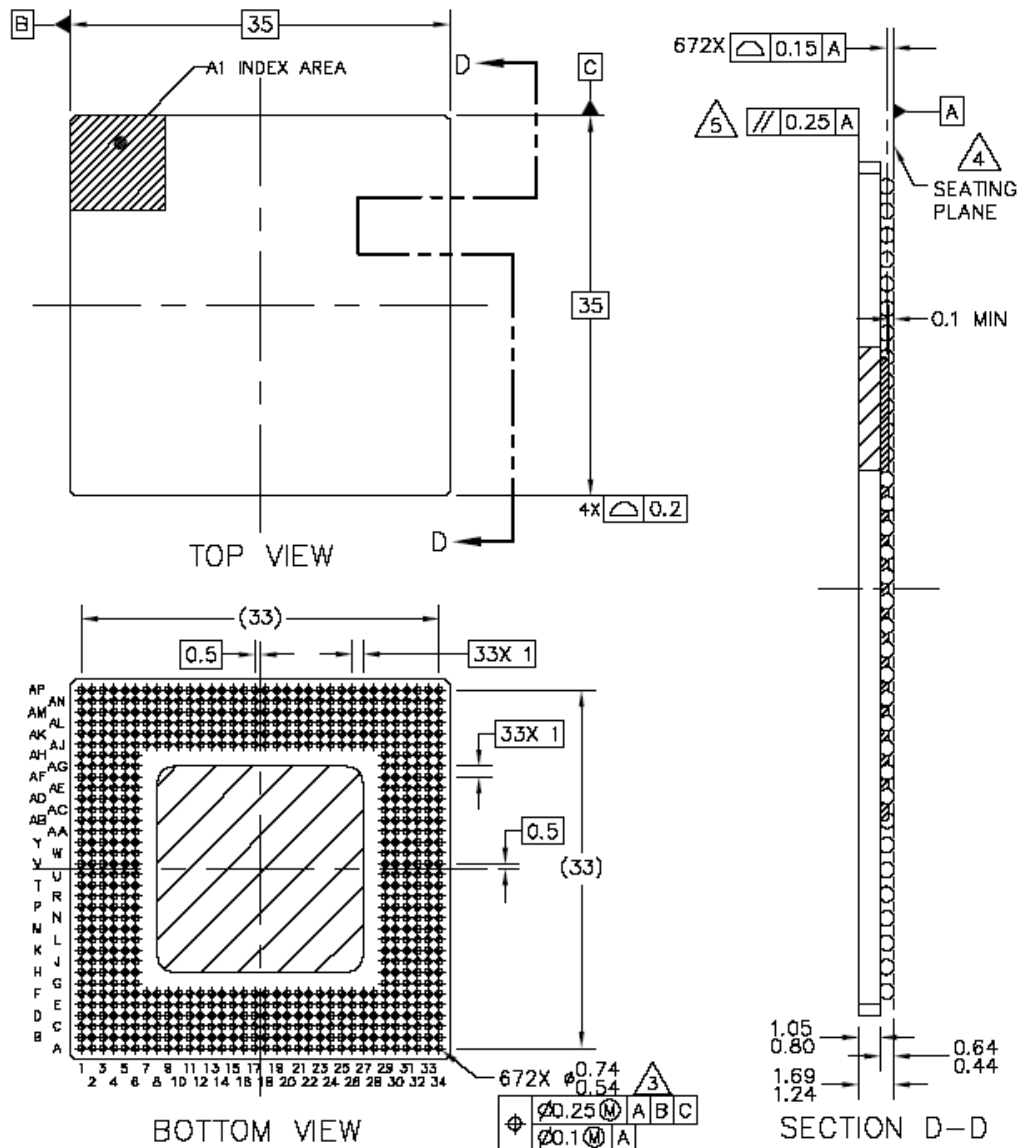
Figure 39. SPI AC Timing in Master Mode (Internal Clock) Diagram

## 18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8349EA is available in a tape ball grid array (TBGA). See Section 18.1, “Package Parameters for the MPC8349EA TBGA” and Section 18.2, “Mechanical Dimensions for the MPC8349EA TBGA.”

## 18.2 Mechanical Dimensions for the MPC8349EA TBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8349EA, 672-TBGA package.



### Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

**Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8349EA TBGA**

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO1[2]/DMA_DDONE0/ GTM1_TOUT1	B25	I/O	OV <sub>DD</sub>	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV <sub>DD</sub>	—
GPIO1[4]/DMA_DACK1/ GTM1_TGATE2/GTM2_TGATE1	A25	I/O	OV <sub>DD</sub>	—
GPIO1[5]/DMA_DDONE1/ GTM1_TOUT2/GTM2_TOUT1	B24	I/O	OV <sub>DD</sub>	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV <sub>DD</sub>	—
GPIO1[7]/DMA_DACK2/ GTM1_TGATE3/GTM2_TGATE4	D23	I/O	OV <sub>DD</sub>	—
GPIO1[8]/DMA_DDONE2/ GTM1_TOUT3	B23	I/O	OV <sub>DD</sub>	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV <sub>DD</sub>	—
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	F22	I/O	OV <sub>DD</sub>	—
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	E22	I/O	OV <sub>DD</sub>	—
<b>USB Port 1</b>				
MPH1_D0_ENABLEN/ DR_D0_ENABLEN	A26	I/O	OV <sub>DD</sub>	—
MPH1_D1_SER_TXD/ DR_D1_SER_TXD	B26	I/O	OV <sub>DD</sub>	—
MPH1_D2_VMO_SE0/ DR_D2_VMO_SE0	D25	I/O	OV <sub>DD</sub>	—
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV <sub>DD</sub>	—
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV <sub>DD</sub>	—
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV <sub>DD</sub>	—
MPH1_D6_SER_RCV/ DR_D6_SER_RCV	D26	I/O	OV <sub>DD</sub>	—
MPH1_D7_DRVVBUS/ DR_D7_DRVVBUS	E26	I/O	OV <sub>DD</sub>	—
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV <sub>DD</sub>	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV <sub>DD</sub>	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	O	OV <sub>DD</sub>	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
<b>Gigabit Reference Clock</b>				
EC_GTX_CLK125	C8	I	LV <sub>DD1</sub>	—
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 1)</b>				
TSEC1_COL/GPIO2[20]	A17	I/O	OV <sub>DD</sub>	—
TSEC1_CRS/GPIO2[21]	F12	I/O	LV <sub>DD1</sub>	—
TSEC1_GTX_CLK	D10	O	LV <sub>DD1</sub>	3
TSEC1_RX_CLK	A11	I	LV <sub>DD1</sub>	—
TSEC1_RX_DV	B11	I	LV <sub>DD1</sub>	—
TSEC1_RX_ER/GPIO2[26]	B17	I/O	OV <sub>DD</sub>	—
TSEC1_RXD[7:4]/GPIO2[22:25]	B16, D16, E16, F16	I/O	OV <sub>DD</sub>	—
TSEC1_RXD[3:0]	E10, A8, F10, B8	I	LV <sub>DD1</sub>	—
TSEC1_TX_CLK	D17	I	OV <sub>DD</sub>	—
TSEC1_TXD[7:4]/GPIO2[27:30]	A15, B15, A14, B14	I/O	OV <sub>DD</sub>	—
TSEC1_TXD[3:0]	A10, E11, B10, A9	O	LV <sub>DD1</sub>	10
TSEC1_TX_EN	B9	O	LV <sub>DD1</sub>	—
TSEC1_TX_ER/GPIO2[31]	A16	I/O	OV <sub>DD</sub>	—
<b>Three-Speed Ethernet Controller (Gigabit Ethernet 2)</b>				
TSEC2_COL/GPIO1[21]	C14	I/O	OV <sub>DD</sub>	—
TSEC2_CRS/GPIO1[22]	D6	I/O	LV <sub>DD2</sub>	—
TSEC2_GTX_CLK	A4	O	LV <sub>DD2</sub>	—
TSEC2_RX_CLK	B4	I	LV <sub>DD2</sub>	—
TSEC2_RX_DV/GPIO1[23]	E6	I/O	LV <sub>DD2</sub>	—
TSEC2_RXD[7:4]/GPIO1[26:29]	A13, B13, C13, A12	I/O	OV <sub>DD</sub>	—
TSEC2_RXD[3:0]/GPIO1[13:16]	D7, A6, E8, B7	I/O	LV <sub>DD2</sub>	—
TSEC2_RX_ER/GPIO1[25]	D14	I/O	OV <sub>DD</sub>	—
TSEC2_TXD[7]/GPIO1[31]	B12	I/O	OV <sub>DD</sub>	—
TSEC2_TXD[6]/ DR_XCVR_TERM_SEL	C12	O	OV <sub>DD</sub>	—
TSEC2_TXD[5]/ DR_UTMI_OPMODE1	D12	O	OV <sub>DD</sub>	—
TSEC2_TXD[4]/ DR_UTMI_OPMODE0	E12	O	OV <sub>DD</sub>	—
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV <sub>DD2</sub>	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	B20	O	OV <sub>DD</sub>	3
TMS	A20	I	OV <sub>DD</sub>	4
TRST	B19	I	OV <sub>DD</sub>	4
<b>Test</b>				
TEST	D22	I	OV <sub>DD</sub>	6
TEST_SEL	AL13	I	OV <sub>DD</sub>	6
<b>PMC</b>				
QUIESCE	A18	O	OV <sub>DD</sub>	—
<b>System Control</b>				
PORESET	C18	I	OV <sub>DD</sub>	—
HRESET	B18	I/O	OV <sub>DD</sub>	1
SRESET	D18	I/O	OV <sub>DD</sub>	2
<b>Thermal Management</b>				
THERM0	K32	I	—	8
<b>Power and Ground Signals</b>				
AV <sub>DD1</sub>	L31	Power for e300 PLL (1.2 V nominal, 1.3 V for 667 MHz)	AV <sub>DD1</sub>	—
AV <sub>DD2</sub>	AP12	Power for system PLL (1.2 V nominal, 1.3 V for 667 MHz)	AV <sub>DD2</sub>	—
AV <sub>DD3</sub>	AE1	Power for DDR DLL (1.2 V nominal, 1.3 V for 667 MHz)	—	—
AV <sub>DD4</sub>	AJ13	Power for LBIU DLL (1.2 V nominal, 1.3 V for 667 MHz)	AV <sub>DD4</sub>	—



Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF2	AD2	I	DDR reference voltage	—

**Notes:**

1. This pin is an open-drain signal. A weak pull-up resistor (1 k $\Omega$ ) should be placed on this pin to OV<sub>DD</sub>.
2. This pin is an open-drain signal. A weak pull-up resistor (2–10 k $\Omega$ ) should be placed on this pin to OV<sub>DD</sub>.
3. During reset, this output is actively driven rather than three-stated.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.
6. This pin must always be tied to GND.
7. This pin must always be left not connected.
8. Thermal sensitive resistor.
9. It is recommended that MDIC0 be tied to GND using an 18.2  $\Omega$  resistor and MDIC1 be tied to DDR power using an 18.2  $\Omega$  resistor.
10. TSEC1\_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.
11. A weak pull-up resistor (2–10 k $\Omega$ ) should be placed on this pin to LV<sub>DD1</sub>.
12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

As shown in [Figure 41](#), the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb\_clk*), the internal clock for the DDR controller (*ddr\_clk*), and the internal clock for the local bus interface unit (*lbiu\_clk*).

The *csb\_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)\} \times SPMF$$

In PCI host mode,  $PCI\_SYNC\_IN \times (1 + CFG\_CLKIN\_DIV)$  is the CLKIN frequency.

The *csb\_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb\_clk* frequency to create the internal clock for the e300 core (*core\_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr\_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + RCWL[DDRCM])$$

*ddr\_clk* is not the external memory bus frequency; *ddr\_clk* passes through the DDR clock divider ( $\div 2$ ) to create the differential DDR memory bus clock outputs (MCK and  $\overline{MCK}$ ). However, the data rate is the same frequency as *ddr\_clk*.

The internal *lbiu\_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + RCWL[LBIUCM])$$

*lbiu\_clk* is not the external local bus frequency; *lbiu\_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC\_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb\_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. [Table 56](#) specifies which units have a configurable clock frequency.

**Table 56. Configurable Clock Units**

Unit	Default Frequency	Options
TSEC1	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
TSEC2, I <sup>2</sup> C1	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
Security core	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
USB DR, USB MPH	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI1, PCI2 and DMA complex	<i>csb_clk</i>	Off, <i>csb_clk</i>

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## 20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

### 20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

$T_J$  = junction temperature (°C)

$T_C$  = case temperature of the package (°C)

$R_{\theta JC}$  = junction-to-case thermal resistance (°C/W)

$P_D$  = power dissipation (W)

## 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8349EA.

### 21.1 System Clocking

The MPC8349EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in [Section 19.1, “System PLL Configuration.”](#)

- The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in [Section 19.2, “Core PLL Configuration.”](#)

## 21.2 PLL Power Supply Filtering

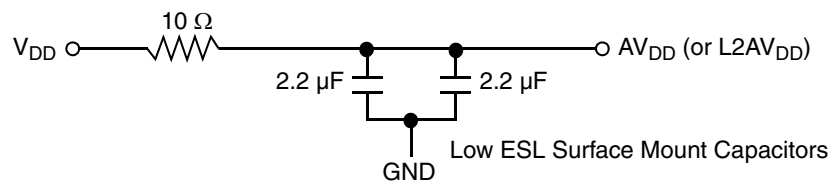
Each PLL gets power through independent power supply pins ( $AV_{DD1}$ ,  $AV_{DD2}$ , respectively). The  $AV_{DD}$  level should always equal to  $V_{DD}$ , and preferably these voltages are derived directly from  $V_{DD}$  through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in [Figure 42](#), one to each of the four  $AV_{DD}$  pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific  $AV_{DD}$  pin being supplied. It should be possible to route directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of package, without the inductance of vias.

[Figure 42](#) shows the PLL power supply filter circuit.



**Figure 42. PLL Power Supply Filter Circuit**

## 21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8349EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8349EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  pin of the device. These capacitors should receive their power from separate  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1  $\mu\text{F}$ . Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

## 22.1 Part Numbers Fully Addressed by This Document

Table 66 shows an analysis of the Freescale part numbering nomenclature for the MPC8349EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

**Table 66. Part Numbering Nomenclature**

MPC	nnnn	e	t	pp	aa	a	r
Product Code	Part Identifier	Encryption Acceleration	Temperature <sup>1</sup> Range	Package <sup>2</sup>	Processor Frequency <sup>3</sup>	Platform Frequency	Revision Level
MPC	8349	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZU = TBGA VV = PB free TBGA	e300 core speed AG = 400 AJ = 533 AL = 667	D = 266 F = 333 <sup>4</sup>	B = 3.1

**Notes:**

1. For temperature range = C, processor frequency is limited to with a platform frequency of 266 and up to 533 with a platform frequency of 333
2. See [Section 18, "Package and Pin Listings,"](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. ALF marked parts support DDR1 data rate up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 data rate up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 data rate up to 333 MHz (at a CSB of 333 MHz).

Table 67 shows the SVR settings by device and package type.

**Table 67. SVR Settings**

Device	Package	SVR (Rev. 3.0)
MPC8349EA	TBGA	8050_0030
MPC8349A	TBGA	8051_0030