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NXP USA Inc. - KMPC8349ZUAGDB Datasheet



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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/kmpc8349zuagdb

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Overview

- On-chip arbitration supporting five masters on PCI1, three masters on PCI2
- Accesses to all PCI address spaces
- Parity supported
- Selectable hardware-enforced coherency
- Address translation units for address mapping between host and peripheral
- Dual address cycle for target
- Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, IEEE Std. 802.11i[®], iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs):
 - Public key execution unit (PKEU) :
 - RSA and Diffie-Hellman algorithms
 - Programmable field size up to 2048 bits
 - Elliptic curve cryptography
 - F2m and F(p) modes
 - Programmable field size up to 511 bits
 - Data encryption standard (DES) execution unit (DEU)
 - DES and 3DES algorithms
 - Two key (K1, K2) or three key (K1, K2, K3) for 3DES
 - ECB and CBC modes for both DES and 3DES
 - Advanced encryption standard unit (AESU)
 - Implements the Rijndael symmetric-key cipher
 - Key lengths of 128, 192, and 256 bits
 - ECB, CBC, CCM, and counter (CTR) modes
 - XOR parity generation accelerator for RAID applications
 - ARC four execution unit (AFEU)
 - Stream cipher compatible with the RC4 algorithm
 - 40- to 128-bit programmable key
 - Message digest execution unit (MDEU)
 - SHA with 160-, 224-, or 256-bit message digest
 - MD5 with 128-bit message digest
 - HMAC with either algorithm
 - Random number generator (RNG)
 - Four crypto-channels, each supporting multi-command descriptor chains
 - Static and/or dynamic assignment of crypto-execution units through an integrated controller
 - Buffer size of 256 bytes for each execution unit, with flow control for large data sizes
- Universal serial bus (USB) dual role controller
 - USB on-the-go mode with both device and host functionality

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.



Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV _{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV _{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV _{DD} = 1.8 V
TSEC/10/100 signals	40	LV _{DD} = 2.5/3.3 V
DUART, system control, I ² C, JTAG, USB	40	OV _{DD} = 3.3 V
GPIO signals	40	OV _{DD} = 3.3 V, LV _{DD} = 2.5/3.3 V

Table 3. Output Drive Capability

2.2 **Power Sequencing**

This section details the power sequencing considerations for the MPC8349EA.

2.2.1 Power-Up Sequencing

MPC8349EA does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD} , LV_{DD} , and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV _{REF}	I _{MVREF}		500	μA	1

Note:

1. The voltage regulator for MV_{REF} must supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	_	MV _{REF} – 0.25	V	_
AC input high voltage	V _{IH}	MV _{REF} + 0.25	—	V	_

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V	—

Parameter	Symbol	Min	Мах	Unit
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	-	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16		2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

Ethernet: Three-Speed Ethernet, MII Management

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V	(continued)
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Parameter	Symbol	Conditions	Min	Мах	Unit
Input high current	I _{IH}	$V_{IN}^{1} = LV_{DD}$	-	10	μA
Input low current	IIL	$V_{IN} = LV_{DD}$	-15	_	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	LV _{DD}	—		2.97	3.63	V
Output high voltage	V _{OH}	I _{OH} = -1.0 mA	$LV_{DD} = Min$	2.10	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND	0.50	V
Input high voltage	V _{IH}	—		2.00	—	V
Input low voltage	V _{IL}	—		-	0.80	V
Input high current	I _{IH}	LV _{DD} = Max	$V_{IN}^{1} = 2.1 V$	_	40	μA
Input low current	۱ _{IL}	LV _{DD} = Max	V _{IN} = 0.5 V	-600	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 34 provides the MII management AC timing specifications.

Table 34. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
MDC frequency	f _{MDC}	_	2.5		MHz	2
MDC period	t _{MDC}		400		ns	_
MDC clock pulse width high	t _{MDCH}	32	—	_	ns	—
MDC to MDIO delay	t _{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t _{MDDVKH}	5	—	_	ns	—
MDIO to MDC hold time	t _{MDDXKH}	0	—	_	ns	—
MDC rise time	t _{MDCR}	_		10	ns	

Local Bus

Figure 21 through Figure 26 show the local bus signals.



Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)



Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)





Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)



Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

JTAG

Figure 30 provides the boundary-scan timing diagram.











Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t _{I2CF}	_	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6	_	μS
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μS
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V

Table 43. I²C AC Electrical Specifications (continued)

Notes:

- 1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2DVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.
- 5.) The device does not follow the "I2C-BUS Specifications" version 2.1 regarding the tI2CF AC parameter.

Figure 32 provides the AC test load for the I^2C .



Figure 32. I²C AC Test Load

Figure 33 shows the AC timing diagram for the I^2C bus.



Figure 33. I²C Bus AC Timing Diagram

15.2 GPIO AC Timing Specifications

Table 50 provides the GPIO input and output AC timing specifications.

Table 50	. GPIO	Input AC	Timing	Specifications ¹
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Parameter	Symbol ²	Min	Unit
GPIO inputs—minimum pulse width	t _{PIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by external synchronous logic. GPIO inputs must be valid for at least t_{PIWID} ns to ensure proper operation.

16 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins.

16.1 IPIC DC Electrical Characteristics

Table 51 provides the DC electrical characteristics for the external interrupt pins.

Table 51. IPIC DC	Electrical Characteristics ¹
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Parameter	Symbol	Condition	Min	Max	Unit	Notes
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	—	-0.3	0.8	V	—
Input current	I _{IN}	—	—	±5	μA	—
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V	2
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V	2

Notes:

1. This table applies for pins \overline{IRQ} [0:7], \overline{IRQ} _OUT, and \overline{MCP} _OUT.

2. IRQ_OUT and MCP_OUT are open-drain pins; thus V_{OH} is not relevant for those pins.

16.2 IPIC AC Timing Specifications

Table 52 provides the IPIC input and output AC timing specifications.

Table 52. IPIC Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
IPIC inputs—minimum pulse width	t _{PICWID}	20	ns

Notes:

1. Input specifications are measured at the 50 percent level of the IPIC input signals. Timings are measured at the pin.

 IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by external synchronous logic. IPIC inputs must be valid for at least t_{PICWID} ns to ensure proper operation in edge triggered mode.

SPI

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications¹

Parameter	Symbol ²	Min	Мах	Unit
SPI outputs valid—Master mode (internal clock) delay	t _{NIKHOV}	_	6	ns
SPI outputs hold—Master mode (internal clock) delay	t _{NIKHOX}	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	t _{NEKHOV}	_	8	ns
SPI outputs hold—Slave mode (external clock) delay	t _{NEKHOX}	2	—	ns
SPI inputs—Master mode (internal clock input setup time	t _{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
</sub>

18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is $35 \text{ mm} \times 35 \text{ mm}$, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MBA[2]	H4	0	GV _{DD}	—
MDIC0	AB1	I/O	—	9
MDIC1	AA1	I/O	—	9
	Local Bus Controller Interface			·
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV _{DD}	_
LDP[0]/CKSTOP_OUT	AM21	I/O	OV _{DD}	—
LDP[1]/CKSTOP_IN	AP22	I/O	OV _{DD}	—
LDP[2]/LCS[4]	AN22	I/O	OV _{DD}	—
LDP[3]/LCS[5]	AM22	I/O	OV _{DD}	—
LA[27:31]	AK21, AP23, AN23, AP24, AK22	0	OV _{DD}	—
LCS[0:3]	AN24, AL23, AP25, AN25	0	OV _{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AK23, AP26, AL24, AM25	0	OV _{DD}	—
LBCTL	AN26	0	OV _{DD}	—
LALE	AK24	0	OV _{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV _{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AL25	I/O	OV _{DD}	—
LGPL2/LSDRAS/LOE	AJ24	0	OV _{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AN27	I/O	OV _{DD}	—
LGPL4/LGTA/LUPWAIT/LPBSE	AP28	I/O	OV _{DD}	12
LGPL5/cfg_clkin_div	AL26	I/O	OV _{DD}	—
LCKE	AM27	0	OV _{DD}	—
LCLK[0:2]	AN28, AK26, AP29	0	OV _{DD}	—
LSYNC_OUT	AM12	0	OV _{DD}	—
LSYNC_IN	AJ10	I	OV _{DD}	—
	General Purpose I/O Timers		•	•
GPIO1[0]/DMA_DREQ0/GTM1_TIN1/ GTM2_TIN2	F24	I/O	OV _{DD}	—
GPIO1[1]/ <u>DMA_DACK0/</u> GTM1_TGATE1/GTM2_TGATE2	E24	I/O	OV _{DD}	—

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO1[2]/DMA_DDONE0/ GTM1_TOUT1	B25	I/O	OV _{DD}	_
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV _{DD}	—
GPIO1[4]/DMA_DACK1/ GTM1_TGATE2/GTM2_TGATE1	A25	I/O	OV _{DD}	—
GPIO1[5]/DMA_DDONE1/ GTM1_TOUT2/GTM2_TOUT1	B24	I/O	OV _{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV _{DD}	—
GPIO1[7]/DMA_DACK2/ GTM1_TGATE3/GTM2_TGATE4	D23	I/O	OV _{DD}	—
GPIO1[8]/DMA_DDONE2/ GTM1_TOUT3	B23	I/O	OV _{DD}	_
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV _{DD}	—
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	F22	I/O	OV _{DD}	—
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	E22	I/O	OV _{DD}	—
	USB Port 1			
MPH1_D0_ENABLEN/ DR_D0_ENABLEN	A26	I/O	OV _{DD}	—
MPH1_D1_SER_TXD/ DR_D1_SER_TXD	B26	I/O	OV _{DD}	—
MPH1_D2_VMO_SE0/ DR_D2_VMO_SE0	D25	I/O	OV _{DD}	—
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV _{DD}	—
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV _{DD}	—
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV _{DD}	—
MPH1_D6_SER_RCV/ DR_D6_SER_RCV	D26	I/O	OV _{DD}	—
MPH1_D7_DRVVBUS/ DR_D7_DRVVBUS	E26	I/O	OV _{DD}	_
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV _{DD}	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV _{DD}	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	0	OV _{DD}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF2	AD2	I	DDR reference voltage	_

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.

2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.

3. During reset, this output is actively driven rather than three-stated.

4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.

6. This pin must always be tied to GND.

7. This pin must always be left not connected.

8. Thermal sensitive resistor.

9. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.

10.TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

11. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to LV_{DD1}.

12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

As shown in Figure 41, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (csb_clk), the internal clock for the DDR controller (ddr_clk), and the internal clock for the local bus interface unit ($lbiu_clk$).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

 $csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$

In PCI host mode, PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV) is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

 $ddr_clk = csb_clk \times (1 + RCWL[DDRCM])$

 ddr_clk is not the external memory bus frequency; ddr_clk passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as ddr_clk .

The internal *lbiu_clk* frequency is determined by the following equation:

 $lbiu_clk = csb_clk \times (1 + RCWL[LBIUCM])$

lbiu_clk is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. Table 56 specifies which units have a configurable clock frequency.

Unit	Default Frequency	Options
TSEC1	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
TSEC2, I ² C1	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
Security core	csb_clk/3	Off, csb_clk, csb_clk/2, csb_clk/3
USB DR, USB MPH	csb_clk/3	Off, csb_clk, csb_clk/2, <i>csb_clk/3</i>
PCI1, PCI2 and DMA complex	csb_clk	Off, csb_clk

RCWL[SPMF]	System PLL Multiplication Factor
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

Table 58. System	n PLL Multi	plication	Factors	(continued))
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As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59 and Table 60 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
				<i>csb_clk</i> Frequency (MHz)		
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333

Table 59. CSB Frequency Options for Host Mode

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
				<i>csb_clk</i> Freq	uency (MHz)	
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

Table 60. CSB Frequency Options for Agent Mode (continued)

¹ CFG_CLKIN_DIV doubles csb_clk if set high.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 61 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 61 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

Thermal

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

 $T_J = T_A + (R_{\theta JA} \times P_D)$

where:

 T_J = junction temperature (°C)

 T_A = ambient temperature for the package (°C)

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 T_J = junction temperature (°C)

 T_T = thermocouple temperature on top of package (°C)

 Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8349EA.

21.5 Output Buffer DC Impedance

The MPC8349EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 43). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.



Figure 43. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is