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Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8349czuajfb

- Double data rate, DDR1/DDR2 SDRAM memory controller
 - Programmable timing supporting DDR1 and DDR2 SDRAM
 - 32- or 64-bit data interface, up to 400 MHz data rate
 - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
 - DRAM chip configurations from 64 Mbits to 1 Gbit with $\times 8/\times 16$ data ports
 - Full error checking and correction (ECC) support
 - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
 - Contiguous or discontiguous memory mapping
 - Read-modify-write support
 - Sleep-mode support for SDRAM self refresh
 - Auto refresh
 - On-the-fly power management using CKE
 - Registered DIMM support
 - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3TM, 802.3uTM, 802.3xTM, 802.3zTM, 802.3acTM standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- Dual PCI interfaces
 - Designed to comply with *PCI Specification Revision 2.3*
 - Data bus width options:
 - Dual 32-bit data PCI interfaces operating at up to 66 MHz
 - Single 64-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities on both interfaces
 - PCI agent mode on PCI1 interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes

- Complies with USB specification Rev. 2.0
- Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints
- Can operate as a stand-alone USB host controller
 - USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
 - Can operate as a stand-alone USB host controller
 - USB root hub with one or two downstream-facing ports
 - Enhanced host controller interface (EHCI) compatible
 - Complies with *USB Specification Rev. 2.0*
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
 - Direct connection to a high-speed device without an external hub
 - External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects for eight external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
 - Three protocol engines on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user-programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
 - Programmable highest priority request
 - Four groups of interrupts with programmable priority
 - External and internal interrupts directed to host processor
 - Redirects interrupts to external $\overline{\text{INTA}}$ pin in core disable mode.
 - Unique vector number for each interrupt source

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}^2	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	40	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-600	—	μA

Notes:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. GMII/MI pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$LV_{DD} = \text{Min}$	1.7	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	$LV_{DD} = \text{Min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8349EA.

9.1 USB DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the USB interface.

Table 35. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, $I_{OH} = -100\ \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100\ \mu A$	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 36 describes the general timing parameters of the USB interface of the MPC8349EA.

Table 36. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol ¹	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	$t_{USKH OV}$	—	7	ns	2–5
Output hold from USB clock—all outputs	$t_{USKH OX}$	2	—	ns	2–5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, $t_{USKH OX}$ symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

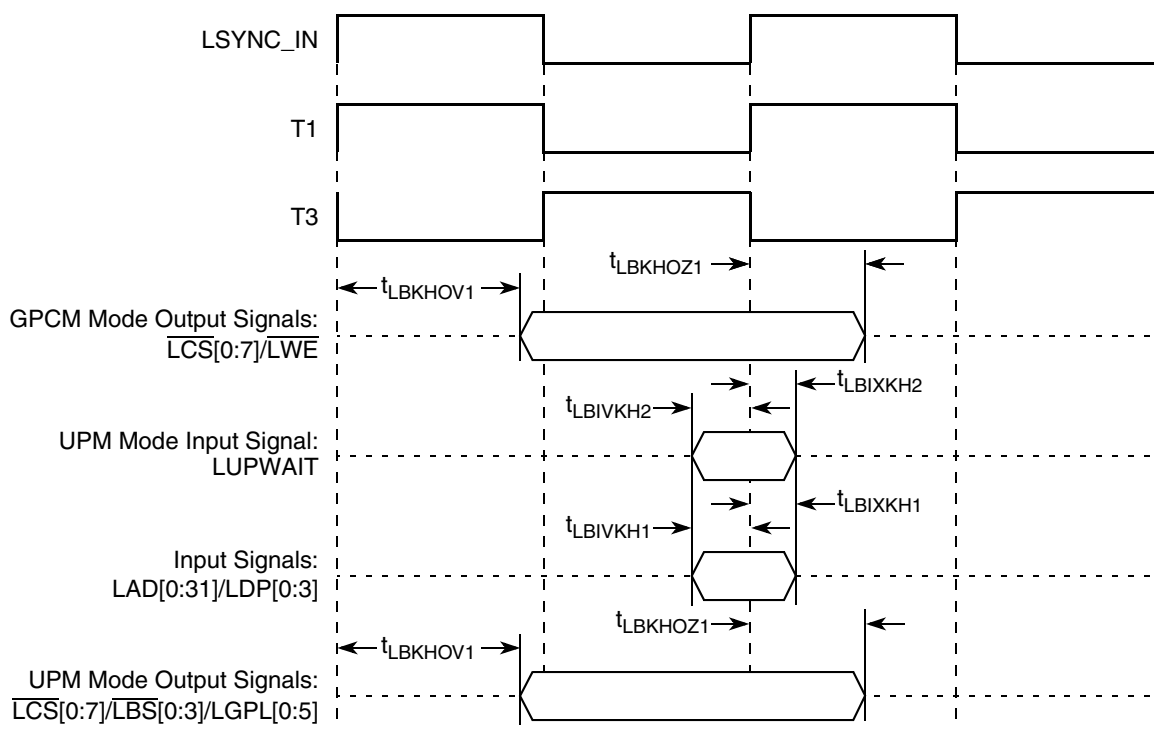


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

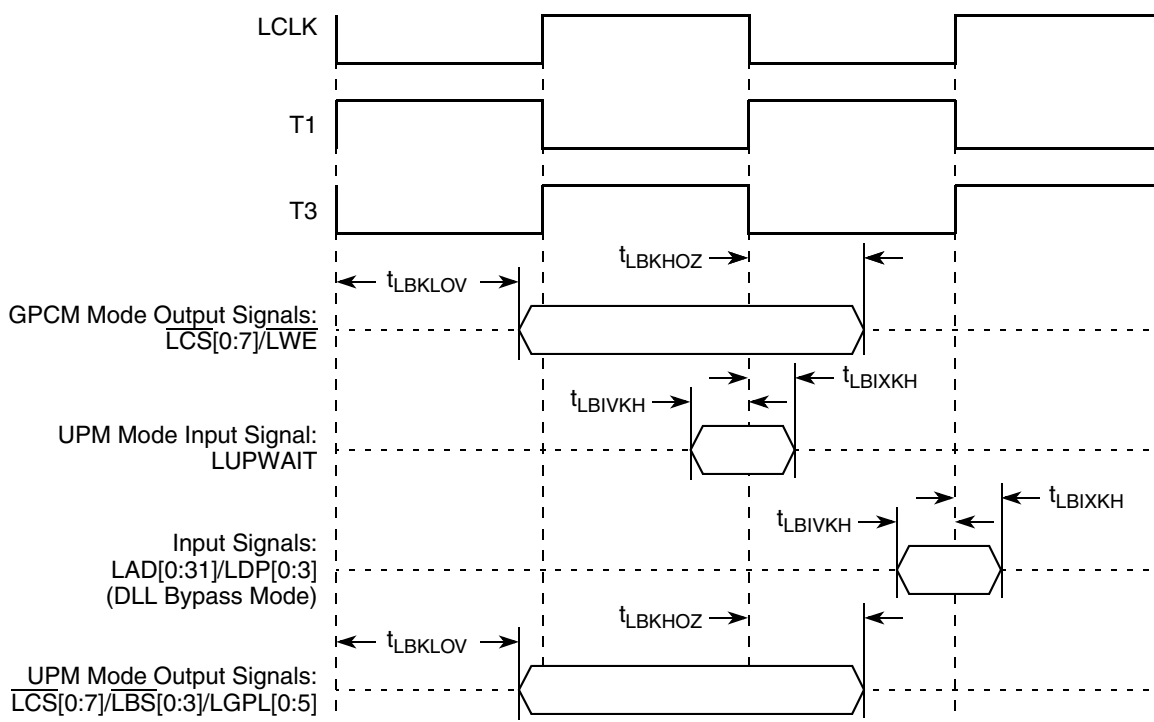


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance:				ns	
Boundary-scan data	t_{JTKLDZ}	2	19		5, 6
TDO	t_{JTKLOZ}	2	9		

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDVXH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. \overline{TRST} is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8349EA.

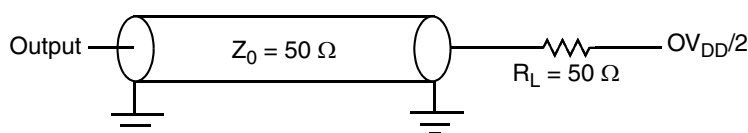
**Figure 27. AC Test Load for the JTAG Interface**

Figure 28 provides the JTAG clock input timing diagram.

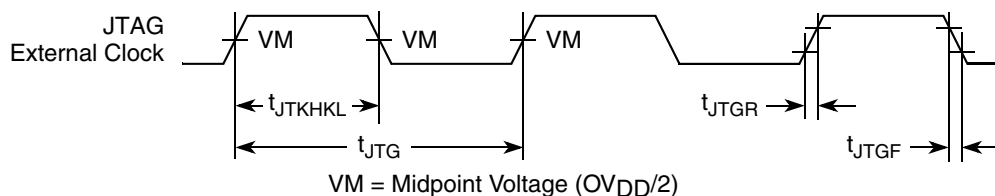
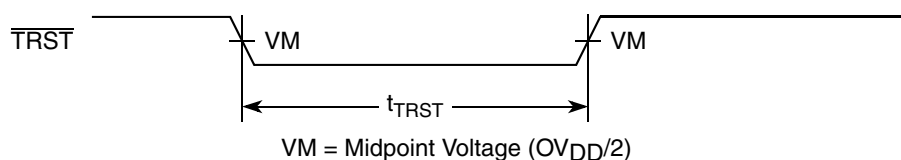
**Figure 28. JTAG Clock Input Timing Diagram**

Figure 29 provides the \overline{TRST} timing diagram.

**Figure 29. \overline{TRST} Timing Diagram**

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications¹

Parameter	Symbol ²	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	$t_{NIKH OV}$	—	6	ns
SPI outputs hold—Master mode (internal clock) delay	$t_{NIKH OX}$	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	$t_{NEKH OV}$	—	8	ns
SPI outputs hold—Slave mode (external clock) delay	$t_{NEKH OX}$	2	—	ns
SPI inputs—Master mode (internal clock input setup time)	$t_{NIIV KH}$	4	—	ns
SPI inputs—Master mode (internal clock input hold time)	$t_{NIIX KH}$	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	$t_{NEIV KH}$	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	$t_{NEIX KH}$	2	—	ns

Notes:

- Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{NIKH OX}$ symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

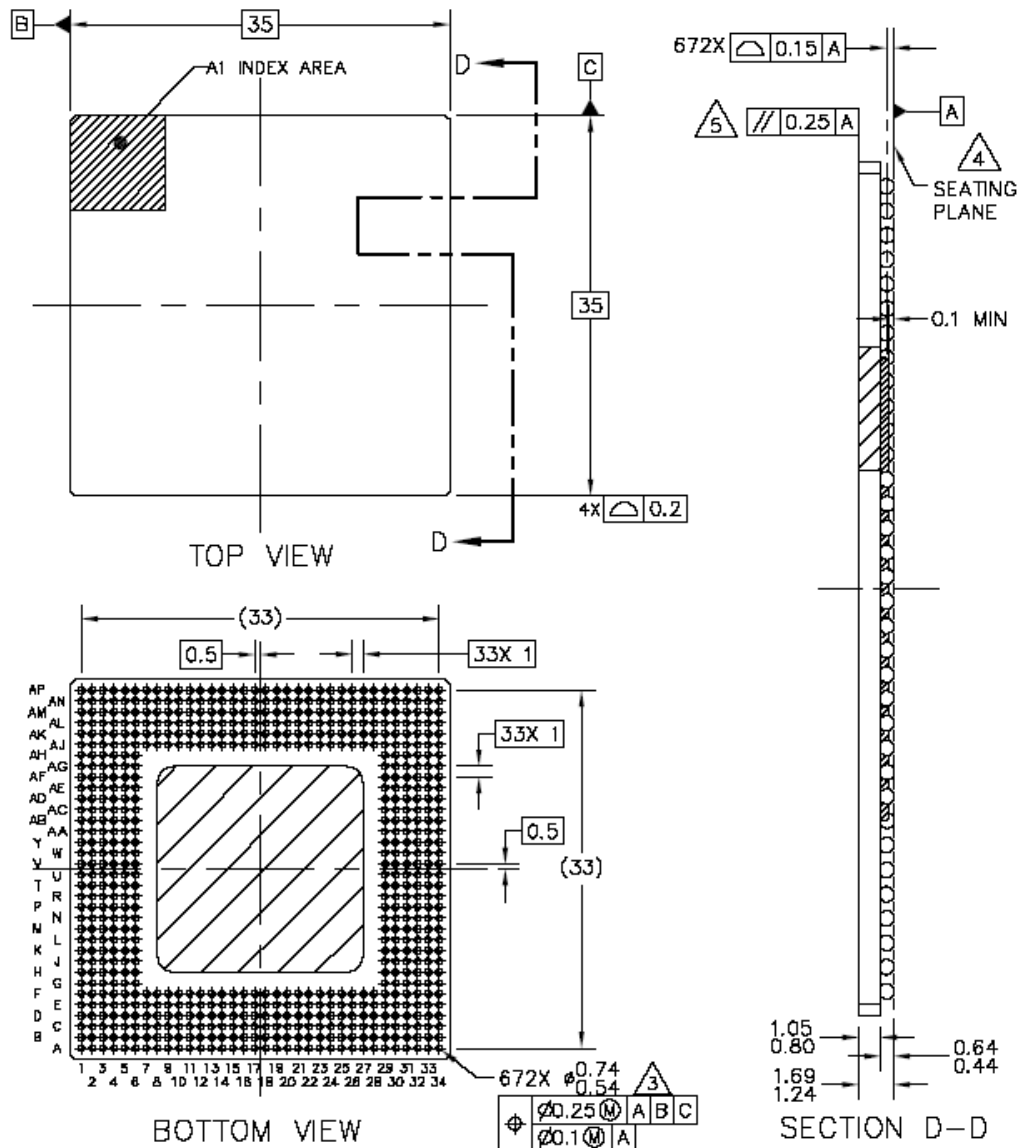
18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

18.2 Mechanical Dimensions for the MPC8349EA TBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8349EA, 672-TBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8349EA TBGA

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV _{DD}	—
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	O	OV _{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	O	OV _{DD}	—
MPH1_CLK/DR_CLK	B29	I	OV _{DD}	—
USB Port 0				
MPH0_D0_ENABLEN/ DR_D8_CHGVBUS	C29	I/O	OV _{DD}	—
MPH0_D1_SER_TXD/ DR_D9_DCHGVBUS	A30	I/O	OV _{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	E28	I/O	OV _{DD}	—
MPH0_D3_SPEED/DR_D11_DMMD	B30	I/O	OV _{DD}	—
MPH0_D4_DP/DR_D12_VBUS_VLD	C30	I/O	OV _{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	A31	I/O	OV _{DD}	—
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV _{DD}	—
MPH0_D7_DRVVBUS/ DR_D15_IDPULLUP	C31	I/O	OV _{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	B32	I	OV _{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	A32	I/O	OV _{DD}	—
MPH0_STP_SUSPEND/ DR_TX_READY	A33	I/O	OV _{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	C32	I	OV _{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	D31	I/O	OV _{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	E30	I/O	OV _{DD}	—
MPH0_CLK/DR_RX_VALID	B33	I	OV _{DD}	—
Programmable Interrupt Controller				
MCP_OUT	AN33	O	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	C19	I/O	OV _{DD}	—
IRQ[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV _{DD}	—
IRQ[6]/GPIO2[18]/CKSTOP_OUT	A21	I/O	OV _{DD}	—
IRQ[7]/GPIO2[19]/CKSTOP_IN	C20	I/O	OV _{DD}	—
Ethernet Management Interface				
EC_MDC	A7	O	LV _{DD1}	—
EC_MDIO	E9	I/O	LV _{DD1}	11

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV _{DD}	—
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV _{DD2}	—
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV _{DD}	—
UART				
UART_SOUT[1:2]/MSRCID[0:1]/LSRCID[0:1]	AK27, AN29	O	OV _{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/LSRCID[2:3]	AL28, AM29	I/O	OV _{DD}	—
UART_CTS[1]/MSRCID4/LSRCID4	AP30	I/O	OV _{DD}	—
UART_CTS[2]/MDVAL/ LDVAL	AN30	I/O	OV _{DD}	—
UART_RTS[1:2]	AP31, AM30	O	OV _{DD}	—
I²C interface				
IIC1_SDA	AK29	I/O	OV _{DD}	2
IIC1_SCL	AP32	I/O	OV _{DD}	2
IIC2_SDA	AN31	I/O	OV _{DD}	2
IIC2_SCL	AM31	I/O	OV _{DD}	2
SPI				
SPIMOSI/LCS[6]	AN32	I/O	OV _{DD}	—
SPIMISO/LCS[7]	AP33	I/O	OV _{DD}	—
SPICLK	AK30	I/O	OV _{DD}	—
SPISEL	AL31	I	OV _{DD}	—
Clocks				
PCI_CLK_OUT[0:2]	AN9, AP9, AM10,	O	OV _{DD}	—
PCI_CLK_OUT[3]/LCS[6]	AN10	O	OV _{DD}	—
PCI_CLK_OUT[4]/LCS[7]	AJ11	O	OV _{DD}	—
PCI_CLK_OUT[5:7]	AP10, AL11, AM11	O	OV _{DD}	—
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV _{DD}	—
PCI_SYNC_OUT	AP11	O	OV _{DD}	3
RTC/PIT_CLOCK	AM32	I	OV _{DD}	—
CLKIN	AM9	I	OV _{DD}	—
JTAG				
TCK	E20	I	OV _{DD}	—
TDI	F20	I	OV _{DD}	4

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	—	—	—
GV _{DD}	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV _{DD}	—
LV _{DD1}	C9, D11	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV _{DD1}	—
LV _{DD2}	C6, D9	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV _{DD2}	—
V _{DD}	E19, E29, F7, F9, F11, F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V _{DD}	—
OV _{DD}	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV _{DD}	—
MVREF1	M3	I	DDR reference voltage	—

Table 60. CSB Frequency Options for Agent Mode (continued)

CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	4 : 1		100	133	266
High	0011	6 : 1	100	150	200	
High	0100	8 : 1	133	200	266	
High	0101	10 : 1	166	250	333	
High	0110	12 : 1	200	300		
High	0111	14 : 1	233			
High	1000	16 : 1	266			

¹ CFG_CLKIN_DIV doubles *csb_clk* if set high.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

19.2 Core PLL Configuration

RCWL[COREPLL] selects the ratio between the internal coherent system bus clock (*csb_clk*) and the e300 core clock (*core_clk*). Table 61 shows the encodings for RCWL[COREPLL]. COREPLL values that are not listed in Table 61 should be considered as reserved.

NOTE

Core VCO frequency = core frequency × VCO divider

VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta CA}$ = case-to-ambient thermal resistance ($^{\circ}\text{C}/\text{W}$)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 64 shows heat sink thermal resistance for TBGA of the MPC8349EA.

Table 64. Heat Sink and Thermal Resistance of MPC8349EA (TBGA)

Heat Sink Assuming Thermal Grease	Air Flow	35 × 35 mm TBGA
		Thermal Resistance
AAVID 30 × 30 × 9.4 mm pin fin	Natural convection	10
AAVID 30 × 30 × 9.4 mm pin fin	1 m/s	6.5
AAVID 30 × 30 × 9.4 mm pin fin	2 m/s	5.6
AAVID 31 × 35 × 23 mm pin fin	Natural convection	8.4
AAVID 31 × 35 × 23 mm pin fin	1 m/s	4.7
AAVID 31 × 35 × 23 mm pin fin	2 m/s	4
Wakefield, 53 × 53 × 25 mm pin fin	Natural convection	5.7
Wakefield, 53 × 53 × 25 mm pin fin	1 m/s	3.5
Wakefield, 53 × 53 × 25 mm pin fin	2 m/s	2.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	Natural convection	6.7
MEI, 75 × 85 × 12 no adjacent board, extrusion	1 m/s	4.1
MEI, 75 × 85 × 12 no adjacent board, extrusion	2 m/s	2.8
MEI, 75 × 85 × 12 mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

The Bergquist Company
 18930 West 78th St.
 Chanhassen, MN 55317
 Internet: www.bergquistcompany.com

800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8349EA.

21.1 System Clocking

The MPC8349EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in [Section 19.1, “System PLL Configuration.”](#)

22.1 Part Numbers Fully Addressed by This Document

Table 66 shows an analysis of the Freescale part numbering nomenclature for the MPC8349EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

Table 66. Part Numbering Nomenclature

MPC	nnnn	e	t	pp	aa	a	r
Product Code	Part Identifier	Encryption Acceleration	Temperature ¹ Range	Package ²	Processor Frequency ³	Platform Frequency	Revision Level
MPC	8349	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZU = TBGA VV = PB free TBGA	e300 core speed AG = 400 AJ = 533 AL = 667	D = 266 F = 333 ⁴	B = 3.1

Notes:

1. For temperature range = C, processor frequency is limited to with a platform frequency of 266 and up to 533 with a platform frequency of 333
2. See [Section 18, "Package and Pin Listings,"](#) for more information on available package types.
3. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
4. ALF marked parts support DDR1 data rate up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 data rate up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 data rate up to 333 MHz (at a CSB of 333 MHz).

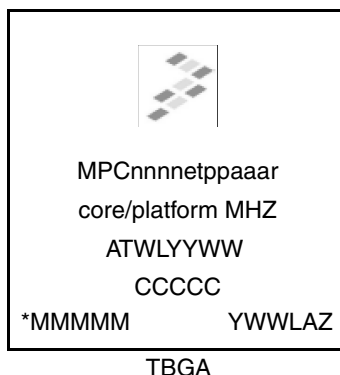
Table 67 shows the SVR settings by device and package type.

Table 67. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8349EA	TBGA	8050_0030
MPC8349A	TBGA	8051_0030

22.2 Part Marking

Parts are marked as in the example shown in [Figure 44](#).



Notes:

ATWLYYWW is the traceability code.

CCCCC is the country code.

MMMMM is the mask number.

YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA Devices

23 Document Revision History

This table provides a revision history of this document.

Table 68. Document Revision History

Rev. Number	Date	Substantive Change(s)
13	09/2011	<ul style="list-style-type: none"> In Section 2.2, "Power Sequencing," added Section 2.2.1, "Power-Up Sequencing" and Figure 4. In Table 25, Table 29 and Table 31, removed the GTX_CLK125. In Table 34, updated t_{MDKHDx} Max value from 170ns to 70ns.
12	11/2010	<ul style="list-style-type: none"> In Table 55 added note for pin LGPL4. In Section 21.7, "Pull-Up Resistor Requirements, updated the list of open drain type pins.
11	05/2010	<ul style="list-style-type: none"> In Table 25 through Table 30, changed $V_{IL}(\text{min})$ to $V_{IH}(\text{max})$ to (20%–80%). Added Table 8, "EC GTX_CLK125 AC Timing Specifications."
10	5/2009	<ul style="list-style-type: none"> In Table 57, updated frequency for max csb_clk to 333 MHz and DDR2, from 100-200 to 100-133 at core frequency = 533MHz. In Section 18.1, "Package Parameters for the MPC8349EA TBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. In Table 66, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.

Table 68. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
3	11/2006	<ul style="list-style-type: none"> Updated note in introduction. In the features list in Section 1, "Overview," updated DDR data rate to show 400 MHz for DDR2 for TBGA parts for silicon 3.x and 400 MHz for DDR2 for TBGA parts for silicon 3.x. In Section 23, "Ordering Information," replicated note from document introduction.
2	8/2006	<ul style="list-style-type: none"> Changed all references to revision 2.0 silicon to revision 3.0 silicon. Changed VIH minimum value in Table 40, "JTAG Interface DC Electrical Characteristics," to $OV_{DD} - 0.3$. In Table 44, "PCI DC Electrical Characteristics," changed high-level input voltage values to min = 2 and max = $OV_{DD} + 0.3$; changed low-level input voltage values to min = (-0.3) and max = 0.8. Updated DDR2 I/O power values in Table 5, "MPC8347EA Typical I/O Power Dissipation." In Table 66, "Suggested PLL Configurations," deleted reference-number rows 902 and 703.
1	4/2006	<ul style="list-style-type: none"> Removed Table 20, "Timing Parameters for DDR2-400." Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, "DDR and DDR2 SDRAM Output AC Timing Specifications," rows 2 and 3, and in Figure 2, "DDR SDRAM Output Timing Diagram." Changed Min and Max values for V_{IH} and V_{IL} in Table 40Table 44, "PCI DC Electrical Characteristics." In Table 55, "MPC8349EA (TBGA) Pinout Listing," and Table 52, "MPC8347EA (PBGA) Pinout Listing," modified rows for MDICO and MDIC1 signals and added note 'It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor.' Table 55, "MPC8349EA (TBGA) Pinout Listing," in row AVDD3 changed power supply from "AVDD3" to '—.'
0	3/2006	Initial public release

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