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Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8349ecvvagdb

- Double data rate, DDR1/DDR2 SDRAM memory controller
 - Programmable timing supporting DDR1 and DDR2 SDRAM
 - 32- or 64-bit data interface, up to 400 MHz data rate
 - Up to four physical banks (chip selects), each bank up to 1 Gbyte independently addressable
 - DRAM chip configurations from 64 Mbits to 1 Gbit with $\times 8/\times 16$ data ports
 - Full error checking and correction (ECC) support
 - Support for up to 16 simultaneous open pages (up to 32 pages for DDR2)
 - Contiguous or discontiguous memory mapping
 - Read-modify-write support
 - Sleep-mode support for SDRAM self refresh
 - Auto refresh
 - On-the-fly power management using CKE
 - Registered DIMM support
 - 2.5-V SSTL2 compatible I/O for DDR1, 1.8-V SSTL2 compatible I/O for DDR2
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
 - Dual controllers designed to comply with IEEE 802.3™, 802.3u™, 802.3x™, 802.3z™, 802.3ac™ standards
 - Ethernet physical interfaces:
 - 1000 Mbps IEEE Std. 802.3 GMII/RGMII, IEEE Std. 802.3z TBI/RTBI, full-duplex
 - 10/100 Mbps IEEE Std. 802.3 MII full- and half-duplex
 - Buffer descriptors are backward-compatible with MPC8260 and MPC860T 10/100 programming models
 - 9.6-Kbyte jumbo frame support
 - RMON statistics support
 - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
 - MII management interface for control and status
 - Programmable CRC generation and checking
- Dual PCI interfaces
 - Designed to comply with *PCI Specification Revision 2.3*
 - Data bus width options:
 - Dual 32-bit data PCI interfaces operating at up to 66 MHz
 - Single 64-bit data PCI interface operating at up to 66 MHz
 - PCI 3.3-V compatible
 - PCI host bridge capabilities on both interfaces
 - PCI agent mode on PCI1 interface
 - PCI-to-memory and memory-to-PCI streaming
 - Memory prefetching of PCI read accesses and support for delayed read transactions
 - Posting of processor-to-PCI and PCI-to-memory writes

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) $\pm$ 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
ADDR/CMD/MODT output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	1.95 2.40 3.15 4.20	— — — —	ns	3
ADDR/CMD/MODT output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	$t_{DDKHCSX}$	1.95 2.40 3.15 4.20	— — — —	ns	3
MCK to MDQS Skew	t_{DDKMH}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	700 775 1100 1200	— — — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	700 900 1100 1200	— — — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)At recommended operating conditions with GV_{DD} of $(1.8 \text{ or } 2.5 \text{ V}) \pm 5\%$.

Parameter	Symbol ¹	Min	Max	Unit	Notes
MDQS epilogue end	t_{DDKHME}	-0.6	0.6	ns	6

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output goes invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are set up (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/ $\overline{MCK}$ referenced measurements are made from the crossing of the two signals $\pm 0.1 \text{ V}$.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/ $\overline{MCK}$, $\overline{MCS}$, and MDQ/MECC/MDM/MDQS. For the ADDR/CMD setup and hold specifications, it is assumed that the clock control register is set to adjust the memory clocks by 1/2 applied cycle.
4. t_{DDKHHM} follows the symbol conventions described in note 1. For example, t_{DDKHHM} describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). t_{DDKHHM} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register and is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters are set to the same adjustment value. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK(n) at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

Figure 6 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHHM}).

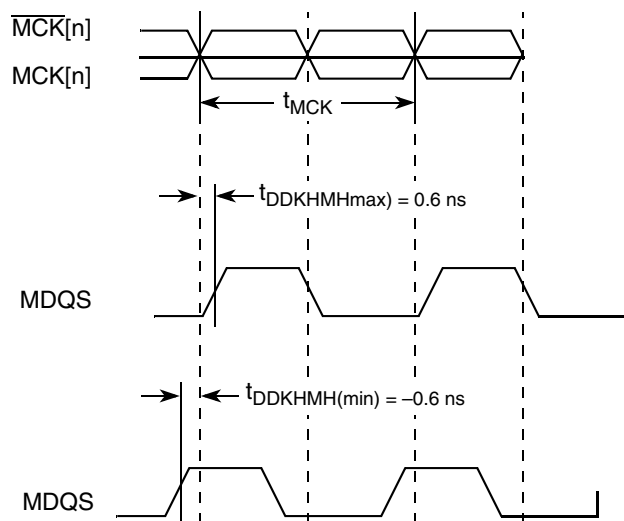
**Figure 6. Timing Diagram for t_{DDKHHM}**

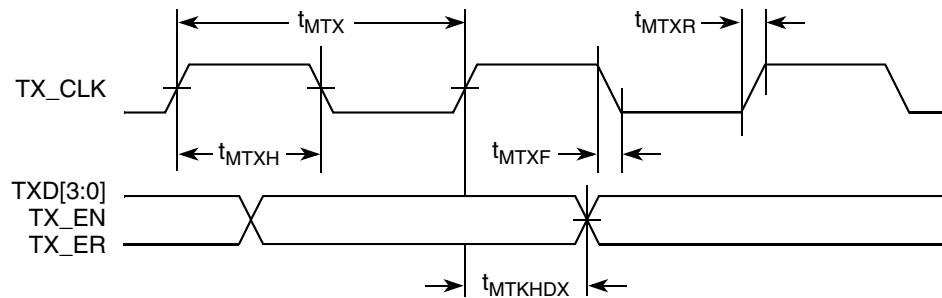
Table 27. MII Transmit AC Timing Specifications (continued)At recommended operating conditions with V_{DD}/OV_{DD} of 3.3 V $\pm$ 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 11 shows the MII transmit AC timing diagram.

**Figure 11. MII Transmit AC Timing Diagram**

8.2.2.2 MII Receive AC Timing Specifications

Table 28 provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing SpecificationsAt recommended operating conditions with V_{DD}/OV_{DD} of 3.3 V $\pm$ 10%.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns

Figure 16 shows the RBMII and RTBI AC timing and multiplexing diagrams.

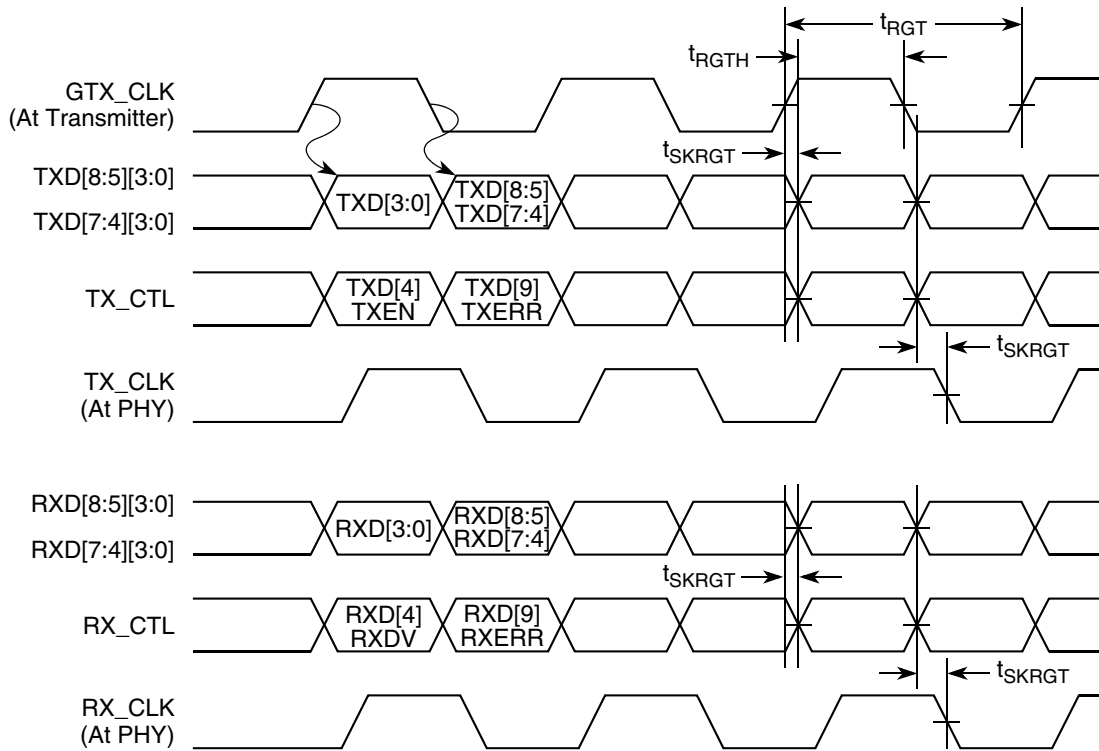


Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in [Section 8.1, “Three-Speed Ethernet Controller \(TSEC\)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics.”](#)

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in [Table 32](#) and [Table 33](#).

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (2.5 V)	V_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$V_{DD} = \text{Min}$	2.00	$V_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$V_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$V_{DD} = \text{Min}$	1.7	—	V
Input low voltage	V_{IL}	—	$V_{DD} = \text{Min}$	-0.3	0.70	V

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8349EA.

9.1 USB DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the USB interface.

Table 35. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 36 describes the general timing parameters of the USB interface of the MPC8349EA.

Table 36. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol ¹	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	$t_{USKH OV}$	—	7	ns	2–5
Output hold from USB clock—all outputs	$t_{USKH OX}$	2	—	ns	2–5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, $t_{USKH OX}$ symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

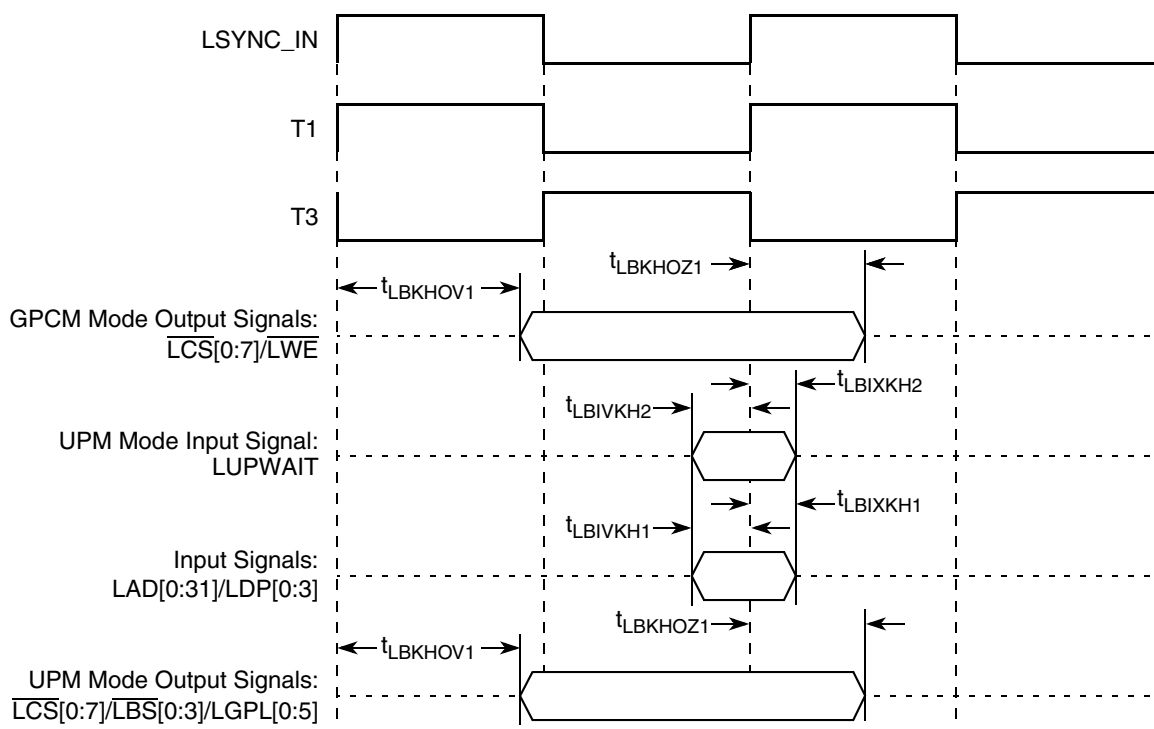


Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)

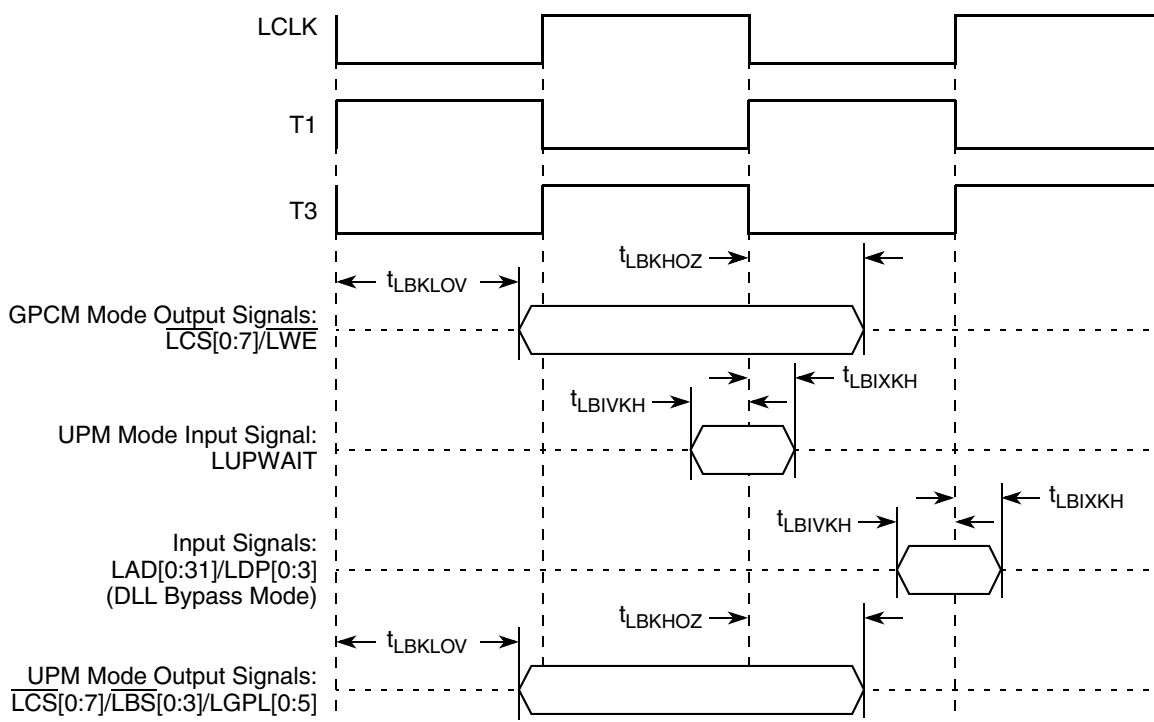


Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Table 43. I²C AC Electrical Specifications (continued)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t_{I2CF}	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μ s
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μ s
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	$0.2 \times OV_{DD}$	—	V

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The device provides a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. C_B = capacitance of one bus line in pF.
- 5.)The device does not follow the "I²C-BUS Specifications" version 2.1 regarding the t_{I2CF} AC parameter.

Figure 32 provides the AC test load for the I²C.

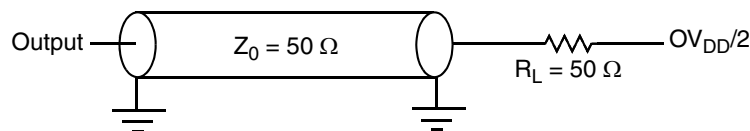
Figure 32. I²C AC Test Load

Figure 33 shows the AC timing diagram for the I²C bus.

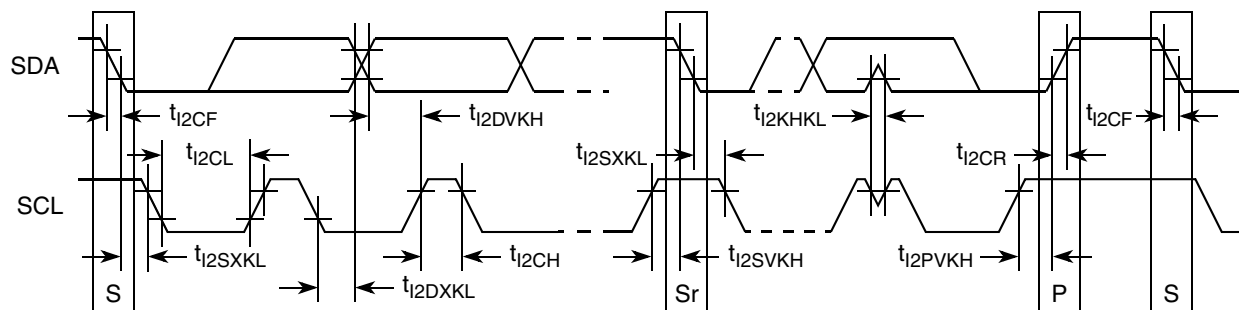
Figure 33. I²C Bus AC Timing Diagram

Table 47. Timer DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8349EA GPIO.

Table 49. GPIO DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0 \text{ mA}$	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0 \text{ mA}$	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	—	0.4	V

18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is 35 mm × 35 mm, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

18.3 Pinout Listings

Table 55 provides the pin-out listing for the MPC8349EA, 672 TBGA package.

Table 55. MPC8349EA (TBGA) Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI1 and PCI2 (One 64-Bit or Two 32-Bit)				
PCI1_INTA/IRQ_OUT	B34	O	OV _{DD}	2
PCI1_RESET_OUT	C33	O	OV _{DD}	—
PCI1_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV _{DD}	—
PCI1_C/ $\overline{\text{BE}}$ [3:0]	J30, M31, P33, T34	I/O	OV _{DD}	—
PCI1_PAR	P32	I/O	OV _{DD}	—
PCI1_FRAME	M32	I/O	OV _{DD}	5
PCI1_TRDY	N29	I/O	OV _{DD}	5
PCI1_IRDY	M34	I/O	OV _{DD}	5
PCI1_STOP	N31	I/O	OV _{DD}	5
PCI1_DEVSEL	N30	I/O	OV _{DD}	5
PCI1_IDSEL	J31	I	OV _{DD}	—
PCI1_SERR	N34	I/O	OV _{DD}	5
PCI1_PERR	N33	I/O	OV _{DD}	5
PCI1_REQ[0]	D32	I/O	OV _{DD}	—
PCI1_REQ[1]/CPCI1_HS_ES	D34	I	OV _{DD}	—
PCI1_REQ[2:4]	E34, F32, G29	I	OV _{DD}	—
PCI1_GNT0	C34	I/O	OV _{DD}	—
PCI1_GNT1/CPCI1_HS_LED	D33	O	OV _{DD}	—
PCI1_GNT2/CPCI1_HS_ENUM	E33	O	OV _{DD}	—
PCI1_GNT[3:4]	F31, F33	O	OV _{DD}	—
PCI2_RESET_OUT/GPIO2[0]	W32	I/O	OV _{DD}	—
PCI2_AD[31:0]/PCI1[63:32]	AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30	I/O	OV _{DD}	—
PCI2_C/ $\overline{\text{BE}}$ [3:0]/PCI1_C/ $\overline{\text{BE}}$ [7:4]	AC32, AE32, AH31, AL32	I/O	OV _{DD}	—
PCI2_PAR/PCI1_PAR64	AG34	I/O	OV _{DD}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
PCI2_FRAME/GPIO2[1]	AE33	I/O	OV _{DD}	5
PCI2_TRDY/GPIO2[2]	AF32	I/O	OV _{DD}	5
PCI2_IRDY/GPIO2[3]	AE34	I/O	OV _{DD}	5
PCI2_STOP/GPIO2[4]	AF34	I/O	OV _{DD}	5
PCI2_DEVSEL/GPIO2[5]	AF33	I/O	OV _{DD}	5
PCI2_SERR/PCI1_ACK64	AG33	I/O	OV _{DD}	5
PCI2_PERR/PCI1_REQ64	AG32	I/O	OV _{DD}	5
PCI2_REQ[0:2]/GPIO2[6:8]	Y32, Y34, AA32	I/O	OV _{DD}	—
PCI2_GNT[0:2]/GPIO2[9:11]	Y31, Y33, AA31	I/O	OV _{DD}	—
M66EN	A19	I	OV _{DD}	—
DDR SDRAM Memory Interface				
MDQ[0:63]	D5, A3, C3, D3, C4, B3, C2, D4, D2, E5, G2, H6, E4, F3, G4, G3, H1, J2, L6, M6, H2, K6, L2, M4, N2, P4, R2, T4, P6, P3, R1, T2, AB5, AA3, AD6, AE4, AB4, AC2, AD3, AE6, AE3, AG4, AK5, AK4, AE2, AG6, AK3, AK2, AL2, AL1, AM5, AP5, AM2, AN1, AP4, AN5, AJ7, AN7, AM8, AJ9, AP6, AL7, AL9, AN8	I/O	GV _{DD}	—
MECC[0:4]/MSRCID[0:4]	W4, W3, Y3, AA6, T1	I/O	GV _{DD}	—
MECC[5]/MDVAL	U1	I/O	GV _{DD}	—
MECC[6:7]	Y1, Y6	I/O	GV _{DD}	—
MDM[0:8]	B1, F1, K1, R4, AD4, AJ1, AP3, AP7, Y4	O	GV _{DD}	—
MDQS[0:8]	B2, F5, J1, P2, AC1, AJ2, AN4, AL8, W2	I/O	GV _{DD}	—
MBA[0:1]	AD1, AA5	O	GV _{DD}	—
MA[0:14]	W1, U4, T3, R3, P1, M1, N1, L3, L1, K2, Y2, K3, J3, AP2, AN6	O	GV _{DD}	—
MWE	AF1	O	GV _{DD}	—
MRAS	AF4	O	GV _{DD}	—
MCAS	AG3	O	GV _{DD}	—
MCS[0:3]	AG2, AG1, AK1, AL4	O	GV _{DD}	—
MCKE[0:1]	H3, G1	O	GV _{DD}	3
MCK[0:5]	U2, F4, AM3, V3, F2, AN3	O	GV _{DD}	—
MCK[0:5]	U3, E3, AN2, V4, E1, AM4	O	GV _{DD}	—
MODT[0:3]	AH3, AJ5, AH1, AJ4	O	GV _{DD}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MBA[2]	H4	O	GV _{DD}	—
MDIC0	AB1	I/O	—	9
MDIC1	AA1	I/O	—	9
Local Bus Controller Interface				
LAD[0:31]	AM13, AP13, AL14, AM14, AN14, AP14, AK15, AJ15, AM15, AN15, AP15, AM16, AL16, AN16, AP16, AL17, AM17, AP17, AK17, AP18, AL18, AM18, AN18, AP19, AN19, AM19, AP20, AK19, AN20, AL20, AP21, AN21	I/O	OV _{DD}	—
LDP[0]/CKSTOP_OUT	AM21	I/O	OV _{DD}	—
LDP[1]/CKSTOP_IN	AP22	I/O	OV _{DD}	—
LDP[2]/LCS[4]	AN22	I/O	OV _{DD}	—
LDP[3]/LCS[5]	AM22	I/O	OV _{DD}	—
LA[27:31]	AK21, AP23, AN23, AP24, AK22	O	OV _{DD}	—
LCS[0:3]	AN24, AL23, AP25, AN25	O	OV _{DD}	—
LWE[0:3]/LSDDQM[0:3]/LBS[0:3]	AK23, AP26, AL24, AM25	O	OV _{DD}	—
LBCTL	AN26	O	OV _{DD}	—
LALE	AK24	O	OV _{DD}	—
LGPL0/LSDA10/cfg_reset_source0	AP27	I/O	OV _{DD}	—
LGPL1/LSDWE/cfg_reset_source1	AL25	I/O	OV _{DD}	—
LGPL2/LSDRAS/LOE	AJ24	O	OV _{DD}	—
LGPL3/LSDCAS/cfg_reset_source2	AN27	I/O	OV _{DD}	—
LGPL4/LGT/LUPWAIT/LPBSE	AP28	I/O	OV _{DD}	12
LGPL5/cfg_clkin_div	AL26	I/O	OV _{DD}	—
LCKE	AM27	O	OV _{DD}	—
LCLK[0:2]	AN28, AK26, AP29	O	OV _{DD}	—
LSYNC_OUT	AM12	O	OV _{DD}	—
LSYNC_IN	AJ10	I	OV _{DD}	—
General Purpose I/O Timers				
GPIO1[0]/DMA_DREQ0/GTM1_TIN1/GTM2_TIN2	F24	I/O	OV _{DD}	—
GPIO1[1]/DMA_DACK0/GTM1_TGATE1/GTM2_TGATE2	E24	I/O	OV _{DD}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Gigabit Reference Clock				
EC_GTX_CLK125	C8	I	LV _{DD1}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	A17	I/O	OV _{DD}	—
TSEC1_CRS/GPIO2[21]	F12	I/O	LV _{DD1}	—
TSEC1_GTX_CLK	D10	O	LV _{DD1}	3
TSEC1_RX_CLK	A11	I	LV _{DD1}	—
TSEC1_RX_DV	B11	I	LV _{DD1}	—
TSEC1_RX_ER/GPIO2[26]	B17	I/O	OV _{DD}	—
TSEC1_RXD[7:4]/GPIO2[22:25]	B16, D16, E16, F16	I/O	OV _{DD}	—
TSEC1_RXD[3:0]	E10, A8, F10, B8	I	LV _{DD1}	—
TSEC1_TX_CLK	D17	I	OV _{DD}	—
TSEC1_TXD[7:4]/GPIO2[27:30]	A15, B15, A14, B14	I/O	OV _{DD}	—
TSEC1_TXD[3:0]	A10, E11, B10, A9	O	LV _{DD1}	10
TSEC1_TX_EN	B9	O	LV _{DD1}	—
TSEC1_TX_ER/GPIO2[31]	A16	I/O	OV _{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	C14	I/O	OV _{DD}	—
TSEC2_CRS/GPIO1[22]	D6	I/O	LV _{DD2}	—
TSEC2_GTX_CLK	A4	O	LV _{DD2}	—
TSEC2_RX_CLK	B4	I	LV _{DD2}	—
TSEC2_RX_DV/GPIO1[23]	E6	I/O	LV _{DD2}	—
TSEC2_RXD[7:4]/GPIO1[26:29]	A13, B13, C13, A12	I/O	OV _{DD}	—
TSEC2_RXD[3:0]/GPIO1[13:16]	D7, A6, E8, B7	I/O	LV _{DD2}	—
TSEC2_RX_ER/GPIO1[25]	D14	I/O	OV _{DD}	—
TSEC2_TXD[7]/GPIO1[31]	B12	I/O	OV _{DD}	—
TSEC2_TXD[6]/ DR_XCVR_TERM_SEL	C12	O	OV _{DD}	—
TSEC2_TXD[5]/ DR_UTMI_OPMODE1	D12	O	OV _{DD}	—
TSEC2_TXD[4]/ DR_UTMI_OPMODE0	E12	O	OV _{DD}	—
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV _{DD2}	—

Table 57 provides the operating frequencies for the MPC8349EA TBGA under recommended operating conditions (see Table 2).

Table 57. Operating Frequencies for TBGA

Characteristic ¹	400 MHz	533 MHz	667 MHz	Unit
e300 core frequency (<i>core_clk</i>)	266–400	266–533	266–667	MHz
Coherent system bus frequency (<i>csb_clk</i>)	100–266	100–333	100–333	MHz
DDR1 memory bus frequency (MCK) ²	100–133	100–133	100–166.67	MHz
DDR2 memory bus frequency (MCK) ³	100–133	100–133	100–200	MHz
Local bus frequency (LCLK _n) ⁴	16.67–133	16.67–133	16.67–133	MHz
PCI input frequency (CLKIN or PCI_CLK)	25–66	25–66	25–66	MHz
Security core maximum internal operating frequency	133	133	166	MHz
USB_DR, USB_MPH maximum internal operating frequency	133	133	166	MHz

¹ The CLKIN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen so that the resulting *csb_clk*, MCK, LCLK[0:2], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies. The value of SCCR[ENCCM], SCCR[USBDRCM] and SCCR[USBMPPHCM] must be programmed so that the maximum internal operating frequency of the security core and USB modules does not exceed the respective values listed in this table.

² The DDR data rate is 2x the DDR memory bus frequency.

³ The DDR data rate is 2x the DDR memory bus frequency.

⁴ The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCCR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBIUCM]).

All frequency combinations shown in the table below may not be available. Maximum operating frequencies depend on the part ordered, see Section 22.1, “Part Numbers Fully Addressed by This Document,” for part ordering details and contact your Freescale Sales Representative or authorized distributor for more information.

19.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 58 shows the multiplication factor encodings for the system PLL.

Table 58. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	× 16
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110	× 6

Table 59. CSB Frequency Options for Host Mode (continued)

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk : Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0110	6 : 1	100	150	200	
Low	0111	7 : 1	116	175	233	
Low	1000	8 : 1	133	200	266	
Low	1001	9 : 1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2 : 1				133
High	0011	3 : 1			100	200
High	0100	4 : 1			133	266
High	0101	5 : 1			166	333
High	0110	6 : 1			200	
High	0111	7 : 1			233	
High	1000	8 : 1				

¹ CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 60. CSB Frequency Options for Agent Mode

CFG_CLKIN_DIV at Reset ¹	SPMF	csb_clk : Input Clock Ratio ²	Input Clock Frequency (MHz) ²			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1				100
Low	0100	4 : 1				133
Low	0101	5 : 1				166
Low	0110	6 : 1				200
Low	0111	7 : 1				233
Low	1000	8 : 1				266
Low	1001	9 : 1				300
Low	1010	10 : 1				333
Low	1011	11 : 1				366
Low	1100	12 : 1				400
Low	1101	13 : 1				433
Low	1110	14 : 1				466
Low	1111	15 : 1				500
Low	0000	16 : 1				533

Table 63. Package Thermal Characteristics for TBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See [Table 5](#) for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J , can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

Heat sink vendors include the following list:

Aavid Thermalloy 80 Commercial St. Concord, NH 03301 Internet: www.aavidthermalloy.com	603-224-9988
Alpha Novatech 473 Sapena Ct. #12 Santa Clara, CA 95054 Internet: www.alphanovatech.com	408-567-8082
International Electronic Research Corporation (IERC) 413 North Moss St. Burbank, CA 91502 Internet: www.ctscorp.com	818-842-7277
Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105-3668 Internet: www.chipcoolers.com	800-522-2800
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-5102

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Dow-Corning Electronic Materials P.O. Box 994 Midland, MI 48686-0997 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674

The Bergquist Company
 18930 West 78th St.
 Chanhassen, MN 55317
 Internet: www.bergquistcompany.com

800-347-4572

20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8349EA.

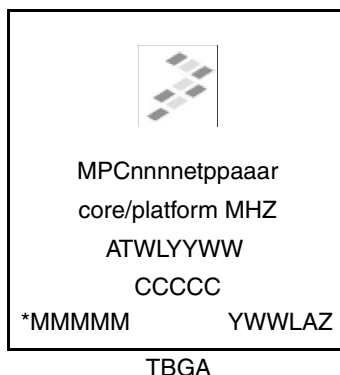
21.1 System Clocking

The MPC8349EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in [Section 19.1, “System PLL Configuration.”](#)

22.2 Part Marking

Parts are marked as in the example shown in [Figure 44](#).



Notes:

ATWLYYWW is the traceability code.

CCCCC is the country code.

MMMMM is the mask number.

YWWLAZ is the assembly traceability code.

Figure 44. Freescale Part Marking for TBGA Devices

23 Document Revision History

This table provides a revision history of this document.

Table 68. Document Revision History

Rev. Number	Date	Substantive Change(s)
13	09/2011	- In Section 2.2, "Power Sequencing," added Section 2.2.1, "Power-Up Sequencing" and Figure 4. - In Table 25, Table 29 and Table 31, removed the GTX_CLK125. - In Table 34, updated t_{MDKHDX} Max value from 170ns to 70ns.
12	11/2010	- In Table 55 added note for pin LGPL4. - In Section 21.7, "Pull-Up Resistor Requirements, updated the list of open drain type pins.
11	05/2010	- In Table 25 through Table 30, changed $V_{IL}(\min)$ to $V_{IH}(\max)$ to (20%–80%). - Added Table 8, "EC_GTX_CLK125 AC Timing Specifications."
10	5/2009	- In Table 57, updated frequency for max csb_clk to 333 MHz and DDR2, from 100-200 to 100-133 at core frequency = 533MHz. - In Section 18.1, "Package Parameters for the MPC8349EA TBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. - In Table 66, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.