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#### Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

E·XE

Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8349ecvvajfb

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

# 1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8349EA.



Figure 1. MPC8349EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.



Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

## 2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV <sub>DD</sub> = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV <sub>DD</sub> = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV <sub>DD</sub> = 1.8 V
TSEC/10/100 signals	40	LV <sub>DD</sub> = 2.5/3.3 V
DUART, system control, I <sup>2</sup> C, JTAG, USB	40	OV <sub>DD</sub> = 3.3 V
GPIO signals	40	OV <sub>DD</sub> = 3.3 V, LV <sub>DD</sub> = 2.5/3.3 V

Table 3. Output Drive Capability

# 2.2 **Power Sequencing**

This section details the power sequencing considerations for the MPC8349EA.

### 2.2.1 Power-Up Sequencing

MPC8349EA does not require the core supply voltage ( $V_{DD}$  and  $AV_{DD}$ ) and I/O supply voltages ( $GV_{DD}$ ,  $LV_{DD}$ , and  $OV_{DD}$ ) to be applied in any particular order. During the power ramp up, before the power

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

# 4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI\_SYNC\_IN) DC timing specifications for the MPC8349EA.

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	_	V <sub>IH</sub>	2.7	OV <sub>DD</sub> + 0.3	V
Input low voltage	_	V <sub>IL</sub>	-0.3	0.4	V
CLKIN input current	$0~V \leq V_{IN} \leq OV_{DD}$	I <sub>IN</sub>	—	±10	μA
PCI_SYNC_IN input current	$\begin{array}{c} 0 \text{ V} \leq \text{V}_{\text{IN}} \leq 0.5 \text{ V or} \\ \text{OV}_{\text{DD}} - 0.5 \text{ V} \leq \text{V}_{\text{IN}} \leq \text{OV}_{\text{DD}} \end{array}$	I <sub>IN</sub>	_	±10	μA
PCI_SYNC_IN input current	$0.5~V \leq V_{IN} \leq OV_{DD} - 0.5~V$	I <sub>IN</sub>	—	±50	μA

Table 6. CLKIN DC Timing Specifications

# 4.2 AC Electrical Characteristics

The primary clock source for the MPC8349EA can be one of two inputs, CLKIN or PCI\_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI\_CLK) AC timing specifications for the device.

**Table 7. CLKIN AC Timing Specifications** 

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f <sub>CLKIN</sub>	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t <sub>CLKIN</sub>	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t <sub>KHK</sub> /t <sub>CLKIN</sub>	40	—	60	%	3
CLKIN/PCI_CLK jitter	_	—	—	±150	ps	4, 5

Notes:

1. Caution: The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.

- 2. Rise and fall times for CLKIN/PCI\_CLK are measured at 0.4 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The CLKIN/PCI\_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
- 6. Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 50 KHz modulation rate regardless of input frequency.

**RESET Initialization** 

# 4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC\_GTX\_CLK125) AC timing specifications.

### Table 8. EC\_GTX\_CLK125 AC Timing Specifications

At recommended operating conditions with LV  $_{DD}$  = 2.5  $\pm$  0.125 mV/ 3.3 V  $\pm$  165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t <sub>G125</sub>	—	125		MHz	
EC_GTX_CLK125 cycle time	t <sub>G125</sub>	—	8	_	ns	_
EC_GTX_CLK125 rise and fall time $LV_{DD} = 2.5 V$ $LV_{DD} = 3.3 V$	t <sub>G125R</sub> /t <sub>G125F</sub>			0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t <sub>G125H</sub> /t <sub>G125</sub>	45 47	_	55 53	%	2
EC_GTX_CLK125 jitter	_	—	—	±150	ps	2

#### Notes:

1. Rise and fall times for EC\_GTX\_CLK125 are measured from 0.5 and 2.0 V for  $LV_{DD}$  = 2.5 V and from 0.6 and 2.7 V for  $LV_{DD}$  = 3.3 V.

2. EC\_GTX\_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC\_GTX\_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX\_CLK. See Section 8.2.4, "RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

# 5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8349EA.

# 5.1 **RESET DC Electrical Characteristics**

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8349EA.

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	_	±5	μA
Output high voltage <sup>2</sup>	V <sub>OH</sub>	I <sub>OH</sub> = -8.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	—	0.5	V

Table 9. RESET Pins DC Electrical Characteristics<sup>1</sup>

Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times	-	100	μs	_
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb\_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb\_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

# 6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8349EA. Note that DDR SDRAM is  $GV_{DD}(typ) = 2.5$  V and DDR2 SDRAM is  $GV_{DD}(typ) = 1.8$  V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

### NOTE

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

# 6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8349EA when  $GV_{DD}(typ) = 1.8 \text{ V}.$ 

Table 12	. DDR2	SDRAM D	C Electrica	I Characteristics	for GV <sub>DD</sub> (typ	) = 1.8 V
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Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV <sub>DD</sub>	1.71	1.89	V	1
I/O reference voltage	MV <sub>REF</sub>	$0.49\times GV_{DD}$	$0.51  imes GV_{DD}$	V	2
I/O termination voltage	V <sub>TT</sub>	MV <sub>REF</sub> – 0.04	MV <sub>REF</sub> + 0.04	V	3
Input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.125	GV <sub>DD</sub> + 0.3	V	—
Input low voltage	V <sub>IL</sub>	-0.3	MV <sub>REF</sub> – 0.125	V	—
Output leakage current	I <sub>OZ</sub>	-9.9	9.9	μA	4
Output high current (V <sub>OUT</sub> = 1.420 V)	I <sub>OH</sub>	-13.4	_	mA	—

#### DDR and DDR2 SDRAM

### Table 12. DDR2 SDRAM DC Electrical Characteristics for GV<sub>DD</sub>(typ) = 1.8 V (continued)

Output low current (V <sub>OUT</sub> = 0.280 V)	I <sub>OL</sub>	13.4	_	mA	_

Notes:

1.  $GV_{DD}$  is expected to be within 50 mV of the DRAM  $GV_{DD}$  at all times.

2.  $MV_{REF}$  is expected to equal 0.5 ×  $GV_{DD}$ , and to track  $GV_{DD}$  DC variations as measured at the receiver. Peak-to-peak noise on  $MV_{REF}$  cannot exceed ±2% of the DC value.

 V<sub>TT</sub> is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to equal MV<sub>REF</sub>. This rail should track variations in the DC level of MV<sub>REF</sub>.

4. Output leakage is measured with all outputs disabled, 0 V  $\leq$  V<sub>OUT</sub>  $\leq$  GV<sub>DD</sub>.

Table 13 provides the DDR2 capacitance when  $GV_{DD}(typ) = 1.8$  V.

#### Table 13. DDR2 SDRAM Capacitance for GV<sub>DD</sub>(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
Input/output capacitance: DQ, DQS, DQS	C <sub>IO</sub>	6	8	pF	1
Delta input/output capacitance: DQ, DQS, DQS	C <sub>DIO</sub>	_	0.5	pF	1

Note:

1. This parameter is sampled.  $GV_{DD} = 1.8 \text{ V} \pm 0.090 \text{ V}$ , f = 1 MHz, T<sub>A</sub> = 25°C, V<sub>OUT</sub> =  $GV_{DD}/2$ , V<sub>OUT</sub> (peak-to-peak) = 0.2 V.

Table 14 provides the recommended operating conditions for the DDR SDRAM component(s) when  $GV_{DD}(typ) = 2.5 \text{ V}.$ 

#### Table 14. DDR SDRAM DC Electrical Characteristics for GV<sub>DD</sub>(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Мах	Unit	Notes
I/O supply voltage	GV <sub>DD</sub>	2.375	2.625	V	1
I/O reference voltage	MV <sub>REF</sub>	$0.49  imes GV_{DD}$	$0.51  imes GV_{DD}$	V	2
I/O termination voltage	V <sub>TT</sub>	MV <sub>REF</sub> – 0.04	MV <sub>REF</sub> + 0.04	V	3
Input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.18	GV <sub>DD</sub> + 0.3	V	—
Input low voltage	V <sub>IL</sub>	-0.3	MV <sub>REF</sub> – 0.18	V	—
Output leakage current	I <sub>OZ</sub>	-9.9	-9.9	μA	4
Output high current (V <sub>OUT</sub> = 1.95 V)	I <sub>ОН</sub>	-15.2	—	mA	—
Output low current (V <sub>OUT</sub> = 0.35 V)	I <sub>OL</sub>	15.2	—	mA	—

Notes:

1.  $GV_{DD}$  is expected to be within 50 mV of the DRAM  $GV_{DD}$  at all times.

2. MV<sub>REF</sub> is expected to be equal to 0.5 × GV<sub>DD</sub>, and to track GV<sub>DD</sub> DC variations as measured at the receiver. Peak-to-peak noise on MV<sub>REF</sub> may not exceed ±2% of the DC value.

3. V<sub>TT</sub> is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV<sub>REF</sub>. This rail should track variations in the DC level of MV<sub>REF</sub>.

4. Output leakage is measured with all outputs disabled, 0 V  $\leq$  V<sub>OUT</sub>  $\leq$  GV<sub>DD</sub>.

Table 15 provides the DDR capacitance when  $GV_{DD}(typ) = 2.5$  V.

Table 15. DDR SDRAM Capacitance for GV<sub>DD</sub>(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C <sub>IO</sub>	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C <sub>DIO</sub>	_	0.5	pF	1

Note:

1. This parameter is sampled.  $GV_{DD} = 2.5 V \pm 0.125 V$ , f = 1 MHz,  $T_A = 25^{\circ}C$ ,  $V_{OUT} = GV_{DD}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2 V.

### Table 16 provides the current draw characteristics for MV<sub>REF</sub>.

Table 16. Current Draw Characteristics for MV<sub>REF</sub>

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV <sub>REF</sub>	I <sub>MVREF</sub>		500	μA	1

#### Note:

1. The voltage regulator for  $\text{MV}_{\text{REF}}$  must supply up to 500  $\mu\text{A}$  current.

# 6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

# 6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when  $GV_{DD}(typ) = 1.8 \text{ V}$ .

### Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with  $GV_{DD}$  of 1.8 ± 5%.

Parameter	Symbol	Min	Min Max		Notes
AC input low voltage	V <sub>IL</sub>	_	MV <sub>REF</sub> – 0.25	V	_
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.25	—	V	_

Table 18 provides the input AC timing specifications for the DDR SDRAM when  $GV_{DD}(typ) = 2.5 \text{ V}$ .

### Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with  $GV_{DD}$  of 2.5 ± 5%.

Parameter	Symbol	Min	Мах		Notes
AC input low voltage	V <sub>IL</sub>	—	MV <sub>REF</sub> – 0.31	V	—
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.31	—	V	—

#### DDR and DDR2 SDRAM

### Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

#### Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with  $GV_{DD}$  of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t <sub>CISKEW</sub>			ps	1, 2
400 MHz		-600	600		3
333 MHz		-750	750		—
266 MHz		-750	750		—
200 MHz		-750	750		—

Notes:

1. t<sub>CISKEW</sub> represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t<sub>DISKEW</sub>. This can be determined by the equation: t<sub>DISKEW</sub> = ± (T/4 – abs (t<sub>CISKEW</sub>)); where T is the clock period and abs (t<sub>CISKEW</sub>) is the absolute value of t<sub>CISKEW</sub>.
- 3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t<sub>DISKEW</sub> timing parameter.



Figure 5. DDR Input Timing Diagram

Parameter	Symbol	Min	Мах	Unit
High-level output voltage, $I_{OH} = -100 \ \mu A$	V <sub>OH</sub>	OV <sub>DD</sub> - 0.2	-	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V <sub>OL</sub>	—	0.2	V

# 7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16		2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8<sup>th</sup> sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16<sup>th</sup> sample.

# 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

# 8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

# 8.2.1.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

### Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
GTX_CLK clock period	t <sub>GTX</sub>	—	8.0	—	ns
GTX_CLK duty cycle	t <sub>GTXH</sub> /t <sub>GTX</sub>	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	<sup>t</sup> GTKHDX	0.5	—	5.0	ns
GTX_CLK clock rise time (20%-80%)	t <sub>GTXR</sub>	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t <sub>GTXF</sub>		_	1.0	ns

#### Notes:

1. The symbols for timing specifications follow the pattern t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>GTKHDV</sub> symbolizes GMII transmit timing (GT) with respect to the t<sub>GTX</sub> clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t<sub>GTKHDX</sub> symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the clock reference (K) going to the high state (H) relative to the time date input signals (D) with respect to the t<sub>GTX</sub> clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t<sub>GTX</sub> represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

### Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

## 8.2.1.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

### Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV\_DD/OV\_DD of 3.3 V  $\pm$  10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
RX_CLK clock period	t <sub>GRX</sub>	_	8.0	_	ns
RX_CLK duty cycle	t <sub>GRXH</sub> /t <sub>GRX</sub>	40	_	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t <sub>GRDVKH</sub>	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t <sub>GRDXKH</sub>	0.5	_	_	ns

#### Ethernet: Three-Speed Ethernet, MII Management

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V	(continued)
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Parameter	Symbol	Conditions	Min	Мах	Unit
Input high current	I <sub>IH</sub>	$V_{IN}^{1} = LV_{DD}$	-	10	μA
Input low current	IIL	$V_{IN} = LV_{DD}$	-15	_	μA

Note:

1. The symbol  $V_{IN}$ , in this case, represents the  $LV_{IN}$  symbol referenced in Table 1 and Table 2.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (3.3 V)	LV <sub>DD</sub>	—		2.97	3.63	V
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	$LV_{DD} = Min$	2.10	LV <sub>DD</sub> + 0.3	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 1.0 mA	$LV_{DD} = Min$	GND	0.50	V
Input high voltage	V <sub>IH</sub>	—		2.00	—	V
Input low voltage	V <sub>IL</sub>	—		-	0.80	V
Input high current	I <sub>IH</sub>	$LV_{DD} = Max$ $V_{IN}^1 = 2.1 V$		_	40	μA
Input low current	۱ <sub>IL</sub>	$LV_{DD} = Max$ $V_{IN} = 0.5 V$		-600	—	μA

Note:

1. The symbol  $V_{IN}$ , in this case, represents the LV<sub>IN</sub> symbol referenced in Table 1 and Table 2.

# 8.3.2 MII Management AC Electrical Specifications

Table 34 provides the MII management AC timing specifications.

### Table 34. MII Management AC Timing Specifications

At recommended operating conditions with  $LV_{DD}$  is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit	Notes
MDC frequency	f <sub>MDC</sub>	_	2.5		MHz	2
MDC period	t <sub>MDC</sub>		400		ns	_
MDC clock pulse width high	t <sub>MDCH</sub>	32	—	_	ns	—
MDC to MDIO delay	t <sub>MDKHDX</sub>	10	—	70	ns	3
MDIO to MDC setup time	t <sub>MDDVKH</sub>	5	—	_	ns	—
MDIO to MDC hold time	t <sub>MDDXKH</sub>	0	—	_	ns	—
MDC rise time	t <sub>MDCR</sub>	_		10	ns	

Figure 34 provides the AC test load for PCI.



Figure 34. PCI AC Test Load

Figure 35 shows the PCI input AC timing diagram.



Figure 35. PCI Input AC Timing Diagram

Figure 36 shows the PCI output AC timing diagram.



# 14 Timers

This section describes the DC and AC electrical specifications for the timers.

# 14.1 Timer DC Electrical Characteristics

Table 47 provides the DC electrical characteristics for the MPC8349EA timer pins, including TIN, TOUT, TGATE, and RTC\_CLK.

**Table 47. Timer DC Electrical Characteristics** 

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	_	±5	μA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8.0 mA	2.4	—	V

Table 47. Timer DC Electrical C	Characteristics (continued)
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Parameter	Symbol	Condition	Min	Мах	Unit
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	_	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	_	0.4	V

# 14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

### Table 48. Timers Input AC Timing Specifications<sup>1</sup>

Parameter	Symbol <sup>2</sup>	Min	Unit
Timers inputs—minimum pulse width	t <sub>TIWID</sub>	20	ns

#### Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t<sub>TIWID</sub> ns to ensure proper operation.

# 15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

# **15.1 GPIO DC Electrical Characteristics**

Table 49 provides the DC electrical characteristics for the MPC8349EA GPIO.

Table 49. GPIO DC Electrical Characteristics

PArameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>	_	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	_	±5	μA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	_	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V

Package and Pin Listings

# 18.2 Mechanical Dimensions for the MPC8349EA TBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8349EA, 672-TBGA package.



#### Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement must exclude any effect of mark on top surface of package.

#### Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8349EA TBGA

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	_		_
GV <sub>DD</sub>	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV <sub>DD</sub>	_
LV <sub>DD1</sub>	C9, D11	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV <sub>DD1</sub>	_
LV <sub>DD2</sub>	C6, D9	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV <sub>DD2</sub>	_
V <sub>DD</sub>	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V <sub>DD</sub>	_
OV <sub>DD</sub>	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV <sub>DD</sub>	_
MVREF1	МЗ	I	DDR reference voltage	_

### Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

### Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF2	AD2	I	DDR reference voltage	_

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV<sub>DD</sub>.

2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV<sub>DD</sub>.

3. During reset, this output is actively driven rather than three-stated.

4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.

6. This pin must always be tied to GND.

7. This pin must always be left not connected.

8. Thermal sensitive resistor.

9. It is recommended that MDIC0 be tied to GND using an 18.2  $\Omega$  resistor and MDIC1 be tied to DDR power using an 18.2  $\Omega$  resistor.

10.TSEC1\_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

11. A weak pull-up resistor (2–10 k $\Omega$ ) should be placed on this pin to LV<sub>DD1</sub>.

12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

RCWL[SPMF]	System PLL Multiplication Factor
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

Table 58. System	n PLL Multi	plication	Factors	(continued)	)
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As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG\_CLKIN\_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI\_CLK) and the internal coherent system bus clock (*csb\_clk*). Table 59 and Table 60 show the expected frequency values for the CSB frequency for select *csb\_clk* to CLKIN/PCI\_SYNC\_IN ratios.

CFG_CLKIN_DIV at Reset <sup>1</sup>	SPMF	<i>csb_clk</i> : Input Clock Ratio <sup>2</sup>	Input Clock Frequency (MHz) <sup>2</sup>			
			16.67	25	33.33	66.67
			<i>csb_clk</i> Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333

Table 59. CSB Frequency Options for Host Mode

#### Thermal

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

 $T_J = T_A + (R_{\theta JA} \times P_D)$ 

where:

 $T_J$  = junction temperature (°C)

 $T_A$  = ambient temperature for the package (°C)

 $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

## 20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter ( $\Psi_{JT}$ ) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)

 $T_T$  = thermocouple temperature on top of package (°C)

 $\Psi_{JT}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

## 20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

#### System Design Information

2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, "Core PLL Configuration."

# 21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ( $AV_{DD}1$ ,  $AV_{DD}2$ , respectively). The  $AV_{DD}$  level should always equal to  $V_{DD}$ , and preferably these voltages are derived directly from  $V_{DD}$  through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four  $AV_{DD}$  pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific  $AV_{DD}$  pin being supplied. It should be possible to route directly from the capacitors to the  $AV_{DD}$  pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.



Figure 42. PLL Power Supply Filter Circuit

# 21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8349EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8349EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  pin of the device. These capacitors should receive their power from separate  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1  $\mu$ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the  $V_{DD}$ ,  $OV_{DD}$ ,  $GV_{DD}$ , and  $LV_{DD}$  planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330  $\mu$ F (AVX TPS tantalum or Sanyo OSCON).

# 21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to  $OV_{DD}$ ,  $GV_{DD}$ , or  $LV_{DD}$  as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external  $V_{DD}$ ,  $GV_{DD}$ ,  $LV_{DD}$ ,  $OV_{DD}$ , and GND pins of the MPC8349EA.

# 21.5 Output Buffer DC Impedance

The MPC8349EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for  $I^2C$ ).

To measure  $Z_0$  for the single-ended drivers, an external resistor is connected from the chip pad to  $OV_{DD}$  or GND. Then the value of each resistor is varied until the pad voltage is  $OV_{DD}/2$  (see Figure 43). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and  $R_P$  is trimmed until the voltage at the pad equals  $OV_{DD}/2$ .  $R_P$  then becomes the resistance of the pull-up devices.  $R_P$  and  $R_N$  are designed to be close to each other in value. Then,  $Z_0 = (R_P + R_N) \div 2$ .



Figure 43. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is  $V_1 = R_{source} \times I_{source}$ . Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value  $R_{term}$ . The measured voltage is