NXP USA Inc. - MPC8349ECZUAGDB Datasheet





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Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8349eczuagdb

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- Complies with USB specification Rev. 2.0
- Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints
- Can operate as a stand-alone USB host controller
 - USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
 - Can operate as a stand-alone USB host controller
 - USB root hub with one or two downstream-facing ports
 - Enhanced host controller interface (EHCI) compatible
 - Complies with USB Specification Rev. 2.0
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
 - Direct connection to a high-speed device without an external hub
 - External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects for eight external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
 - Three protocol engines on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user-programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
 - Programmable highest priority request
 - Four groups of interrupts with programmable priority
 - External and internal interrupts directed to host processor
 - Redirects interrupts to external INTA pin in core disable mode.
 - Unique vector number for each interrupt source

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table	1.	Absol	ute I	Maxim	um	Ratings	1
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Parameter			Max Value	Unit	Notes
Core supply voltage		V _{DD}	–0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	_
PLL supply voltage			V _{DD} -0.3 to 1.32 (1.36 max for 667-MHz core frequency)		—
DDR and DDR2 DRAM I/O voltage		GV _{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV _{DD}	-0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C , and JTAG I/O voltage		OV _{DD}	-0.3 to 3.63	V	_
Input voltage	DDR DRAM signals	MV _{IN}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV _{REF}	–0.3 to (GV _{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV _{IN}	–0.3 to (LV _{DD} + 0.3)	V	4, 5
Local bus, DUART, CLKIN, system control and power management, I ² C, and JTAG signals		OV _{IN}	-0.3 to (OV _{DD} + 0.3)	V	3, 5
	PCI	OV _{IN}	–0.3 to (OV _{DD} + 0.3)	V	6
Storage temperature r	ange	T _{STG}	-55 to 150	°C	_

Notes:

¹ Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

- ² Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- ³ **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- ⁴ **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
- ⁵ (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
- 6 OVIN on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

- ² Typical power is based on a voltage of V_{DD} = 1.2 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- ³ Thermal solutions may need to design to a value higher than typical power based on the end application, T_A target, and I/O power.
- ⁴ Maximum power is based on a voltage of V_{DD} = 1.2 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.
- ⁵ Typical power is based on a voltage of V_{DD} = 1.3 V, a junction temperature of T_J = 105°C, and a Dhrystone benchmark application.
- ⁶ Maximum power is based on a voltage of V_{DD} = 1.3 V, worst case process, a junction temperature of T_J = 105°C, and an artificial smoke test.

Table 5 shows the estimated typical I/O power dissipation for MPC8349EA.

Interface	Parameter	GV _{DD} (1.8 V)	GV _{DD} (2.5 V)	OV _{DD} (3.3 V)	LV _{DD} (3.3 V)	LV _{DD} (2.5 V)	Unit	Comments
DDR I/O	200 MHz, 32 bits	0.31	0.42				W	—
65% utilization 2.5 V	200 MHz, 64 bits	0.42	0.55				W	—
Rs = 20 Ω Bt = 50 Ω	266 MHz, 32 bits	0.35	0.5				W	—
2 pair of clocks	266 MHz, 64 bits	0.47	0.66				W	—
	300 MHz, 32 bits	0.37	0.54	_	_	_	W	—
	300 MHz, 64 bits	0.50	0.7	_	_	_	W	—
	333 MHz, 32 bits	0.39	0.58	_	_	_	W	—
	333 MHz, 64 bits	0.53	0.76	_	_	_	W	—
	400 MHz, 32 bits	0.44						—
	400 MHz, 64 bits	0.59	_	_		_	_	—
PCI I/O	33 MHz, 64 bits	_	_	0.08	_	_	W	—
10ad = 30 pF	66 MHz, 64 bits	_	_	0.14	_	_	W	—
	33 MHz, 32 bits	_	_	0.04	_	_	W	Multiply by 2 if using
	66 MHz, 32 bits	_	_	0.07	_	_	W	2 ports.
Local bus I/O	133 MHz, 32 bits	_	_	0.27	_	_	W	—
10ad = 25 pF	83 MHz, 32 bits	_	_	0.17	_	_	W	—
	66 MHz, 32 bits	_	_	0.14	_	_	W	—
	50 MHz, 32 bits	_	_	0.11	_	_	W	—
TSEC I/O	MII	_	_	_	0.01	_	W	Multiply by number of
load = 25 pF	GMII or TBI	_			0.06	_	W	interfaces used.
	RGMII or RTBI	_				0.04	W	
USB	12 MHz	_	_	0.01	_	_	W	Multiply by 2 if using
	480 MHz	_	_	0.2	_	_	W	2 ports.
Other I/O	—			0.01			W	—

Table 5. MPC8349EA Typical I/O Power Dissipation

4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI_SYNC_IN) DC timing specifications for the MPC8349EA.

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	_	V _{IH}	2.7	OV _{DD} + 0.3	V
Input low voltage	_	V _{IL}	-0.3	0.4	V
CLKIN input current	$0~V \leq V_{IN} \leq OV_{DD}$	I _{IN}	—	±10	μA
PCI_SYNC_IN input current	$\begin{array}{c} 0 \text{ V} \leq \text{V}_{\text{IN}} \leq 0.5 \text{ V or} \\ \text{OV}_{\text{DD}} - 0.5 \text{ V} \leq \text{V}_{\text{IN}} \leq \text{OV}_{\text{DD}} \end{array}$	I _{IN}	_	±10	μA
PCI_SYNC_IN input current	$0.5~V \leq V_{IN} \leq OV_{DD} - 0.5~V$	I _{IN}	—	±50	μA

Table 6. CLKIN DC Timing Specifications

4.2 AC Electrical Characteristics

The primary clock source for the MPC8349EA can be one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI_CLK) AC timing specifications for the device.

Table 7. CLKIN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f _{CLKIN}	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t _{CLKIN}	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t _{KH} , t _{KL}	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t _{KHK} /t _{CLKIN}	40	—	60	%	3
CLKIN/PCI_CLK jitter	_	—	—	±150	ps	4, 5

Notes:

1. Caution: The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.

- 2. Rise and fall times for CLKIN/PCI_CLK are measured at 0.4 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The CLKIN/PCI_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
- 6. Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 50 KHz modulation rate regardless of input frequency.

RESET Initialization

4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV $_{DD}$ = 2.5 \pm 0.125 mV/ 3.3 V \pm 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t _{G125}	—	125		MHz	
EC_GTX_CLK125 cycle time	t _{G125}	—	8	_	ns	_
EC_GTX_CLK125 rise and fall time $LV_{DD} = 2.5 V$ $LV_{DD} = 3.3 V$	t _{G125R} /t _{G125F}			0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t _{G125H} /t _{G125}	45 47	_	55 53	%	2
EC_GTX_CLK125 jitter	_	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.

2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, "RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

5 **RESET Initialization**

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8349EA.

5.1 **RESET DC Electrical Characteristics**

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8349EA.

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	_	±5	μA
Output high voltage ²	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V

Table 9. RESET Pins DC Electrical Characteristics¹

RESET Initialization

Table 9. RESET Pins DC Electrical Characteristics¹ (continued)

Parameter	Symbol	Condition	Min	Мах	Unit
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus V_{OH} is not relevant for those pins.

5.2 **RESET AC Electrical Characteristics**

Table 10 provides the reset initialization AC timing specifications of the MPC8349EA.

Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Natas
Parameter	IVIIII	max	Unit	notes
Required assertion time of HRESET or SRESET (input) to activate reset flow	32	_	t _{PCI_SYNC_IN}	1
Required assertion time of $\overrightarrow{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8349EA is in PCI host mode	32	—	t _{CLKIN}	2
Required assertion time of PORESET with stable clock applied to PCI_SYNC_IN when the MPC8349EA is in PCI agent mode	32	—	t _{PCI_SYNC_IN}	1
HRESET/SRESET assertion (output)	512	—	t _{PCI_SYNC_IN}	1
HRESET negation to SRESET negation (output)	16	—	t _{PCI_SYNC_IN}	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8349EA is in PCI host mode	4	_	t _{CLKIN}	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8349EA is in PCI agent mode	4	_	tpci_sync_in	1
Input hold time for POR configuration signals with respect to negation of HRESET	0	—	ns	—
Time for the MPC8349EA to turn off POR configuration signals with respect to the assertion of $\overrightarrow{\text{HRESET}}$	_	4	ns	3
Time for the MPC8349EA to turn on POR configuration signals with respect to the negation of HRESET	1	—	t _{PCI_SYNC_IN}	1, 3

Notes:

1. t_{PCI_SYNC_IN} is the clock period of the input clock applied to PCI_SYNC_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI_SYNC_IN period depends on the value of CFG_CLKIN_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

2. t_{CLKIN} is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual.

3. POR configuration signals consist of CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV.

Parameter	Symbol	Min	Мах	Unit
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	-	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16		2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

8.2.1.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
GTX_CLK clock period	t _{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t _{GTXH} /t _{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	^t GTKHDX	0.5	—	5.0	ns
GTX_CLK clock rise time (20%-80%)	t _{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t _{GTXF}		_	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the clock reference (K) going to the high state (H) relative to the time date input signals (D) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_DD/OV_DD of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period	t _{GRX}	_	8.0	_	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	_	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.5	_	_	ns

Table 30. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t _{TRDVKH} 2	2.5	—	_	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t _{тRDXKH} ²	1.5	—	_	ns
RX_CLK clock rise time (20%–80%)	t _{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time (80%-20%)	t _{TRXF}	0.7	_	2.4	ns

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
</sub>

2. Setup and hold time of even numbered RCG are measured from the riding edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the riding edge of PMA_RX_CLK0.

Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram



Figure 16 shows the RBMII and RTBI AC timing and multiplexing diagrams.

Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 32 and Table 33.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (2.5 V)	LV _{DD}	—		2.37	2.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = Min$	2.00	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND – 0.3	0.40	V
Input high voltage	V _{IH}	—	$LV_{DD} = Min$	1.7	—	V
Input low voltage	V _{IL}	—	$LV_{DD} = Min$	-0.3	0.70	V

Table 32. MII Management DC Electrical	Characteristics Powered at 2.5 V
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Figure 18 and Figure 19 provide the AC test load and signals for the USB, respectively.



10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8349EA.

10.1 Local Bus DC Electrical Characteristics

Table 37 provides the DC electrical characteristics for the local bus interface.

 Table 37. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current	I _{IN}	_	±5	μA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	_	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	_	0.2	V

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8349EA.

12.1 I²C DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the I²C interface of the MPC8349EA.

Table 42. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	$0.7 \times OV_{DD}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	_
Low level output voltage	V _{OL}	0	$0.2\times\text{OV}_{\text{DD}}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t _{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{i2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I	-10	10	μA	4
Capacitance for each I/O pin	Cl	—	10	pF	_

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. C_B = capacitance of one bus line in pF.

3. Refer to the MPC8349EA Integrated Host Processor Family Reference Manual, for information on the digital filter used.

4. I/O pins obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.

12.2 I²C AC Electrical Specifications

Table 43 provides the AC timing parameters for the I²C interface of the MPC8349EA. Note that all values refer to $V_{IH}(min)$ and $V_{IL}(max)$ levels (see Table 42).

Table 43. I²C AC Electrical Specifications

Parameter	Symbol ¹	Min	Мах	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL}	1.3	—	μS
High period of the SCL clock	t _{I2CH}	0.6	—	μS
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μS
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	-	μs
Data setup time	t _{I2DVKH}	100	—	ns
Data hold time:CBUS compatible masters I ² C bus devices	t _{i2DXKL}	$\overline{0^2}$	0.9 ³	μS

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8349EA.

13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8349EA.

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	$V_{OUT} \le V_{OL}$ (max)	-0.3	0.8	V
Input current	I _{IN}	$V_{IN}^{1} = 0 V \text{ or } V_{IN} = OV_{DD}$	_	±5	μA
High-level output voltage	V _{OH}	OV _{DD} = min, I _{OH} = -100 μA	OV _{DD} – 0.2	_	V
Low-level output voltage	V _{OL}	OV _{DD} = min, I _{OL} = 100 μA	_	0.2	V

Table 44. PCI DC Electrical Characteristics

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8349EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing	Specifications at 66 MHz ¹
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Parameter	Symbol ²	Min	Мах	Unit	Notes
Clock to output valid	^t PCKHOV	—	6.0	ns	3
Output hold from clock	t _{PCKHOX}	1		ns	3
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t _{PCIVKH}	3.0	_	ns	3, 5
Input hold from clock	t _{PCIXKH}	0	_	ns	3, 5
REQ64 to PORESET setup time	t _{PCRVRH}	5	—	clocks	6

Table 47. Timer DC Electrical C	Characteristics (continued)
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Parameter	Symbol	Condition	Min	Мах	Unit
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8349EA GPIO.

Table 49. GPIO DC Electrical Characteristics

PArameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	_	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

SPI

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications¹

Parameter	Symbol ²	Min	Мах	Unit
SPI outputs valid—Master mode (internal clock) delay	t _{NIKHOV}	_	6	ns
SPI outputs hold—Master mode (internal clock) delay	t _{NIKHOX}	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	t _{NEKHOV}	_	8	ns
SPI outputs hold—Slave mode (external clock) delay	t _{NEKHOX}	2	—	ns
SPI inputs—Master mode (internal clock input setup time	t _{NIIVKH}	4	—	ns
SPI inputs—Master mode (internal clock input hold time	t _{NIIXKH}	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	—	ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
</sub>

Figure 37 provides the AC test load for the SPI.



Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 38 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.



Figure 39 shows the SPI timings in master mode (internal clock).



Figure 39. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8349EA is available in a tape ball grid array (TBGA). See Section 18.1, "Package Parameters for the MPC8349EA TBGA" and Section 18.2, "Mechanical Dimensions for the MPC8349EA TBGA.

18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is $35 \text{ mm} \times 35 \text{ mm}$, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

	RCWL		400 MHz Device			533 MHz Device		66	7 MHz Dev	ice	
Ref No. ¹	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
306	0011	0000110		_			_		66	200	600
405	0100	0000101		_			_		66	266	667
504	0101	0000100		_			_		66	333	667

Table 62. Suggested PLL Configurations (continued)

¹ The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

² The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

20 Thermal

This section describes the thermal specifications of the MPC8349EA.

20.1 Thermal Characteristics

Table 63 provides the package thermal characteristics for the 672 35×35 mm TBGA of the MPC8349EA.

Table 63. Package Thermal	Characteristics for TBGA
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Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{ ext{ heta}JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{ ext{ heta}JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{ ext{ heta}JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{ ext{ heta}JMA}$	8	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on single-layer board (1s)	$R_{ ext{ heta}JMA}$	9	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on four-layer board (2s2p)	$R_{ ext{ heta}JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	°C/W	4
Junction-to-case thermal	$R_{ ext{ heta}JC}$	1.7	°C/W	5

Table 63. Package Thermal Characteristics for TBGA (continued)

Characteristic	Symbol	Value	Unit	Notes
Junction-to-package natural convection on top	Ψ_{JT}	1	°C/W	6

Notes:

- 1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 2. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
- 3. Per JEDEC JESD51-6 with the board horizontal, 1 m/s is approximately equal to 200 linear feet per minute (LFM).
- 4. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
- 6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

20.2 Thermal Management Information

For the following sections, $P_D = (V_{DD} \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers. See Table 5 for I/O power dissipation values.

20.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

 T_J = junction temperature (°C)

 T_A = ambient temperature for the package (°C)

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Generally, the value obtained on a single-layer board is appropriate for a tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity $T_J - T_A$) are possible.

20.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction-to-ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 64 shows heat sink thermal resistance for TBGA of the MPC8349EA.

Host Sink Assuming Thermal Grosse	Air Flow	35 imes 35 mm TBGA
neat Sink Assuming merinal drease		Thermal Resistance
AAVID $30 \times 30 \times 9.4$ mm pin fin	Natural convection	10
AAVID $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.5
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	5.6
AAVID 31 \times 35 \times 23 mm pin fin	Natural convection	8.4
AAVID 31 \times 35 \times 23 mm pin fin	1 m/s	4.7
AAVID 31 \times 35 \times 23 mm pin fin	2 m/s	4
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	5.7
Wakefield, $53 \times 53 \times 25$ mm pin fin	1 m/s	3.5
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	2.7
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	6.7
MEI, 75 \times 85 \times 12 no adjacent board, extrusion	1 m/s	4.1
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	2 m/s	2.8
MEI, $75 \times 85 \times 12$ mm, adjacent board, 40 mm side bypass	1 m/s	3.1

Table 64. Heat Sink and Thermal Resistance of MPC8349EA (TBGA)

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.