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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
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- Complies with USB specification Rev. 2.0
- Can operate as a stand-alone USB device
 - One upstream facing port
 - Six programmable USB endpoints
- Can operate as a stand-alone USB host controller
 - USB root hub with one downstream-facing port
 - Enhanced host controller interface (EHCI) compatible
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- External PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- Universal serial bus (USB) multi-port host controller
 - Can operate as a stand-alone USB host controller
 - USB root hub with one or two downstream-facing ports
 - Enhanced host controller interface (EHCI) compatible
 - Complies with USB Specification Rev. 2.0
 - High-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
 - Direct connection to a high-speed device without an external hub
 - External PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
 - Multiplexed 32-bit address and data operating at up to 133 MHz
 - Eight chip selects for eight external slaves
 - Up to eight-beat burst transfers
 - 32-, 16-, and 8-bit port sizes controlled by an on-chip memory controller
 - Three protocol engines on a per chip select basis:
 - General-purpose chip select machine (GPCM)
 - Three user-programmable machines (UPMs)
 - Dedicated single data rate SDRAM controller
 - Parity support
 - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
 - Functional and programming compatibility with the MPC8260 interrupt controller
 - Support for 8 external and 35 internal discrete interrupt sources
 - Support for 1 external (optional) and 7 internal machine checkstop interrupt sources
 - Programmable highest priority request
 - Four groups of interrupts with programmable priority
 - External and internal interrupts directed to host processor
 - Redirects interrupts to external INTA pin in core disable mode.
 - Unique vector number for each interrupt source

Electrical Characteristics

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8349EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Parameter	Symbol	Recommended Value	Unit	Notes
Core supply voltage for 667-MHz core frequency	V _{DD}	1.3 V ± 60 mV	V	1
Core supply voltage	V _{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage for 667-MHz core frequency	AV_{DD}	1.3 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
Three-speed Ethernet I/O supply voltage	LV _{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	_

Table 2. Recommended C	Operating Co	nditions
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Note:

¹ GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8349EA.



Table 11 lists the PLL and DLL lock times.

Table 11. PLL and DLL Lock Times

Parameter/Condition	Min	Мах	Unit	Notes
PLL lock times	-	100	μs	_
DLL lock times	7680	122,880	csb_clk cycles	1, 2

Notes:

1. DLL lock times are a function of the ratio between the output clock and the coherency system bus clock (csb_clk). A 2:1 ratio results in the minimum and an 8:1 ratio results in the maximum.

2. The csb_clk is determined by the CLKIN and system PLL ratio. See Section 19, "Clocking."

6 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8349EA. Note that DDR SDRAM is $GV_{DD}(typ) = 2.5$ V and DDR2 SDRAM is $GV_{DD}(typ) = 1.8$ V. The AC electrical specifications are the same for DDR and DRR2 SDRAM.

NOTE

The information in this document is accurate for revision 3.0 silicon and later. For information on revision 1.1 silicon and earlier versions see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*. See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

6.1 DDR and DDR2 SDRAM DC Electrical Characteristics

Table 12 provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8349EA when $GV_{DD}(typ) = 1.8 \text{ V}.$

Table 12	. DDR2	SDRAM D	C Electrica	I Characteristics	for GV _{DD} (typ) = 1.8 V
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Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O supply voltage	GV _{DD}	1.71	1.89	V	1
I/O reference voltage	MV _{REF}	$0.49 imes GV_{DD}$	$0.51 imes GV_{DD}$	V	2
I/O termination voltage	V _{TT}	MV _{REF} – 0.04	MV _{REF} + 0.04	V	3
Input high voltage	V _{IH}	MV _{REF} + 0.125	GV _{DD} + 0.3	V	—
Input low voltage	V _{IL}	-0.3	MV _{REF} – 0.125	V	—
Output leakage current	I _{OZ}	-9.9	9.9	μA	4
Output high current (V _{OUT} = 1.420 V)	I _{OH}	-13.4	_	mA	—

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
ADDR/CMD/MODT output setup with respect to MCK	t _{DDKHAS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
ADDR/CMD/MODT output hold with respect to MCK	t _{DDKHAX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output setup with respect to MCK	t _{DDKHCS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output hold with respect to MCK	t _{DDKHCX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	_		
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t _{DDKHDS,} t _{DDKLDS}			ps	5
400 MHz		700	—		
333 MHz		775	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	t _{DDKHDX,} t _{DDKLDX}			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{\text{MCK}}-0.6$	$-0.5\times t_{MCK}+0.6$	ns	6

Parameter	Symbol	Min	Мах	Unit
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	-	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}	—	0.2	V

7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16		2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8th sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16th sample.

8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

Table 26. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock rise (20%–80%)	t _{GRXR}		_	1.0	ns
RX_CLK clock fall time (80%-20%)	t _{GRXF}	_		1.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

Figure 10 shows the GMII receive AC timing diagram.



8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 27 provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Tim	ing Specifications
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At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.
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Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
TX_CLK clock period 10 Mbps	t _{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t _{MTX}	—	40	—	ns
TX_CLK duty cycle	t _{MTXH} /t _{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t _{MTKHDX}	1	5	15	ns

Ethernet: Three-Speed Ethernet, MII Management

Table 27. MII Transmit AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
TX_CLK data clock rise (20%-80%)	t _{MTXR}	1.0	_	4.0	ns
TX_CLK data clock fall (80%–20%)	t _{MTXF}	1.0		4.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). In general, the clock reference symbol is based on two to three letters representing the clock of a particular function. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 11 shows the MII transmit AC timing diagram.



Figure 11. MII Transmit AC Timing Diagram

8.2.2.2 MII Receive AC Timing Specifications

Table 28 provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
RX_CLK clock period 10 Mbps	t _{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t _{MRX}	—	40	—	ns
RX_CLK duty cycle	t _{MRXH} /t _{MRX}	35	_	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	_	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	_		ns

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	_	4.0	ns
RX_CLK clock fall time (80%-20%)	t _{MRXF}	1.0	_	4.0	ns

Note:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

Figure 12 provides the AC test load for TSEC.



Figure 12. TSEC AC Test Load

Figure 13 shows the MII receive AC timing diagram.



Figure 13. MII Receive AC Timing Diagram

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



Figure 16 shows the RBMII and RTBI AC timing and multiplexing diagrams.

Figure 16. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to the MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for GMII, RGMII, TBI and RTBI are specified in Section 8.1, "Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics."

8.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 2.5 or 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 32 and Table 33.

Parameter	Symbol	Conditions		Min	Мах	Unit
Supply voltage (2.5 V)	LV _{DD}	-	_	2.37	2.63	V
Output high voltage	V _{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = Min$	2.00	LV _{DD} + 0.3	V
Output low voltage	V _{OL}	I _{OL} = 1.0 mA	$LV_{DD} = Min$	GND – 0.3	0.40	V
Input high voltage	V _{IH}	—	$LV_{DD} = Min$	1.7	—	V
Input low voltage	V _{IL}	—	$LV_{DD} = Min$	-0.3	0.70	V

Table 32. MII Management DC Electrical	Characteristics Powered at 2.5 V
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Figure 18 and Figure 19 provide the AC test load and signals for the USB, respectively.



10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8349EA.

10.1 Local Bus DC Electrical Characteristics

Table 37 provides the DC electrical characteristics for the local bus interface.

 Table 37. Local Bus DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current	I _{IN}	_	±5	μA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V _{OH}	OV _{DD} - 0.2	_	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V _{OL}		0.2	V





Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)



Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

Parameter	Symbol ¹	Min	Max	Unit
Fall time of both SDA and SCL signals ⁵	t _{I2CF}	—	300	ns
Setup time for STOP condition	t _{I2PVKH}	0.6	—	μS
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	—	μS
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V

Table 43. I²C AC Electrical Specifications (continued)

Notes:

- 1. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2DVKH} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) goes invalid (X) relative to the t_{I2C} clock reference (K) going to the stop condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- The device provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}(min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DVKH} must be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.
- 5.) The device does not follow the "I2C-BUS Specifications" version 2.1 regarding the tI2CF AC parameter.

Figure 32 provides the AC test load for the I^2C .



Figure 32. I²C AC Test Load

Figure 33 shows the AC timing diagram for the I^2C bus.



Figure 33. I²C Bus AC Timing Diagram

Table 45. PCI AC Timing Specifications at 66 MHz ¹	(continued)
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Parameter	Symbol ²	Min	Max	Unit	Notes
PORESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	6

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.}
- 3. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.
- 6. The setup and hold time is with respect to the rising edge of PORESET.

Table 46 provides the PCI AC timing specifications at 33 MHz.

Table 46. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol ¹	Min	Max	Unit	Notes
Clock to output valid	^t PCKHOV	—	11	ns	2
Output hold from clock	t _{PCKHOX}	2		ns	2
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t _{PCIVKH}	3.0	-	ns	2, 4
Input hold from clock	t _{PCIXKH}	0	_	ns	2, 4
REQ64 to PORESET setup time	t _{PCRVRH}	5	_	clocks	5
PORESET to REQ64 hold time	t _{PCRHRX}	0	50	ns	5

Notes:

2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.

3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4. Input timings are measured at the pin.

5. The setup and hold time is with respect to the rising edge of PORESET.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
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Table 47. Timer DC Electrical C	Characteristics (continued)
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Parameter	Symbol	Symbol Condition		Мах	Unit
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications¹

Parameter	Symbol ²	Min	Unit
Timers inputs—minimum pulse width	t _{TIWID}	20	ns

Notes:

1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.

2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8349EA GPIO.

Table 49. GPIO DC Electrical Characteristics

PArameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	_	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	_	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

SPI

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V _{IH}	—	2.0	OV _{DD} + 0.3	V
Input low voltage	V _{IL}	—	-0.3	0.8	V
Input current	I _{IN}	—	—	±5	μA
Output high voltage	V _{OH}	I _{OH} = -8.0 mA	2.4	—	V
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	—	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications¹

Parameter	Symbol ²	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t _{NIKHOV}	_	6	ns
SPI outputs hold—Master mode (internal clock) delay	t _{NIKHOX}	0.5	_	ns
SPI outputs valid—Slave mode (external clock) delay	t _{NEKHOV}	_	8	ns
SPI outputs hold—Slave mode (external clock) delay	t _{NEKHOX}	2	_	ns
SPI inputs—Master mode (internal clock input setup time	t _{NIIVKH}	4	_	ns
SPI inputs—Master mode (internal clock input hold time	t _{NIIXKH}	0	_	ns
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	_	ns
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	_	ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
</sub>

18.1 Package Parameters for the MPC8349EA TBGA

The package parameters are provided in the following list. The package type is $35 \text{ mm} \times 35 \text{ mm}$, 672 tape ball grid array (TBGA).

Package outline	35 mm × 35 mm
Interconnects	672
Pitch	1.00 mm
Module height (typical)	1.46 mm
Solder balls	62 Sn/36 Pb/2 Ag (ZU package) 96.5 Sn/3.5Ag (VV package)
Ball diameter (typical)	0.64 mm

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF2	AD2	I	DDR reference voltage	_

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV_{DD}.

2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV_{DD}.

3. During reset, this output is actively driven rather than three-stated.

4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.

6. This pin must always be tied to GND.

7. This pin must always be left not connected.

8. Thermal sensitive resistor.

9. It is recommended that MDIC0 be tied to GND using an 18.2 Ω resistor and MDIC1 be tied to DDR power using an 18.2 Ω resistor.

10.TSEC1_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

11. A weak pull-up resistor (2–10 k Ω) should be placed on this pin to LV_{DD1}.

12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

	RC	WL	40) MHz Dev	ice	533 MHz Device			MHz Device 667 MHz Device		
Ref No. ¹	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
306	0011	0000110	—		—		66	200	600		
405	0100	0000101	_		_		66	266	667		
504	0101	0000100		—		—		66	333	667	

Table 62. Suggested PLL Configurations (continued)

¹ The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.

² The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

20 Thermal

This section describes the thermal specifications of the MPC8349EA.

20.1 Thermal Characteristics

Table 63 provides the package thermal characteristics for the 672 35×35 mm TBGA of the MPC8349EA.

Table 63. Package Thermal	Characteristics for TBGA
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Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{ ext{ heta}JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{ ext{ heta}JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{ ext{ heta}JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{ ext{ heta}JMA}$	8	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on single-layer board (1s)	$R_{ ext{ heta}JMA}$	9	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on four-layer board (2s2p)	$R_{ ext{ heta}JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	°C/W	4
Junction-to-case thermal	$R_{ ext{ heta}JC}$	1.7	°C/W	5

System Design Information

2. The e300 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e300 core clock and the platform clock is selected using the e300 PLL ratio configuration bits as described in Section 19.2, "Core PLL Configuration."

21.2 PLL Power Supply Filtering

Each PLL gets power through independent power supply pins ($AV_{DD}1$, $AV_{DD}2$, respectively). The AV_{DD} level should always equal to V_{DD} , and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to provide power reliably to the PLLs, but the recommended solution is to provide four independent filter circuits as illustrated in Figure 42, one to each of the four AV_{DD} pins. Independent filters to each PLL reduce the opportunity to cause noise injection from one PLL to the other.

The circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

To minimize noise coupled from nearby circuits, each circuit should be placed as closely as possible to the specific AV_{DD} pin being supplied. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias.

Figure 42 shows the PLL power supply filter circuit.



Figure 42. PLL Power Supply Filter Circuit

21.3 Decoupling Recommendations

Due to large address and data buses and high operating frequencies, the MPC8349EA can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8349EA system, and the device itself requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} pin of the device. These capacitors should receive their power from separate V_{DD} , OV_{DD} , GV_{DD} , LV_{DD} , and GND power planes in the PCB, with short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Others can surround the part.

These capacitors should have a value of 0.01 or 0.1 μ F. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, distribute several bulk storage capacitors around the PCB, feeding the V_{DD} , OV_{DD} , GV_{DD} , and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should

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