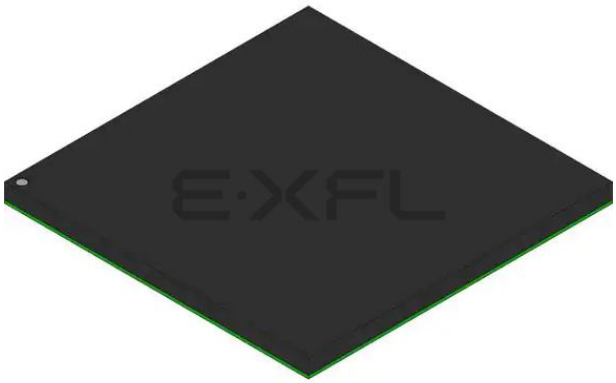


Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8349vvagdb

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications.*

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8349EA.

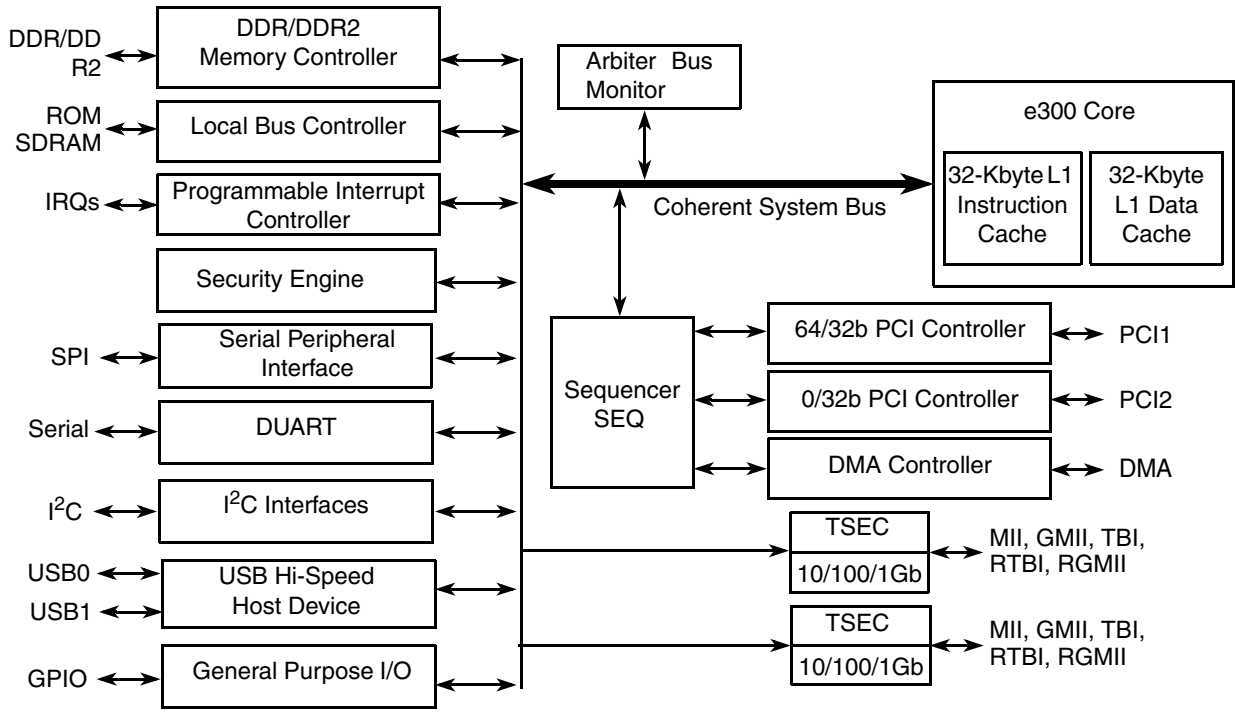


Figure 1. MPC8349EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology

- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - Handshaking (external control) signals for all channels: $\overline{\text{DMA\_DREQ}}$[0:3], $\overline{\text{DMA\_DACK}}$[0:3], $\overline{\text{DMA\_DDONE}}$[0:3]
  - All channels accessible to local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI) for master or slave
- General-purpose parallel I/O (GPIO)
  - 64 parallel I/O pins multiplexed on various chip interfaces
- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- Designed to comply with IEEE Std. 1149.1™, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8349EA. The device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings[1]

Parameter		Symbol	Max Value	Unit	Notes
Core supply voltage		V_{DD}	–0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
PLL supply voltage		AV_{DD}	–0.3 to 1.32 (1.36 max for 667-MHz core frequency)	V	—
DDR and DDR2 DRAM I/O voltage		GV_{DD}	–0.3 to 2.75 –0.3 to 1.98	V	—
Three-speed Ethernet I/O, MII management voltage		LV_{DD}	–0.3 to 3.63	V	—
PCI, local bus, DUART, system control and power management, I^2C, and JTAG I/O voltage		OV_{DD}	–0.3 to 3.63	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	DDR DRAM reference	MV_{REF}	–0.3 to (GV_{DD} + 0.3)	V	2, 5
	Three-speed Ethernet signals	LV_{IN}	–0.3 to (LV_{DD} + 0.3)	V	4, 5
	Local bus, DUART, CLKIN, system control and power management, I^2C, and JTAG signals	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	3, 5
	PCI	OV_{IN}	–0.3 to (OV_{DD} + 0.3)	V	6
Storage temperature range		T_{STG}	–55 to 150	°C	—

Notes:

1 Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2 **Caution:** MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3 **Caution:** OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4 **Caution:** LV_{IN} must not exceed LV_{DD} by more than 0.3 V. This limit can be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5 (M,L,O)V_{IN} and MV_{REF} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.

6 OVIN on the PCI interface can overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 3.

Figure 3 shows the undershoot and overshoot voltage of the PCI interface of the MPC8349EA for the 3.3-V signals, respectively.

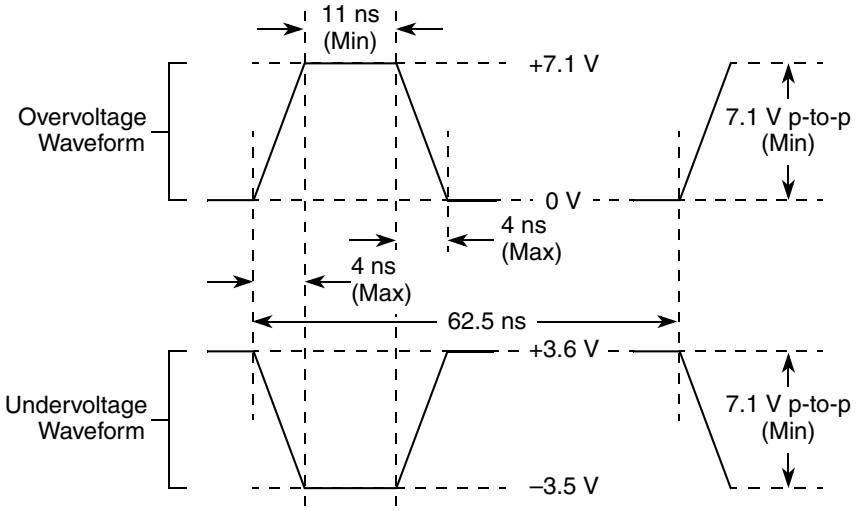


Figure 3. Maximum AC Waveforms on PCI Interface for 3.3-V Signaling

2.1.3 Output Driver Characteristics

Table 3 provides information on the characteristics of the output driver strengths. The values are preliminary estimates.

Table 3. Output Drive Capability

Driver Type	Output Impedance (Ω)	Supply Voltage
Local bus interface utilities signals	40	OV_{DD} = 3.3 V
PCI signals (not including PCI output clocks)	25	
PCI output clocks (including PCI_SYNC_OUT)	40	
DDR signal	18	GV_{DD} = 2.5 V
DDR2 signal	18 36 (half-strength mode)	GV_{DD} = 1.8 V
TSEC/10/100 signals	40	LV_{DD} = 2.5/3.3 V
DUART, system control, I^2C, JTAG, USB	40	OV_{DD} = 3.3 V
GPIO signals	40	OV_{DD} = 3.3 V, LV_{DD} = 2.5/3.3 V

2.2 Power Sequencing

This section details the power sequencing considerations for the MPC8349EA.

2.2.1 Power-Up Sequencing

MPC8349EA does not require the core supply voltage (V_{DD} and AV_{DD}) and I/O supply voltages (GV_{DD}, LV_{DD}, and OV_{DD}) to be applied in any particular order. During the power ramp up, before the power

4.3 TSEC Gigabit Reference Clock Timing

Table 8 provides the TSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications.

Table 8. EC_GTX_CLK125 AC Timing Specifications

At recommended operating conditions with LV_{DD} = 2.5 ± 0.125 mV/ 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Notes
EC_GTX_CLK125 frequency	t_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK125 rise and fall time LV_{DD} = 2.5 V LV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	 0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	 45 47	—	 55 53	%	2
EC_GTX_CLK125 jitter	—	—	—	±150	ps	2

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for LV_{DD} = 2.5 V and from 0.6 and 2.7 V for LV_{DD} = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. The EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.2.4, “RGMII and RTBI AC Timing Specifications for the duty cycle for 10Base-T and 100Base-T reference clock.

5 RESET Initialization

This section describes the DC and AC electrical specifications for the reset initialization timing and electrical requirements of the MPC8349EA.

5.1 RESET DC Electrical Characteristics

Table 9 provides the DC electrical characteristics for the RESET pins of the MPC8349EA.

Table 9. RESET Pins DC Electrical Characteristics[1]

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage[2]	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V

Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t_{CISKEW}			ps	1, 2
400 MHz		–600	600		3
333 MHz		–750	750		—
266 MHz		–750	750		—
200 MHz		–750	750		—

Notes:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the equation: $t_{DISKEW} = \pm (T/4 - abs(t_{CISKEW}))$; where T is the clock period and abs (t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t_{DISKEW} timing parameter.

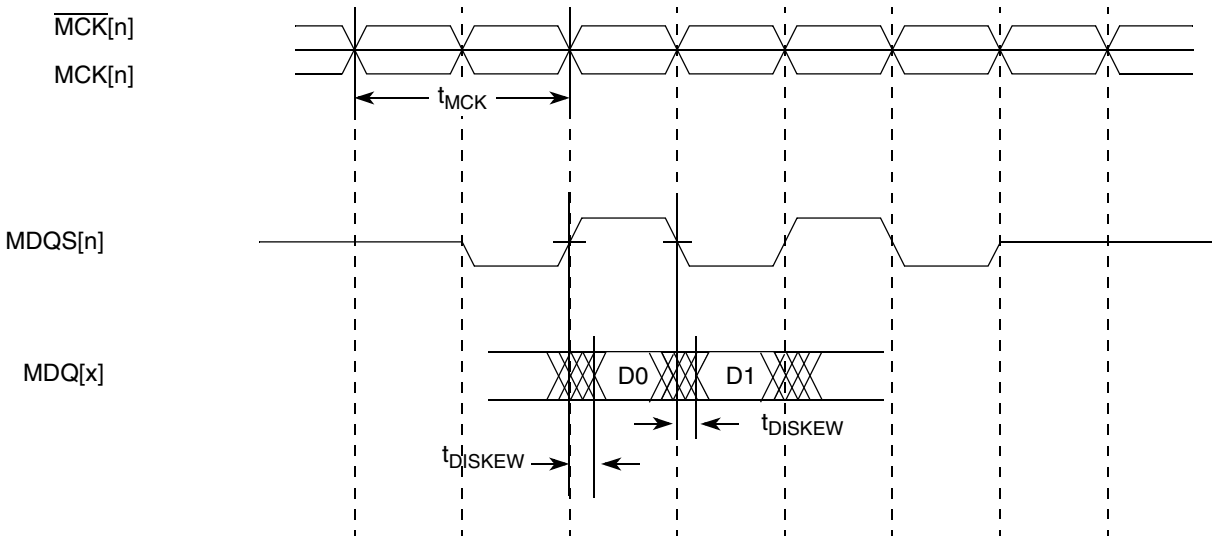


Figure 5. DDR Input Timing Diagram

Table 26. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{GRXR}	—	—	1.0	ns
RX_CLK clock fall time (80%–20%)	t_{GRXF}	—	—	1.0	ns

Note:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 10 shows the GMII receive AC timing diagram.

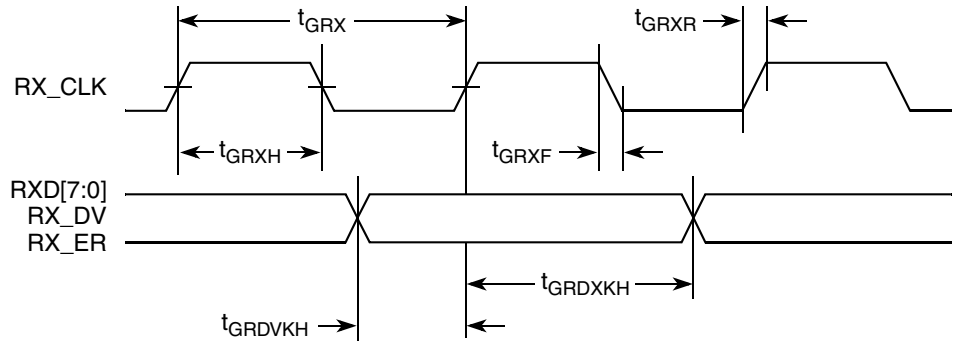


Figure 10. GMII Receive AC Timing Diagram

8.2.2 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

8.2.2.1 MII Transmit AC Timing Specifications

Table 27 provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns

8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

Table 31. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.5	—	0.5	ns
Data to clock input skew (at receiver)[2]	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration[3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T[4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX[3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.
5. Duty cycle reference is $LV_{DD}/2$.

Table 32. MII Management DC Electrical Characteristics Powered at 2.5 V (continued)

Parameter	Symbol	Conditions	Min	Max	Unit
Input high current	I_{IH}	V_{IN}[1] = LV_{DD}	—	10	μA
Input low current	I_{IL}	V_{IN} = LV_{DD}	–15	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

Table 33. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	LV_{DD}	—		2.97	3.63	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	LV_{DD} = Min	2.10	LV_{DD} + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	LV_{DD} = Min	GND	0.50	V
Input high voltage	V_{IH}	—		2.00	—	V
Input low voltage	V_{IL}	—		—	0.80	V
Input high current	I_{IH}	LV_{DD} = Max	V_{IN}[1] = 2.1 V	—	40	μA
Input low current	I_{IL}	LV_{DD} = Max	V_{IN} = 0.5 V	–600	—	μA

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.3.2 MII Management AC Electrical Specifications

Table 34 provides the MII management AC timing specifications.

Table 34. MII Management AC Timing Specifications

At recommended operating conditions with LV_{DD} is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	10	—	70	ns	3
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8349EA.

9.1 USB DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the USB interface.

Table 35. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	OV_{DD} + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	OV_{DD} – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 36 describes the general timing parameters of the USB interface of the MPC8349EA.

Table 36. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol[1]	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2–5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2–5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to 0.4 × OV_{DD} of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Table 40. JTAG Interface DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA. Table 41 provides the JTAG AC timing specifications as defined in Figure 28 through Figure 31.

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)[1]

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)[1] (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol[2]	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8349EA.

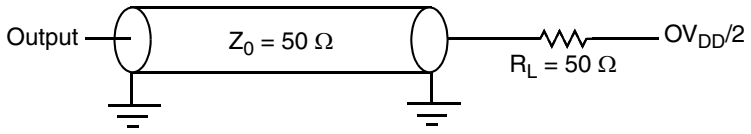


Figure 27. AC Test Load for the JTAG Interface

Figure 28 provides the JTAG clock input timing diagram.

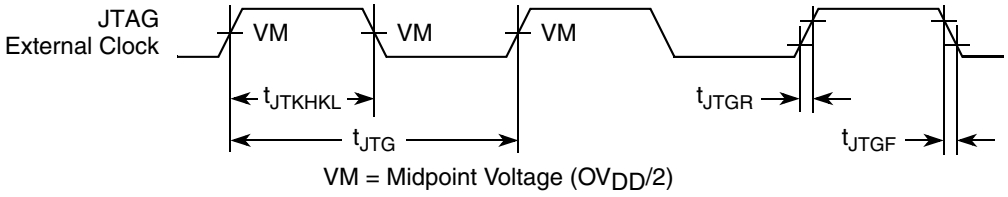


Figure 28. JTAG Clock Input Timing Diagram

Figure 29 provides the $\overline{\text{TRST}}$ timing diagram.

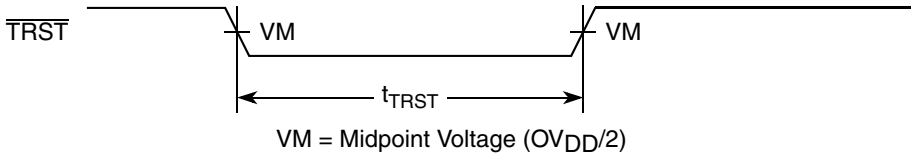


Figure 29. $\overline{\text{TRST}}$ Timing Diagram

Table 47. Timer DC Electrical Characteristics (continued)

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

14.2 Timer AC Timing Specifications

Table 48 provides the timer input and output AC timing specifications.

Table 48. Timers Input AC Timing Specifications[1]

Parameter	Symbol[2]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Notes:
1. Input specifications are measured from the 50 percent level of the signal to the 50 percent level of the rising edge of CLKIN. Timings are measured at the pin.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

15 GPIO

This section describes the DC and AC electrical specifications for the GPIO.

15.1 GPIO DC Electrical Characteristics

Table 49 provides the DC electrical characteristics for the MPC8349EA GPIO.

Table 49. GPIO DC Electrical Characteristics

PArameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	OV_{DD} + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

Figure 37 provides the AC test load for the SPI.

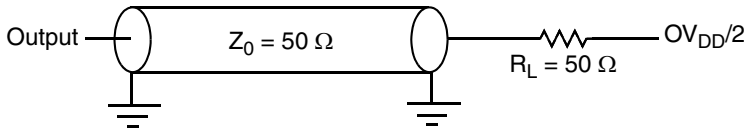
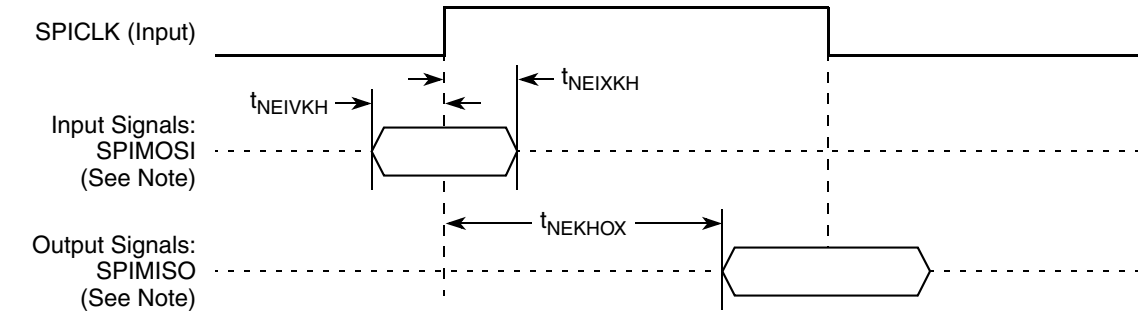


Figure 37. SPI AC Test Load

Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

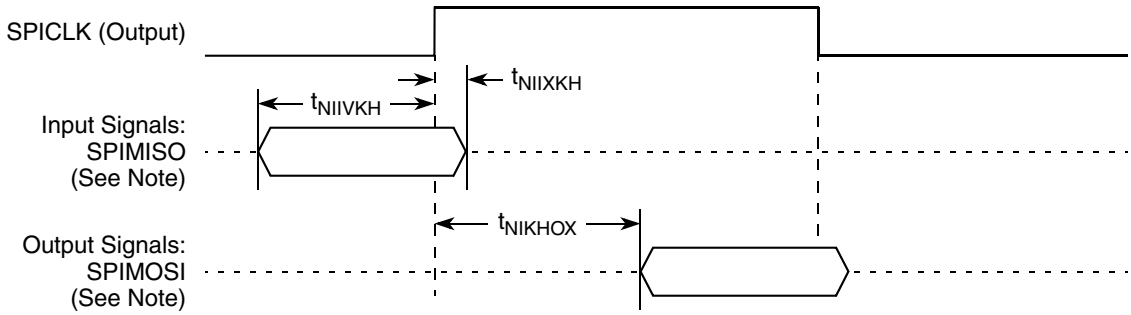
Figure 38 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 38. SPI AC Timing in Slave Mode (External Clock) Diagram

Figure 39 shows the SPI timings in master mode (internal clock).



Note: The clock edge is selectable on SPI.

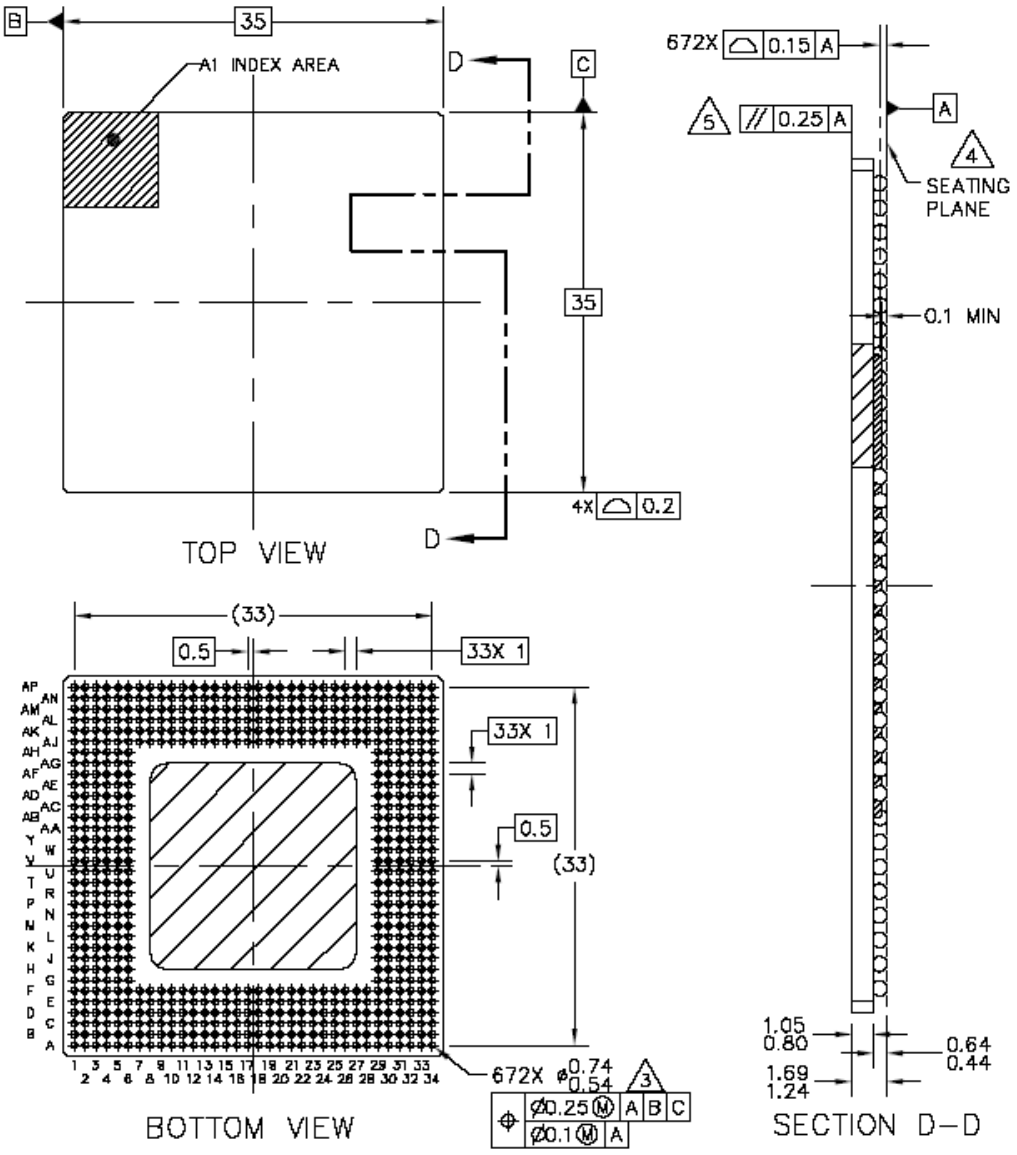
Figure 39. SPI AC Timing in Master Mode (Internal Clock) Diagram

18 Package and Pin Listings

This section details package parameters, pin assignments, and dimensions. The MPC8349EA is available in a tape ball grid array (TBGA). See Section 18.1, “Package Parameters for the MPC8349EA TBGA” and Section 18.2, “Mechanical Dimensions for the MPC8349EA TBGA.

18.2 Mechanical Dimensions for the MPC8349EA TBGA

Figure 40 shows the mechanical dimensions and bottom surface nomenclature for the MPC8349EA, 672-TBGA package.



Notes:

1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement must exclude any effect of mark on top surface of package.

Figure 40. Mechanical Dimensions and Bottom Surface Nomenclature for the MPC8349EA TBGA

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Gigabit Reference Clock				
EC_GTX_CLK125	C8	I	LV_{DD1}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_COL/GPIO2[20]	A17	I/O	OV_{DD}	—
TSEC1_CRS/GPIO2[21]	F12	I/O	LV_{DD1}	—
TSEC1_GTX_CLK	D10	O	LV_{DD1}	3
TSEC1_RX_CLK	A11	I	LV_{DD1}	—
TSEC1_RX_DV	B11	I	LV_{DD1}	—
TSEC1_RX_ER/GPIO2[26]	B17	I/O	OV_{DD}	—
TSEC1_RXD[7:4]/GPIO2[22:25]	B16, D16, E16, F16	I/O	OV_{DD}	—
TSEC1_RXD[3:0]	E10, A8, F10, B8	I	LV_{DD1}	—
TSEC1_TX_CLK	D17	I	OV_{DD}	—
TSEC1_TXD[7:4]/GPIO2[27:30]	A15, B15, A14, B14	I/O	OV_{DD}	—
TSEC1_TXD[3:0]	A10, E11, B10, A9	O	LV_{DD1}	10
TSEC1_TX_EN	B9	O	LV_{DD1}	—
TSEC1_TX_ER/GPIO2[31]	A16	I/O	OV_{DD}	—
Three-Speed Ethernet Controller (Gigabit Ethernet 2)				
TSEC2_COL/GPIO1[21]	C14	I/O	OV_{DD}	—
TSEC2_CRS/GPIO1[22]	D6	I/O	LV_{DD2}	—
TSEC2_GTX_CLK	A4	O	LV_{DD2}	—
TSEC2_RX_CLK	B4	I	LV_{DD2}	—
TSEC2_RX_DV/GPIO1[23]	E6	I/O	LV_{DD2}	—
TSEC2_RXD[7:4]/GPIO1[26:29]	A13, B13, C13, A12	I/O	OV_{DD}	—
TSEC2_RXD[3:0]/GPIO1[13:16]	D7, A6, E8, B7	I/O	LV_{DD2}	—
TSEC2_RX_ER/GPIO1[25]	D14	I/O	OV_{DD}	—
TSEC2_TXD[7]/GPIO1[31]	B12	I/O	OV_{DD}	—
TSEC2_TXD[6]/ DR_XCVR_TERM_SEL	C12	O	OV_{DD}	—
TSEC2_TXD[5]/ DR_UTMI_OPMODE1	D12	O	OV_{DD}	—
TSEC2_TXD[4]/ DR_UTMI_OPMODE0	E12	O	OV_{DD}	—
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV_{DD2}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TSEC2_TX_ER/GPIO1[24]	F14	I/O	OV_{DD}	—
TSEC2_TX_EN/GPIO1[12]	C5	I/O	LV_{DD2}	—
TSEC2_TX_CLK/GPIO1[30]	E14	I/O	OV_{DD}	—
DUART				
UART_SOUT[1:2]/MSRCID[0:1]/ LSRCID[0:1]	AK27, AN29	O	OV_{DD}	—
UART_SIN[1:2]/MSRCID[2:3]/ LSRCID[2:3]	AL28, AM29	I/O	OV_{DD}	—
$\overline{\text{UART\_CTS}}$[1]/MSRCID4/LSRCID4	AP30	I/O	OV_{DD}	—
$\overline{\text{UART\_CTS}}$[2]/MDVAL/ LDVAL	AN30	I/O	OV_{DD}	—
$\overline{\text{UART\_RTS}}$[1:2]	AP31, AM30	O	OV_{DD}	—
I^2C interface				
IIC1_SDA	AK29	I/O	OV_{DD}	2
IIC1_SCL	AP32	I/O	OV_{DD}	2
IIC2_SDA	AN31	I/O	OV_{DD}	2
IIC2_SCL	AM31	I/O	OV_{DD}	2
SPI				
SPIMOSI/$\overline{\text{LCS}}$[6]	AN32	I/O	OV_{DD}	—
SPIMISO/$\overline{\text{LCS}}$[7]	AP33	I/O	OV_{DD}	—
SPICLK	AK30	I/O	OV_{DD}	—
SPISEL	AL31	I	OV_{DD}	—
Clocks				
PCI_CLK_OUT[0:2]	AN9, AP9, AM10,	O	OV_{DD}	—
PCI_CLK_OUT[3]/$\overline{\text{LCS}}$[6]	AN10	O	OV_{DD}	—
PCI_CLK_OUT[4]/$\overline{\text{LCS}}$[7]	AJ11	O	OV_{DD}	—
PCI_CLK_OUT[5:7]	AP10, AL11, AM11	O	OV_{DD}	—
PCI_SYNC_IN/PCI_CLOCK	AK12	I	OV_{DD}	—
PCI_SYNC_OUT	AP11	O	OV_{DD}	3
RTC/PIT_CLOCK	AM32	I	OV_{DD}	—
CLKIN	AM9	I	OV_{DD}	—
JTAG				
TCK	E20	I	OV_{DD}	—
TDI	F20	I	OV_{DD}	4

Table 58. System PLL Multiplication Factors (continued)

RCWL[SPMF]	System PLL Multiplication Factor
0111	× 7
1000	× 8
1001	× 9
1010	× 10
1011	× 11
1100	× 12
1101	× 13
1110	× 14
1111	× 15

As described in Section 19, "Clocking," the LBIUCM, DDRCM, and SPMF parameters in the reset configuration word low and the CFG_CLKIN_DIV configuration input signal select the ratio between the primary clock input (CLKIN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 59 and Table 60 show the expected frequency values for the CSB frequency for select *csb_clk* to CLKIN/PCI_SYNC_IN ratios.

Table 59. CSB Frequency Options for Host Mode

CFG_CLKIN_DIV at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio[2]	Input Clock Frequency (MHz)[2]			
			16.67	25	33.33	66.67
			csb_clk Frequency (MHz)			
Low	0010	2 : 1				133
Low	0011	3 : 1			100	200
Low	0100	4 : 1		100	133	266
Low	0101	5 : 1		125	166	333

Table 62. Suggested PLL Configurations (continued)

Ref No.[1]	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz)[2]	CSB Freq (MHz)	Core Freq (MHz)
306	**0011**	**0000110**	—			—			66	200	600
405	**0100**	**0000101**	—			—			66	266	667
504	**0101**	**0000100**	—			—			66	333	667

1 The PLL configuration reference number is the hexadecimal representation of RCWL, bits 4–15 associated with the SPMF and COREPLL settings given in the table.
2 The input clock is CLKIN for PCI host mode or PCI_CLK for PCI agent mode.

20 Thermal

This section describes the thermal specifications of the MPC8349EA.

20.1 Thermal Characteristics

Table 63 provides the package thermal characteristics for the 672 35 × 35 mm TBGA of the MPC8349EA.

Table 63. Package Thermal Characteristics for TBGA

Characteristic	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection on single-layer board (1s)	$R_{\theta JA}$	14	°C/W	1, 2
Junction-to-ambient natural convection on four-layer board (2s2p)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on single-layer board (1s)	$R_{\theta JMA}$	11	°C/W	1, 3
Junction-to-ambient (at 200 ft/min) on four-layer board (2s2p)	$R_{\theta JMA}$	8	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on single-layer board (1s)	$R_{\theta JMA}$	9	°C/W	1, 3
Junction-to-ambient (at 2 m/s) on four-layer board (2s2p)	$R_{\theta JMA}$	7	°C/W	1, 3
Junction-to-board thermal	$R_{\theta JB}$	3.8	°C/W	4
Junction-to-case thermal	$R_{\theta JC}$	1.7	°C/W	5

Table 68. Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
9	2/2009	• Added footnote 6 to Table 7. • In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. • In Table 39, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 22, Figure 24, and Figure 25 for output signals. • Added footnote 11 to Table 55. • Added footnote 4 to Table 66. • In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. • In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." • In Table 57, corrected the max csb_clk to 266 MHz. • In Table 62, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz • In Table 66, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 533 with a platform frequency of 266."
8	4/2007	• In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. • In Section 21.7, "Pull-Up Resistor Requirements,"deleted last two paragraphs and after first paragraph, added a new paragraph. • Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
7	3/2007	• In Table 57, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (*csb_clk*)' row, changed the value in the 533 MHz column to 100-333. • In Table 63, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. • In Section 23, "Ordering Information," replaced first paragraph and added a note. • In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
6	2/2007	• Page 1, updated first paragraph to reflect PowerQUICC II Pro information. • In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. • In Figure 41, "JTAG Interface Connection," updated with new figure. • In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced third sentence of first paragraph directing customer to product summary page for available frequency configuration parts.
5	1/2007	• In Table 1, "Absolute Maximum Ratings," added (1.36 max for 667-MHz core frequency) to max V_{DD} and Av_{DD} values. • In Table 2, "Recommended Operating Conditions," added a row showing nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts. • In Table 4, "MPC8349EA Power Dissipation," added two footnotes to 667-MHz row showing nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts. • In Table 54, "MPC83479EA (TBGA) Pinout Listing," updated V_{DD} nd AV_{DD} rows to show nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T_{ddkhds} for 333 MHz from 900 ps to 775 ps.