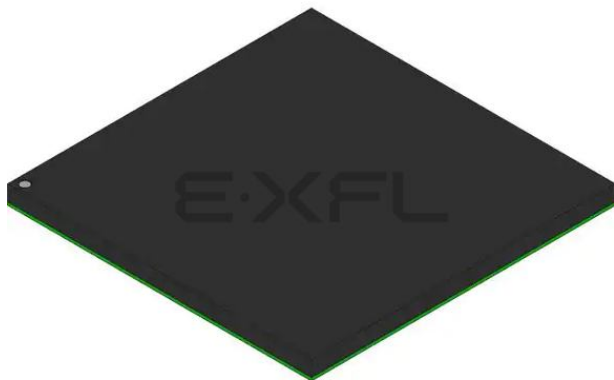




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Details

Product Status	Active
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	533MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8349vvajfb

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8349EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Parameter	Symbol	Recommended Value	Unit	Notes
Core supply voltage for 667-MHz core frequency	V _{DD}	1.3 V ± 60 mV	V	1
Core supply voltage	V _{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage for 667-MHz core frequency	AV _{DD}	1.3 V ± 60 mV	V	1
PLL supply voltage	AV _{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	LV _{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	LV _{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	—

Note:

¹ GV_{DD} , LV_{DD} , OV_{DD} , AV_{DD} , and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8349EA.

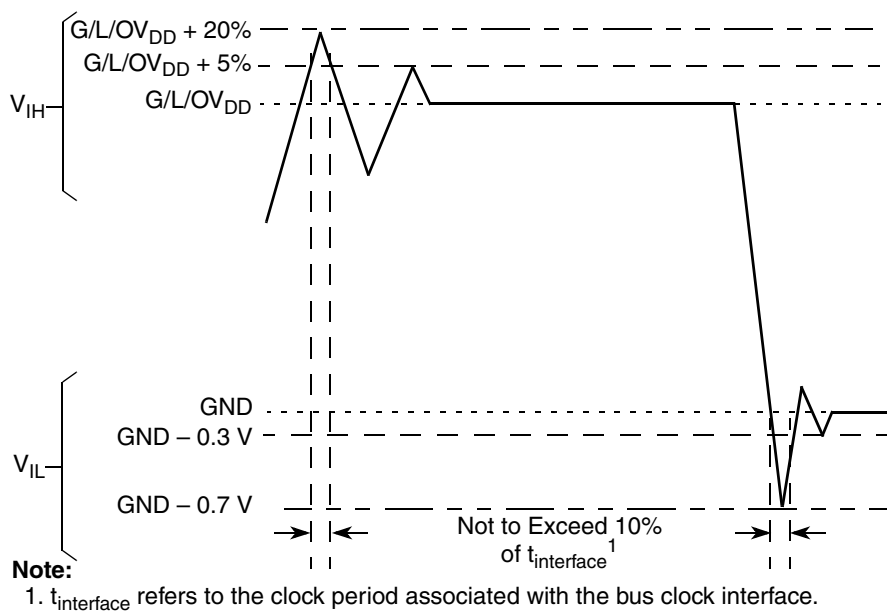


Figure 2. Overshoot/Undershoot Voltage for GV_{DD}/OV_{DD}/LV_{DD}

supplies are stable and if the I/O voltages are supplied before the core voltage, there may be a period of time that all input and output pins will actively be driven and cause contention and excessive current from 3A to 5A. In order to avoid actively driving the I/O pins and to eliminate excessive current draw, apply the core voltage (V_{DD}) before the I/O voltage (GV_{DD} , LV_{DD} , and OV_{DD}) and assert $\overline{PORESET}$ before the power supplies fully ramp up. In the case where the core voltage is applied first, the core voltage supply must rise to 90% of its nominal value before the I/O supplies reach 0.7 V, see Figure 4.

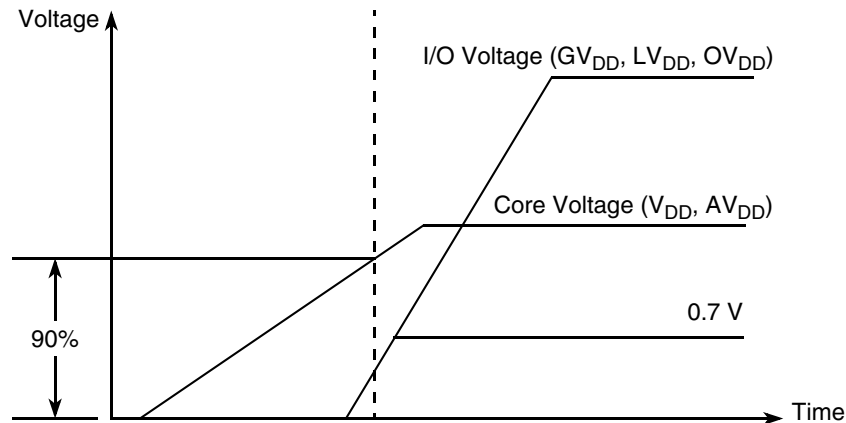


Figure 4. Power Sequencing Example

I/O voltage supplies (GV_{DD} , LV_{DD} , and OV_{DD}) do not have any ordering requirements with respect to one another.

3 Power Characteristics

The estimated typical power dissipation for the MPC8349EA device is shown in Table 4.

Table 4. MPC8349EA Power Dissipation¹

	Core Frequency (MHz)	CSB Frequency (MHz)	Typical at $T_J = 65$	Typical ^{2, 3}	Maximum ⁴	Unit
TBGA	333	333	2.0	3.0	3.2	W
		166	1.8	2.8	2.9	W
	400	266	2.1	3.0	3.3	W
		133	1.9	2.9	3.1	W
	450	300	2.3	3.2	3.5	W
		150	2.1	3.0	3.2	W
	500	333	2.4	3.3	3.6	W
		166	2.2	3.1	3.4	W
	533	266	2.4	3.3	3.6	W
		133	2.2	3.1	3.4	W
	667 ^{5, 6}	333	3.5	4.6	5	W

¹ The values do not include I/O supply power (OV_{DD} , LV_{DD} , GV_{DD}) or AV_{DD} . For I/O power values, see Table 5.

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) $\pm$ 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
ADDR/CMD/MODT output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAS}	1.95 2.40 3.15 4.20	— — — —	ns	3
ADDR/CMD/MODT output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHAX}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output setup with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHCS}	1.95 2.40 3.15 4.20	— — — —	ns	3
$\overline{MCS}(n)$ output hold with respect to MCK 400 MHz 333 MHz 266 MHz 200 MHz	$t_{DDKHCSX}$	1.95 2.40 3.15 4.20	— — — —	ns	3
MCK to MDQS Skew	t_{DDKMH}	−0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHDS} , t_{DDKLDS}	700 775 1100 1200	— — — —	ps	5
MDQ/MECC/MDM output hold with respect to MDQS 400 MHz 333 MHz 266 MHz 200 MHz	t_{DDKHDX} , t_{DDKLDX}	700 900 1100 1200	— — — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6

8.1.1 TSEC DC Electrical Characteristics

GMII, MII, TBI, RGMII, and RTBI drivers and receivers comply with the DC parametric attributes specified in Table 23 and Table 24. The RGMII and RTBI signals in Table 24 are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 23. GMII/TBI and MII DC Electrical Characteristics

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage 3.3 V	LV_{DD}^2	—		2.97	3.63	V
Output high voltage	V_{OH}	$I_{OH} = -4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.40	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$	$LV_{DD} = \text{Min}$	GND	0.50	V
Input high voltage	V_{IH}	—	—	2.0	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	—	-0.3	0.90	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	40	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-600	—	μA

Notes:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.
2. GMII/MI pins not needed for RGMII or RTBI operation are powered by the OV_{DD} supply.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics

Parameters	Symbol	Conditions		Min	Max	Unit
Supply voltage 2.5 V	LV_{DD}	—		2.37	2.63	V
Output high voltage	V_{OH}	$I_{OH} = -1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	2.00	$LV_{DD} + 0.3$	V
Output low voltage	V_{OL}	$I_{OL} = 1.0 \text{ mA}$	$LV_{DD} = \text{Min}$	$\text{GND} - 0.3$	0.40	V
Input high voltage	V_{IH}	—	$LV_{DD} = \text{Min}$	1.7	$LV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	$LV_{DD} = \text{Min}$	-0.3	0.70	V
Input high current	I_{IH}	$V_{IN}^1 = LV_{DD}$		—	10	μA
Input low current	I_{IL}	$V_{IN}^1 = \text{GND}$		-15	—	μA

Note:

1. The symbol V_{IN} , in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

8.2 GMII, MII, TBI, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for GMII, MII, TBI, RGMII, and RTBI are presented in this section.

8.2.1 GMII Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications (continued)At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns

Note:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 provides the AC test load for TSEC.

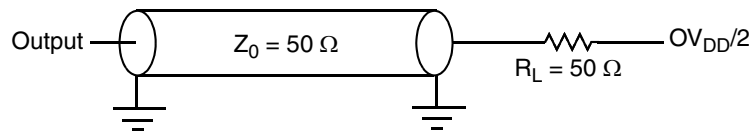
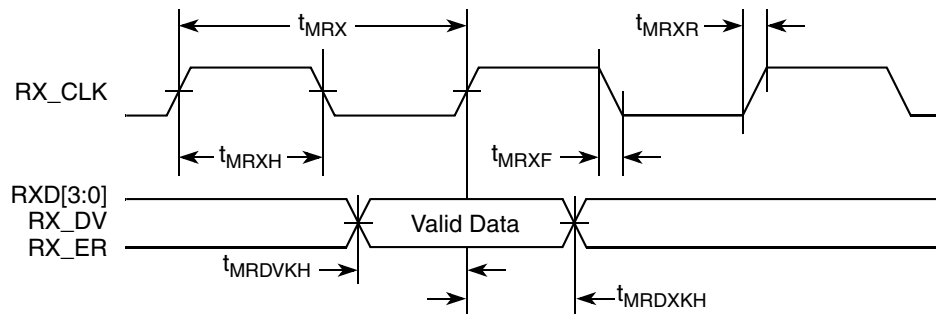
**Figure 12. TSEC AC Test Load**

Figure 13 shows the MII receive AC timing diagram.

**Figure 13. MII Receive AC Timing Diagram**

8.2.3 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

8.2.3.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
GTX_CLK clock period	t_{TTX}	—	8.0	—	ns
GTX_CLK duty cycle	t_{TTXH}/t_{TTX}	40	—	60	%
GTX_CLK to TBI data TXD[7:0], TX_ER, TX_EN delay	t_{TTKHDX}	1.0	—	5.0	ns
GTX_CLK clock rise (20%–80%)	t_{TTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t_{TTXF}	—	—	1.0	ns

Notes:

- The symbols for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 14 shows the TBI transmit AC timing diagram.

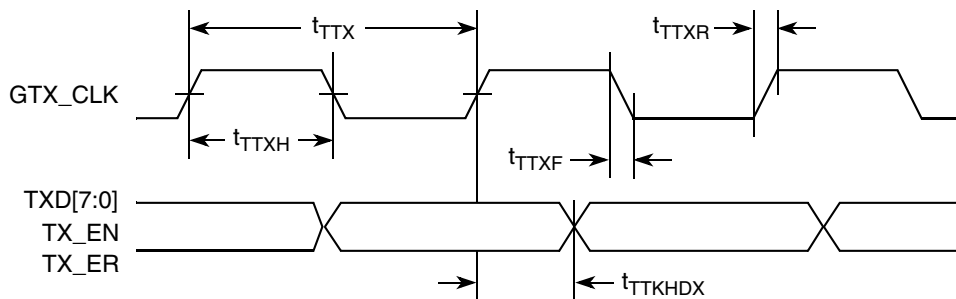


Figure 14. TBI Transmit AC Timing Diagram

8.2.3.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
PMA_RX_CLK clock period	t_{TRX}		16.0		ns
PMA_RX_CLK skew	t_{SKTRX}	7.5	—	8.5	ns
RX_CLK duty cycle	t_{TRXH}/t_{TRX}	40	—	60	%

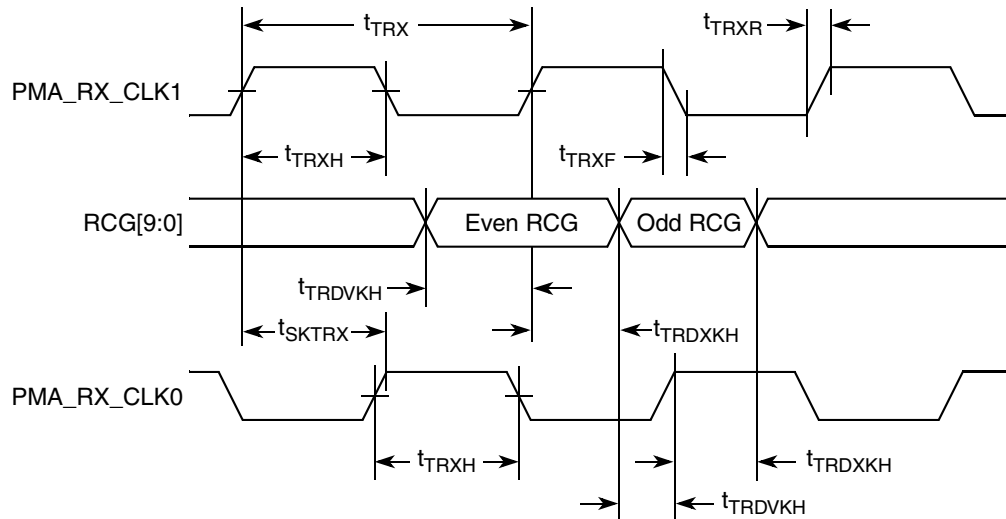
Table 30. TBI Receive AC Timing Specifications (continued)At recommended operating conditions with V_{DD}/OV_{DD} of $3.3\text{ V} \pm 10\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t_{TRDVKH}^2	2.5	—	—	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t_{TRDXKH}^2	1.5	—	—	ns
RX_CLK clock rise time (20%–80%)	t_{TRXR}	0.7	—	2.4	ns
RX_CLK clock fall time (80%–20%)	t_{TRXF}	0.7	—	2.4	ns

Notes:

- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{TRDVKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{TRX} clock reference (K) going to the high (H) state or setup time. Also, t_{TRDXKH} symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t_{TRX} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{TRX} represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
- Setup and hold time of even numbered RCG are measured from the rising edge of PMA_RX_CLK1. Setup and hold times of odd-numbered RCG are measured from the rising edge of PMA_RX_CLK0.

Figure 15 shows the TBI receive AC timing diagram.

**Figure 15. TBI Receive AC Timing Diagram**

8.2.4 RGMII and RTBI AC Timing Specifications

Table 31 presents the RGMII and RTBI AC timing specifications.

Table 31. RGMII and RTBI AC Timing Specifications

At recommended operating conditions with LV_{DD} of $2.5\text{ V} \pm 5\%$.

Parameter/Condition	Symbol ¹	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ²	t_{SKRGT}	1.0	—	2.8	ns
Clock cycle duration ³	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T ^{4, 5}	t_{RGTH}/t_{RGTF}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX ^{3, 5}	t_{RGTH}/t_{RGTF}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (80%–20%)	t_{RGTF}	—	—	0.75	ns

Notes:

1. In general, the clock reference symbol for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Also, the notation for rise (R) and fall (F) times follows the clock symbol. For symbols representing skews, the subscript is SK followed by the clock being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to $400\text{ ns} \pm 40\text{ ns}$ and $40\text{ ns} \pm 4\text{ ns}$, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned.
5. Duty cycle reference is $LV_{DD}/2$.

9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8349EA.

9.1 USB DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the USB interface.

Table 35. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	$OV_{DD} + 0.3$	V
Low-level input voltage	V_{IL}	-0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, $I_{OH} = -100 \mu A$	V_{OH}	$OV_{DD} - 0.2$	—	V
Low-level output voltage, $I_{OL} = 100 \mu A$	V_{OL}	—	0.2	V

9.2 USB AC Electrical Specifications

Table 36 describes the general timing parameters of the USB interface of the MPC8349EA.

Table 36. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol ¹	Min	Max	Unit	Notes
USB clock cycle time	t_{USCK}	15	—	ns	2–5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2–5
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2–5
USB clock to output valid—all outputs	$t_{USKH OV}$	—	7	ns	2–5
Output hold from USB clock—all outputs	$t_{USKH OX}$	2	—	ns	2–5

Notes:

1. The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, $t_{USKH OX}$ symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from $OV_{DD}/2$ of the rising edge of the USB clock to $0.4 \times OV_{DD}$ of the signal in question for 3.3 V signaling levels.
4. Input timings are measured at the pin.
5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

Figure 21 through Figure 26 show the local bus signals.

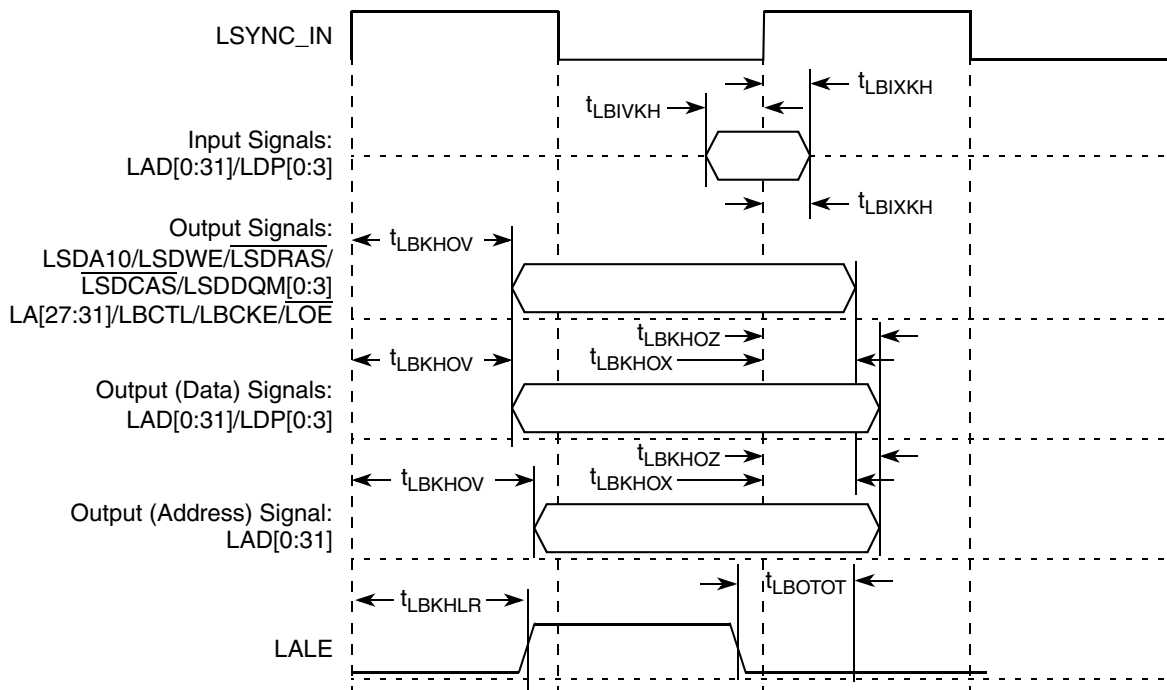


Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)

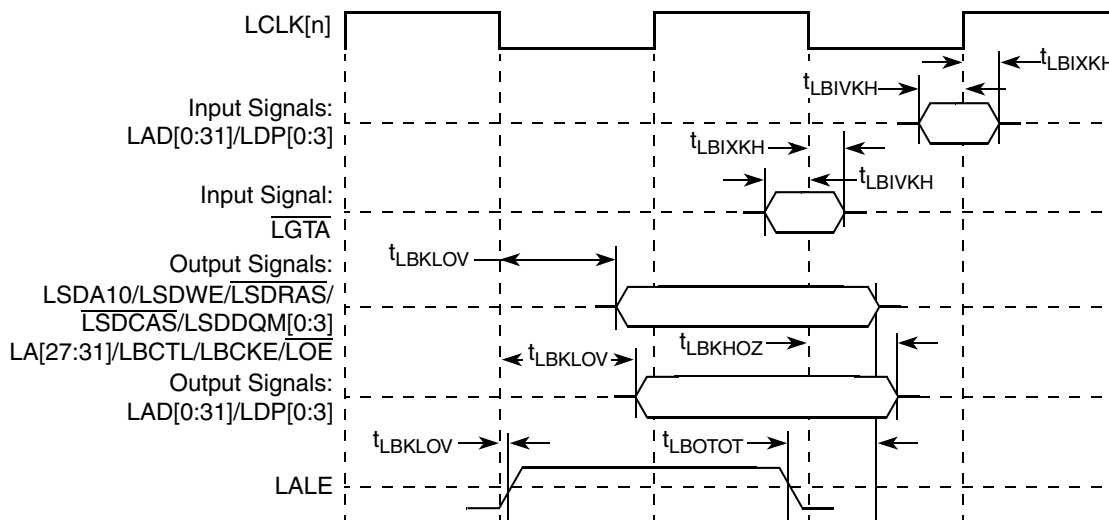


Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)¹ (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t_{JTKLDZ} t_{JTKLOZ}	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50 Ω load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{JTDVXH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDVXH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK} .
5. Non-JTAG signal output timing with respect to t_{TCLK} .
6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8349EA.

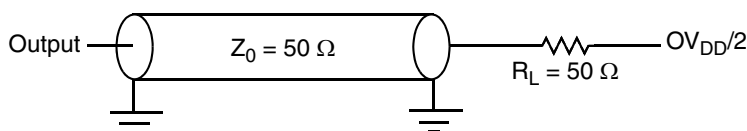
**Figure 27. AC Test Load for the JTAG Interface**

Figure 28 provides the JTAG clock input timing diagram.

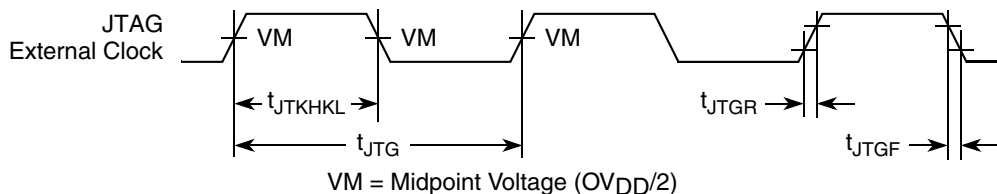
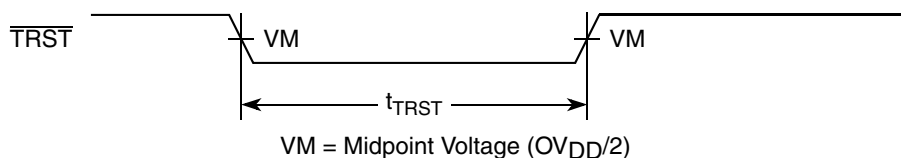
**Figure 28. JTAG Clock Input Timing Diagram**

Figure 29 provides the $\overline{TRST}$ timing diagram.

**Figure 29. $\overline{TRST}$ Timing Diagram**

17 SPI

This section describes the SPI DC and AC electrical specifications.

17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.0	$OV_{DD} + 0.3$	V
Input low voltage	V_{IL}	—	−0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	$I_{OH} = -8.0$ mA	2.4	—	V
Output low voltage	V_{OL}	$I_{OL} = 8.0$ mA	—	0.5	V
Output low voltage	V_{OL}	$I_{OL} = 3.2$ mA	—	0.4	V

17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

Table 54. SPI AC Timing Specifications¹

Parameter	Symbol ²	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	$t_{NIKH OV}$	—	6	ns
SPI outputs hold—Master mode (internal clock) delay	$t_{NIKH OX}$	0.5	—	ns
SPI outputs valid—Slave mode (external clock) delay	$t_{NEKH OV}$	—	8	ns
SPI outputs hold—Slave mode (external clock) delay	$t_{NEKH OX}$	2	—	ns
SPI inputs—Master mode (internal clock input setup time)	$t_{NIIV KH}$	4	—	ns
SPI inputs—Master mode (internal clock input hold time)	$t_{NIIX KH}$	0	—	ns
SPI inputs—Slave mode (external clock) input setup time	$t_{NEIV KH}$	4	—	ns
SPI inputs—Slave mode (external clock) input hold time	$t_{NEIX KH}$	2	—	ns

Notes:

- Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.
- The symbols for timing specifications follow the pattern of $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, $t_{NIKH OX}$ symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GPIO1[2]/DMA_DDONE0/ GTM1_TOUT1	B25	I/O	OV _{DD}	—
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV _{DD}	—
GPIO1[4]/DMA_DACK1/ GTM1_TGATE2/GTM2_TGATE1	A25	I/O	OV _{DD}	—
GPIO1[5]/DMA_DDONE1/ GTM1_TOUT2/GTM2_TOUT1	B24	I/O	OV _{DD}	—
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV _{DD}	—
GPIO1[7]/DMA_DACK2/ GTM1_TGATE3/GTM2_TGATE4	D23	I/O	OV _{DD}	—
GPIO1[8]/DMA_DDONE2/ GTM1_TOUT3	B23	I/O	OV _{DD}	—
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV _{DD}	—
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	F22	I/O	OV _{DD}	—
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	E22	I/O	OV _{DD}	—
USB Port 1				
MPH1_D0_ENABLEN/ DR_D0_ENABLEN	A26	I/O	OV _{DD}	—
MPH1_D1_SER_TXD/ DR_D1_SER_TXD	B26	I/O	OV _{DD}	—
MPH1_D2_VMO_SE0/ DR_D2_VMO_SE0	D25	I/O	OV _{DD}	—
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV _{DD}	—
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV _{DD}	—
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV _{DD}	—
MPH1_D6_SER_RCV/ DR_D6_SER_RCV	D26	I/O	OV _{DD}	—
MPH1_D7_DRVVBUS/ DR_D7_DRVVBUS	E26	I/O	OV _{DD}	—
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV _{DD}	—
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV _{DD}	—
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	O	OV _{DD}	—

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
TDO	B20	O	OV _{DD}	3
TMS	A20	I	OV _{DD}	4
TRST	B19	I	OV _{DD}	4
Test				
TEST	D22	I	OV _{DD}	6
TEST_SEL	AL13	I	OV _{DD}	6
PMC				
QUIESCE	A18	O	OV _{DD}	—
System Control				
PORESET	C18	I	OV _{DD}	—
HRESET	B18	I/O	OV _{DD}	1
SRESET	D18	I/O	OV _{DD}	2
Thermal Management				
THERM0	K32	I	—	8
Power and Ground Signals				
AV _{DD1}	L31	Power for e300 PLL (1.2 V nominal, 1.3 V for 667 MHz)	AV _{DD1}	—
AV _{DD2}	AP12	Power for system PLL (1.2 V nominal, 1.3 V for 667 MHz)	AV _{DD2}	—
AV _{DD3}	AE1	Power for DDR DLL (1.2 V nominal, 1.3 V for 667 MHz)	—	—
AV _{DD4}	AJ13	Power for LBIU DLL (1.2 V nominal, 1.3 V for 667 MHz)	AV _{DD4}	—

As shown in [Figure 41](#), the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb_clk = \{PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)\} \times SPMF$$

In PCI host mode, $PCI_SYNC_IN \times (1 + CFG_CLKIN_DIV)$ is the CLKIN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL), which is loaded at power-on reset or by one of the hard-coded reset options. See the chapter on reset, clocking, and initialization in the *MPC8349EA Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr_clk = csb_clk \times (1 + RCWL[DDRCM])$$

ddr_clk is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider ($\div 2$) to create the differential DDR memory bus clock outputs (MCK and $\overline{MCK}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu_clk = csb_clk \times (1 + RCWL[LBIUCM])$$

lbiu_clk is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LSYNC_OUT and LCLK[0:2]). The LBIU clock divider ratio is controlled by LCCR[CLKDIV].

In addition, some of the internal units may have to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory-mapped register after the device exits reset. [Table 56](#) specifies which units have a configurable clock frequency.

Table 56. Configurable Clock Units

Unit	Default Frequency	Options
TSEC1	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
TSEC2, I ² C1	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
Security core	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
USB DR, USB MPH	<i>csb_clk</i> /3	Off, <i>csb_clk</i> , <i>csb_clk</i> /2, <i>csb_clk</i> /3
PCI1, PCI2 and DMA complex	<i>csb_clk</i>	Off, <i>csb_clk</i>

Table 61. e300 Core PLL Configuration

RCWL[COREPLL]			<i>core_clk</i> : <i>csb_clk</i> Ratio	VCO Divider ¹
0–1	2–5	6		
nn	0000	n	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)	PLL bypassed (PLL off, <i>csb_clk</i> clocks core directly)
00	0001	0	1:1	2
01	0001	0	1:1	4
10	0001	0	1:1	8
11	0001	0	1:1	8
00	0001	1	1.5:1	2
01	0001	1	1.5:1	4
10	0001	1	1.5:1	8
11	0001	1	1.5:1	8
00	0010	0	2:1	2
01	0010	0	2:1	4
10	0010	0	2:1	8
11	0010	0	2:1	8
00	0010	1	2.5:1	2
01	0010	1	2.5:1	4
10	0010	1	2.5:1	8
11	0010	1	2.5:1	8
00	0011	0	3:1	2
01	0011	0	3:1	4
10	0011	0	3:1	8
11	0011	0	3:1	8

¹ Core VCO frequency = core frequency × VCO divider. The VCO divider must be set properly so that the core VCO frequency is in the range of 800–1800 MHz.

19.3 Suggested PLL Configurations

Table 62 shows suggested PLL configurations for 33 and 66 MHz input clocks.

Table 62. Suggested PLL Configurations

Ref No. ¹	RCWL		400 MHz Device			533 MHz Device			667 MHz Device		
	SPMF	CORE PLL	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)	Input Clock Freq (MHz) ²	CSB Freq (MHz)	Core Freq (MHz)
33 MHz CLKIN/PCI_CLK Options											
922	1001	0100010	—	—	—	—	—	f300	33	300	300
723	0111	0100011	33	233	350	33	233	350	33	233	350
604	0110	0000100	33	200	400	33	200	400	33	200	400
624	0110	0100100	33	200	400	33	200	400	33	200	400
803	1000	0000011	33	266	400	33	266	400	33	266	400
823	1000	0100011	33	266	400	33	266	400	33	266	400
903	1001	0000011	—			33	300	450	33	300	450
923	1001	0100011	—			33	300	450	33	300	450
704	0111	0000011	—			33	233	466	33	233	466
724	0111	0100011	—			33	233	466	33	233	466
A03	1010	0000011	—			33	333	500	33	333	500
804	1000	0000100	—			33	266	533	33	266	533
705	0111	0000101	—			—			33	233	583
606	0110	0000110	—			—			33	200	600
904	1001	0000100	—			—			33	300	600
805	1000	0000101	—			—			33	266	667
A04	1010	0000100	—			—			33	333	667
66 MHz CLKIN/PCI_CLK Options											
304	0011	0000100	66	200	400	66	200	400	66	200	400
324	0011	0100100	66	200	400	66	200	400	66	200	400
403	0100	0000011	66	266	400	66	266	400	66	266	400
423	0100	0100011	66	266	400	66	266	400	66	266	400
305	0011	0000101	—			66	200	500	66	200	500
503	0101	0000011	—			66	333	500	66	333	500
404	0100	0000100	—			66	266	533	66	266	533

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20.3 Heat Sink Attachment

When heat sinks are attached, an interface material is required, preferably thermal grease and a spring clip. The spring clip should connect to the printed-circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces that can lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. The recommended maximum force on the top of the package is 10 lb force (4.5 kg force). Any adhesive attachment should attach to painted or plastic surfaces, and its performance should be verified under the application requirements.

20.3.1 Experimental Determination of the Junction Temperature with a Heat Sink

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimize the size of the clearance to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

$$T_J = T_C + (R_{\theta JC} \times P_D)$$

where:

T_J = junction temperature (°C)

T_C = case temperature of the package (°C)

$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

P_D = power dissipation (W)

21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8349EA.

21.1 System Clocking

The MPC8349EA includes two PLLs:

1. The platform PLL generates the platform clock from the externally supplied CLKIN input. The frequency ratio between the platform and CLKIN is selected using the platform PLL ratio configuration bits as described in [Section 19.1, “System PLL Configuration.”](#)

$V_2 = (1 \div (1/R_1 + 1/R_2)) \times I_{\text{source}}$. Solving for the output impedance gives $R_{\text{source}} = R_{\text{term}} \times (V_1 \div V_2 - 1)$. The drive current is then $I_{\text{source}} = V_1 \div R_{\text{source}}$.

Table 65 summarizes the signal impedance targets. The driver impedance are targeted at minimum V_{DD} , nominal OV_{DD} , 105°C.

Table 65. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (Not Including PCI Output Clocks)	PCI Output Clocks (Including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	W
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	W
Differential	NA	NA	NA	NA	Z_{DIFF}	W

Note: Nominal supply voltages. See Table 1, $T_j = 105^\circ\text{C}$.

21.6 Configuration Pin Multiplexing

The MPC8349EA power-on configuration options can be set through external pull-up or pull-down resistors of 4.7 k Ω on certain output pins (see the customer-visible configuration pins). These pins are used as output only pins in normal operation.

However, while $\overline{\text{HRESET}}$ is asserted, these pins are treated as inputs, and the value on these pins is latched when $\overline{\text{PORESET}}$ deasserts. Then the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for the output pins.

21.7 Pull-Up Resistor Requirements

The MPC8349EA requires high resistance pull-up resistors (10 k Ω is recommended) on open-drain pins, including I²C pins, and IPIC interrupt pins.

For more information on required pull-up resistors and the connections required for the JTAG interface, refer to application note AN2931, “PowerQUICC Design Checklist.”

22 Ordering Information

This section presents ordering information for the device discussed in this document, and it shows an example of how the parts are marked.

NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications* (Document Order No. MPC8349EEC).

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