

MPC8349E

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#### **Understanding Embedded - Microprocessors**

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

#### Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	PowerPC e300
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	672-LBGA
Supplier Device Package	672-LBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8349zuagd

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### NOTE

The information in this document is accurate for revision 3.x silicon and later (in other words, for orderable part numbers ending in A or B). For information on revision 1.1 silicon and earlier versions, see the *MPC8349E PowerQUICC II Pro Integrated Host Processor Hardware Specifications*.

See Section 22.1, "Part Numbers Fully Addressed by This Document," for silicon revision level determination.

# 1 Overview

This section provides a high-level overview of the device features. Figure 1 shows the major functional units within the MPC8349EA.



Figure 1. MPC8349EA Block Diagram

Major features of the device are as follows:

- Embedded PowerPC e300 processor core; operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the other Freescale processor families that implement Power Architecture technology

# 4 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the device.

## 4.1 DC Electrical Characteristics

Table 6 provides the clock input (CLKIN/PCI\_SYNC\_IN) DC timing specifications for the MPC8349EA.

Parameter	Condition	Symbol	Min	Мах	Unit
Input high voltage	_	V <sub>IH</sub>	2.7	OV <sub>DD</sub> + 0.3	V
Input low voltage	_	V <sub>IL</sub>	-0.3	0.4	V
CLKIN input current	$0~V \leq V_{IN} \leq OV_{DD}$	I <sub>IN</sub>	—	±10	μA
PCI_SYNC_IN input current	$\begin{array}{c} 0 \text{ V} \leq \text{V}_{\text{IN}} \leq 0.5 \text{ V or} \\ \text{OV}_{\text{DD}} - 0.5 \text{ V} \leq \text{V}_{\text{IN}} \leq \text{OV}_{\text{DD}} \end{array}$	I <sub>IN</sub>	_	±10	μA
PCI_SYNC_IN input current	$0.5~V \leq V_{IN} \leq OV_{DD} - 0.5~V$	I <sub>IN</sub>	—	±50	μA

Table 6. CLKIN DC Timing Specifications

## 4.2 AC Electrical Characteristics

The primary clock source for the MPC8349EA can be one of two inputs, CLKIN or PCI\_CLK, depending on whether the device is configured in PCI host or PCI agent mode. Table 7 provides the clock input (CLKIN/PCI\_CLK) AC timing specifications for the device.

**Table 7. CLKIN AC Timing Specifications** 

Parameter/Condition	Symbol	Min	Typical	Мах	Unit	Notes
CLKIN/PCI_CLK frequency	f <sub>CLKIN</sub>	—	—	66	MHz	1, 6
CLKIN/PCI_CLK cycle time	t <sub>CLKIN</sub>	15	—	—	ns	—
CLKIN/PCI_CLK rise and fall time	t <sub>KH</sub> , t <sub>KL</sub>	0.6	1.0	2.3	ns	2
CLKIN/PCI_CLK duty cycle	t <sub>KHK</sub> /t <sub>CLKIN</sub>	40	—	60	%	3
CLKIN/PCI_CLK jitter	_	—	—	±150	ps	4, 5

Notes:

1. Caution: The system, core, USB, security, and TSEC must not exceed their respective maximum or minimum operating frequencies.

- 2. Rise and fall times for CLKIN/PCI\_CLK are measured at 0.4 and 2.7 V.
- 3. Timing is guaranteed by design and characterization.
- 4. This represents the total input jitter—short term and long term—and is guaranteed by design.
- 5. The CLKIN/PCI\_CLK driver's closed loop jitter bandwidth should be < 500 kHz at -20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track CLKIN drivers with the specified jitter.
- 6. Spread spectrum clocking is allowed with 1% input frequency down-spread at maximum 50 KHz modulation rate regardless of input frequency.

#### **RESET** Initialization

#### Table 9. RESET Pins DC Electrical Characteristics<sup>1</sup> (continued)

Parameter	Symbol	Condition	Min	Мах	Unit
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V

Notes:

1. This table applies for pins PORESET, HRESET, SRESET, and QUIESCE.

2. HRESET and SRESET are open drain pins, thus V<sub>OH</sub> is not relevant for those pins.

### 5.2 **RESET AC Electrical Characteristics**

Table 10 provides the reset initialization AC timing specifications of the MPC8349EA.

#### Table 10. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit	Natas
Parameter	IVIIII	max	Unit	notes
Required assertion time of HRESET or SRESET (input) to activate reset flow	32	_	t <sub>PCI_SYNC_IN</sub>	1
Required assertion time of $\overrightarrow{\text{PORESET}}$ with stable clock applied to CLKIN when the MPC8349EA is in PCI host mode	32	—	t <sub>CLKIN</sub>	2
Required assertion time of PORESET with stable clock applied to PCI_SYNC_IN when the MPC8349EA is in PCI agent mode	32	—	t <sub>PCI_SYNC_IN</sub>	1
HRESET/SRESET assertion (output)	512	—	t <sub>PCI_SYNC_IN</sub>	1
HRESET negation to SRESET negation (output)	16	—	t <sub>PCI_SYNC_IN</sub>	1
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8349EA is in PCI host mode	4	_	t <sub>CLKIN</sub>	2
Input setup time for POR configuration signals (CFG_RESET_SOURCE[0:2] and CFG_CLKIN_DIV) with respect to negation of PORESET when the MPC8349EA is in PCI agent mode	4	_	tpci_sync_in	1
Input hold time for POR configuration signals with respect to negation of HRESET	0	—	ns	—
Time for the MPC8349EA to turn off POR configuration signals with respect to the assertion of $\overrightarrow{\text{HRESET}}$	_	4	ns	3
Time for the MPC8349EA to turn on POR configuration signals with respect to the negation of HRESET	1	—	t <sub>PCI_SYNC_IN</sub>	1, 3

Notes:

1. t<sub>PCI\_SYNC\_IN</sub> is the clock period of the input clock applied to PCI\_SYNC\_IN. In PCI host mode, the primary clock is applied to the CLKIN input, and PCI\_SYNC\_IN period depends on the value of CFG\_CLKIN\_DIV. See the *MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.

2. t<sub>CLKIN</sub> is the clock period of the input clock applied to CLKIN. It is valid only in PCI host mode. See the MPC8349EA PowerQUICC II Pro Integrated Host Processor Family Reference Manual.

3. POR configuration signals consist of CFG\_RESET\_SOURCE[0:2] and CFG\_CLKIN\_DIV.

Table 15 provides the DDR capacitance when  $GV_{DD}(typ) = 2.5$  V.

Table 15. DDR SDRAM Capacitance for GV<sub>DD</sub>(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C <sub>IO</sub>	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C <sub>DIO</sub>	_	0.5	pF	1

Note:

1. This parameter is sampled.  $GV_{DD} = 2.5 V \pm 0.125 V$ , f = 1 MHz,  $T_A = 25^{\circ}C$ ,  $V_{OUT} = GV_{DD}/2$ ,  $V_{OUT}$  (peak-to-peak) = 0.2 V.

#### Table 16 provides the current draw characteristics for MV<sub>REF</sub>.

Table 16. Current Draw Characteristics for MV<sub>REF</sub>

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV <sub>REF</sub>	I <sub>MVREF</sub>		500	μA	1

#### Note:

1. The voltage regulator for  $\text{MV}_{\text{REF}}$  must supply up to 500  $\mu\text{A}$  current.

### 6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

### 6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when  $GV_{DD}(typ) = 1.8 \text{ V}$ .

#### Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with  $GV_{DD}$  of 1.8 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V <sub>IL</sub>	_	MV <sub>REF</sub> – 0.25	V	_
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.25	—	V	_

Table 18 provides the input AC timing specifications for the DDR SDRAM when  $GV_{DD}(typ) = 2.5 \text{ V}$ .

#### Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with  $GV_{DD}$  of 2.5 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V <sub>IL</sub>	—	MV <sub>REF</sub> – 0.31	V	—
AC input high voltage	V <sub>IH</sub>	MV <sub>REF</sub> + 0.31	—	V	—

#### DDR and DDR2 SDRAM

#### Table 19 provides the input AC timing specifications for the DDR SDRAM interface.

#### Table 19. DDR and DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with  $GV_{DD}$  of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM	t <sub>CISKEW</sub>			ps	1, 2
400 MHz		-600	600		3
333 MHz		-750	750		—
266 MHz		-750	750		—
200 MHz		-750	750		—

Notes:

1. t<sub>CISKEW</sub> represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that will be captured with MDQS[n]. This should be subtracted from the total timing budget.

- The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t<sub>DISKEW</sub>. This can be determined by the equation: t<sub>DISKEW</sub> = ± (T/4 – abs (t<sub>CISKEW</sub>)); where T is the clock period and abs (t<sub>CISKEW</sub>) is the absolute value of t<sub>CISKEW</sub>.
- 3. This specification applies only to the DDR interface.

Figure 5 illustrates the DDR input timing diagram showing the t<sub>DISKEW</sub> timing parameter.



Figure 5. DDR Input Timing Diagram

Parameter	Symbol	Min	Мах	Unit
High-level output voltage, $I_{OH} = -100 \ \mu A$	V <sub>OH</sub>	OV <sub>DD</sub> - 0.2	-	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V <sub>OL</sub>	—	0.2	V

## 7.2 DUART AC Electrical Specifications

Table 22 provides the AC timing parameters for the DUART interface of the MPC8349EA.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	256	baud	_
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16		2

Notes:

1. Actual attainable baud rate will be limited by the latency of interrupt processing.

2. The middle of a start bit is detected as the 8<sup>th</sup> sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16<sup>th</sup> sample.

# 8 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speeds (10/100/1000 Mbps) and MII management.

### 8.1 Three-Speed Ethernet Controller (TSEC)—GMII/MII/TBI/RGMII/RTBI Electrical Characteristics

The electrical characteristics specified here apply to gigabit media independent interface (GMII), the media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), and reduced ten-bit interface (RTBI) signals except management data input/output (MDIO) and management data clock (MDC). The MII, GMII, and TBI interfaces are defined for 3.3 V, and the RGMII and RTBI interfaces are defined for 2.5 V. The RGMII and RTBI interfaces follow the Hewlett-Packard *Reduced Pin-Count Interface for Gigabit Ethernet Physical Layer Device Specification*, Version 1.2a (9/22/2000). The electrical characteristics for MDIO and MDC are specified in Section 8.3, "Ethernet Management Interface Electrical Characteristics."

### 8.2.1.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

#### Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V ± 10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Мах	Unit
GTX_CLK clock period	t <sub>GTX</sub>	—	8.0	—	ns
GTX_CLK duty cycle	t <sub>GTXH</sub> /t <sub>GTX</sub>	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	<sup>t</sup> GTKHDX	0.5	—	5.0	ns
GTX_CLK clock rise time (20%-80%)	t <sub>GTXR</sub>	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t <sub>GTXF</sub>		_	1.0	ns

#### Notes:

1. The symbols for timing specifications follow the pattern t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>GTKHDV</sub> symbolizes GMII transmit timing (GT) with respect to the t<sub>GTX</sub> clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t<sub>GTKHDX</sub> symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the clock reference (K) going to the high state (H) relative to the time date input signals (D) with respect to the t<sub>GTX</sub> clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t<sub>GTX</sub> represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

#### Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

### 8.2.1.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

#### Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV\_DD/OV\_DD of 3.3 V  $\pm$  10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
RX_CLK clock period	t <sub>GRX</sub>	_	8.0	_	ns
RX_CLK duty cycle	t <sub>GRXH</sub> /t <sub>GRX</sub>	40	_	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t <sub>GRDVKH</sub>	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t <sub>GRDXKH</sub>	0.5	_	_	ns

#### Table 30. TBI Receive AC Timing Specifications (continued)

At recommended operating conditions with  $LV_{DD}/OV_{DD}$  of 3.3 V  $\pm$  10%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) setup time to rising PMA_RX_CLK	t <sub>TRDVKH</sub> 2	2.5	—	_	ns
RXD[7:0], RX_DV, RX_ER (RCG[9:0]) hold time to rising PMA_RX_CLK	t <sub>тRDXKH</sub> <sup>2</sup>	1.5	—	_	ns
RX_CLK clock rise time (20%–80%)	t <sub>TRXR</sub>	0.7	—	2.4	ns
RX_CLK clock fall time (80%-20%)	t <sub>TRXF</sub>	0.7	_	2.4	ns

Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>TRDVKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>TRDXKH</sub> symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>TRX</sub> clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t<sub>TRX</sub> represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript SK followed by the clock that is being skewed (TRX).
</sub>

2. Setup and hold time of even numbered RCG are measured from the riding edge of PMA\_RX\_CLK1. Setup and hold times of odd-numbered RCG are measured from the riding edge of PMA\_RX\_CLK0.

#### Figure 15 shows the TBI receive AC timing diagram.



Figure 15. TBI Receive AC Timing Diagram

#### Table 34. MII Management AC Timing Specifications (continued)

At recommended operating conditions with  $LV_{DD}$  is 3.3 V ± 10% or 2.5 V ± 5%.

Parameter/Condition	Symbol <sup>1</sup>	Min	Тур	Max	Unit	Notes
MDC fall time	t <sub>MDHF</sub>	_	_	10	ns	

#### Notes:

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>MDKHDX</sub> symbolizes management data timing (MD) for the time t<sub>MDC</sub> from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t<sub>MDDVKH</sub> symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t<sub>MDC</sub> clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub>

- 2. This parameter is dependent on the csb\_clk speed (that is, for a csb\_clk of 267 MHz, the maximum frequency is 8.3 MHz and the minimum frequency is 1.2 MHz; for a csb\_clk of 375 MHz, the maximum frequency is 11.7 MHz and the minimum frequency is 1.7 MHz).
- 3. This parameter is dependent on the csb\_clk speed (that is, for a csb\_clk of 267 MHz, the delay is 70 ns and for a csb\_clk of 333 MHz, the delay is 58 ns).

#### Figure 17 shows the MII management AC timing diagram.



Figure 17. MII Management Interface Timing Diagram

USB

# 9 USB

This section provides the AC and DC electrical specifications for the USB interface of the MPC8349EA.

## 9.1 USB DC Electrical Characteristics

Table 35 provides the DC electrical characteristics for the USB interface.

Table 35. USB	<b>DC Electrical</b>	Characteristics
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Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V <sub>IH</sub>	2	OV <sub>DD</sub> + 0.3	V
Low-level input voltage	V <sub>IL</sub>	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	±5	μA
High-level output voltage, $I_{OH} = -100 \ \mu A$	V <sub>OH</sub>	OV <sub>DD</sub> - 0.2	—	V
Low-level output voltage, $I_{OL} = 100 \ \mu A$	V <sub>OL</sub>	_	0.2	V

## 9.2 USB AC Electrical Specifications

Table 36 describes the general timing parameters of the USB interface of the MPC8349EA.

Table 36. USB General Timing Parameters (ULPI Mode Only)

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
USB clock cycle time	t <sub>USCK</sub>	15		ns	2–5
Input setup to USB clock—all inputs	t <sub>USIVKH</sub>	4	-	ns	2–5
Input hold to USB clock—all inputs	t <sub>USIXKH</sub>	1	-	ns	2–5
USB clock to output valid—all outputs	t <sub>USKHOV</sub>	—	7	ns	2–5
Output hold from USB clock—all outputs	t <sub>USKHOX</sub>	2	_	ns	2–5

Notes:

 The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state)</sub> for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>USIXKH</sub> symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t<sub>USKHOX</sub> symbolizes USB timing (US) for the USB clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to USB clock.

3. All signals are measured from  $OV_{DD}/2$  of the rising edge of the USB clock to  $0.4 \times OV_{DD}$  of the signal in question for 3.3 V signaling levels.

4. Input timings are measured at the pin.

5. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to that of the leakage current specification.

#### Local Bus

Figure 21 through Figure 26 show the local bus signals.



Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)



Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)

#### JTAG

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	_	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	_	0.4	V

#### Table 40. JTAG Interface DC Electrical Characteristics (continued)

### **11.2 JTAG AC Timing Specifications**

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA. Table 41 provides the JTAG AC timing specifications as defined in Figure 28 through Figure 31.

#### Table 41. JTAG AC Timing Specifications (Independent of CLKIN)<sup>1</sup>

At recommended operating conditions (see Table 2).

Parameter		Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock frequer	ncy of operation	f <sub>JTG</sub>	0	33.3	MHz	—
JTAG external clock cycle ti	me	t <sub>JTG</sub>	30	_	ns	—
JTAG external clock pulse w	vidth measured at 1.4 V	t <sub>JTKHKL</sub>	15	—	ns	—
JTAG external clock rise and	d fall times	t <sub>JTGR</sub> , t <sub>JTGF</sub>	0	2	ns	—
TRST assert time		t <sub>TRST</sub>	25	—	ns	3
Input setup times:	Boundary-scan data TMS, TDI	t <sub>JTDVKH</sub> t <sub>JTIVKH</sub>	4 4	_ _	ns	4
Input hold times:	Boundary-scan data TMS, TDI	t <sub>JTDXKH</sub> t <sub>JTIXKH</sub>	10 10		ns	4
Valid times:	Boundary-scan data TDO	t <sub>jtkldv</sub> t <sub>jtklov</sub>	2 2	11 11	ns	5
Output hold times:	Boundary-scan data TDO	t <sub>jtkldx</sub> t <sub>jtklox</sub>	2 2		ns	5

#### Table 41. JTAG AC Timing Specifications (Independent of CLKIN)<sup>1</sup> (continued)

At recommended operating conditions (see Table 2).

Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t <sub>JTKLDZ</sub> t <sub>JTKLOZ</sub>	2 2	19 9	ns	5, 6

Notes:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of  $t_{TCLK}$  to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50  $\Omega$  load (see Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.

2. The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>JTDVKH</sub> symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state or setup time. Also, t<sub>JTDXKH</sub> symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t<sub>JTG</sub> clock reference (K) going to the high (H) state. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).</sub>

3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.

4. Non-JTAG signal input timing with respect to t<sub>TCLK</sub>.

5. Non-JTAG signal output timing with respect to t<sub>TCLK</sub>.

6. Guaranteed by design and characterization.

Figure 27 provides the AC test load for TDO and the boundary-scan outputs of the MPC8349EA.



Figure 27. AC Test Load for the JTAG Interface

Figure 28 provides the JTAG clock input timing diagram.



Figure 28. JTAG Clock Input Timing Diagram

Figure 29 provides the  $\overline{\text{TRST}}$  timing diagram.



Table 45. PCI AC Timing Specifications at 66 MHz <sup>1</sup>	(continued)
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Parameter	Symbol <sup>2</sup>	Min	Max	Unit	Notes
PORESET to REQ64 hold time	t <sub>PCRHRX</sub>	0	50	ns	6

Notes:

- 1. PCI timing depends on M66EN and the ratio between PCI1/PCI2. Refer to the PCI chapter of the reference manual for a description of M66EN.
- 2. The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.</sub>
- 3. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.
- 4. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
- 5. Input timings are measured at the pin.
- 6. The setup and hold time is with respect to the rising edge of PORESET.

#### Table 46 provides the PCI AC timing specifications at 33 MHz.

#### Table 46. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol <sup>1</sup>	Min	Max	Unit	Notes
Clock to output valid	<sup>t</sup> PCKHOV	—	11	ns	2
Output hold from clock	t <sub>PCKHOX</sub>	2		ns	2
Clock to output high impedance	t <sub>PCKHOZ</sub>	—	14	ns	2, 3
Input setup to clock	t <sub>PCIVKH</sub>	3.0	-	ns	2, 4
Input hold from clock	t <sub>PCIXKH</sub>	0	_	ns	2, 4
REQ64 to PORESET setup time	t <sub>PCRVRH</sub>	5	_	clocks	5
PORESET to REQ64 hold time	t <sub>PCRHRX</sub>	0	50	ns	5

Notes:

2. See the timing measurement conditions in the PCI 2.3 Local Bus Specifications.

3. For active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

4. Input timings are measured at the pin.

5. The setup and hold time is with respect to the rising edge of PORESET.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)</sub>(reference)(state)(signal)(state) for outputs. For example, t<sub>PCIVKH</sub> symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI\_SYNC\_IN clock, t<sub>SYS</sub>, reference (K) going to the high (H) state or setup time. Also, t<sub>PCRHFV</sub> symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
</sub>

SPI

# 17 SPI

This section describes the SPI DC and AC electrical specifications.

## 17.1 SPI DC Electrical Characteristics

Table 53 provides the SPI DC electrical characteristics.

#### Table 53. SPI DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Мах	Unit
Input high voltage	V <sub>IH</sub>	—	2.0	OV <sub>DD</sub> + 0.3	V
Input low voltage	V <sub>IL</sub>	—	-0.3	0.8	V
Input current	I <sub>IN</sub>	—	—	±5	μA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -8.0 mA	2.4	—	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8.0 mA	—	0.5	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 3.2 mA	—	0.4	V

## 17.2 SPI AC Timing Specifications

Table 54 provides the SPI input and output AC timing specifications.

#### Table 54. SPI AC Timing Specifications<sup>1</sup>

Parameter	Symbol <sup>2</sup>	Min	Max	Unit
SPI outputs valid—Master mode (internal clock) delay	t <sub>NIKHOV</sub>	_	6	ns
SPI outputs hold—Master mode (internal clock) delay	t <sub>NIKHOX</sub>	0.5	_	ns
SPI outputs valid—Slave mode (external clock) delay	t <sub>NEKHOV</sub>	_	8	ns
SPI outputs hold—Slave mode (external clock) delay	t <sub>NEKHOX</sub>	2	_	ns
SPI inputs—Master mode (internal clock input setup time	t <sub>NIIVKH</sub>	4	_	ns
SPI inputs—Master mode (internal clock input hold time	t <sub>NIIXKH</sub>	0	_	ns
SPI inputs—Slave mode (external clock) input setup time	t <sub>NEIVKH</sub>	4	_	ns
SPI inputs—Slave mode (external clock) input hold time	t <sub>NEIXKH</sub>	2	_	ns

Notes:

1. Output specifications are measured from the 50 percent level of the rising edge of CLKIN to the 50 percent level of the signal. Timings are measured at the pin.

The symbols for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state)</sub> for outputs. For example, t<sub>NIKHOX</sub> symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).
</sub>

Figure 37 provides the AC test load for the SPI.



Figure 38 and Figure 39 represent the AC timings from Table 54. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 38 shows the SPI timings in slave mode (external clock).



Note: The clock edge is selectable on SPI.



Figure 39 shows the SPI timings in master mode (internal clock).



Figure 39. SPI AC Timing in Master Mode (Internal Clock) Diagram

# **18 Package and Pin Listings**

This section details package parameters, pin assignments, and dimensions. The MPC8349EA is available in a tape ball grid array (TBGA). See Section 18.1, "Package Parameters for the MPC8349EA TBGA" and Section 18.2, "Mechanical Dimensions for the MPC8349EA TBGA.

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes	
GPIO1[2]/DMA_DDONE0/ GTM1_TOUT1	B25	I/O	OV <sub>DD</sub>	_	
GPIO1[3]/DMA_DREQ1/GTM1_TIN2/ GTM2_TIN1	D24	I/O	OV <sub>DD</sub>	—	
GPIO1[4]/DMA_DACK1/ GTM1_TGATE2/GTM2_TGATE1	A25	I/O	OV <sub>DD</sub>	—	
GPIO1[5]/DMA_DDONE1/ GTM1_TOUT2/GTM2_TOUT1	B24	I/O	OV <sub>DD</sub>	—	
GPIO1[6]/DMA_DREQ2/GTM1_TIN3/ GTM2_TIN4	A24	I/O	OV <sub>DD</sub>	—	
GPIO1[7]/DMA_DACK2/ GTM1_TGATE3/GTM2_TGATE4	D23	I/O	OV <sub>DD</sub>	—	
GPIO1[8]/DMA_DDONE2/ GTM1_TOUT3	B23	I/O	OV <sub>DD</sub>	_	
GPIO1[9]/DMA_DREQ3/GTM1_TIN4/ GTM2_TIN3	A23	I/O	OV <sub>DD</sub>	—	
GPIO1[10]/DMA_DACK3/ GTM1_TGATE4/GTM2_TGATE3	F22	I/O	OV <sub>DD</sub>	—	
GPIO1[11]/DMA_DDONE3/ GTM1_TOUT4/GTM2_TOUT3	E22	I/O	OV <sub>DD</sub>	—	
USB Port 1					
MPH1_D0_ENABLEN/ DR_D0_ENABLEN	A26	I/O	OV <sub>DD</sub>	—	
MPH1_D1_SER_TXD/ DR_D1_SER_TXD	B26	I/O	OV <sub>DD</sub>	—	
MPH1_D2_VMO_SE0/ DR_D2_VMO_SE0	D25	I/O	OV <sub>DD</sub>	—	
MPH1_D3_SPEED/DR_D3_SPEED	A27	I/O	OV <sub>DD</sub>	—	
MPH1_D4_DP/DR_D4_DP	B27	I/O	OV <sub>DD</sub>	—	
MPH1_D5_DM/DR_D5_DM	C27	I/O	OV <sub>DD</sub>	—	
MPH1_D6_SER_RCV/ DR_D6_SER_RCV	D26	I/O	OV <sub>DD</sub>	—	
MPH1_D7_DRVVBUS/ DR_D7_DRVVBUS	E26	I/O	OV <sub>DD</sub>	_	
MPH1_NXT/DR_SESS_VLD_NXT	D27	I	OV <sub>DD</sub>	—	
MPH1_DIR_DPPULLUP/ DR_XCVR_SEL_DPPULLUP	A28	I/O	OV <sub>DD</sub>	—	
MPH1_STP_SUSPEND/ DR_STP_SUSPEND	F26	0	OV <sub>DD</sub>	—	

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
GND	A1, A34, C1, C7, C10, C11, C15, C23, C25, C28, D1, D8, D20, D30, E7, E13, E15, E17, E18, E21, E23, E25, E32, F6, F19, F27, F30, F34, G31, H5, J4, J34, K30, L5, M2, M5, M30, M33, N3, N5, P30, R5, R32, T5, T30, U6, U29, U33, V2, V5, V30, W6, W30, Y30, AA2, AA30, AB2, AB6, AB30, AC3, AC6, AD31, AE5, AF2, AF5, AF31, AG30, AG31, AH4, AJ3, AJ19, AJ22, AK7, AK13, AK14, AK16, AK18, AK20, AK25, AK28, AL3, AL5, AL10, AL12, AL22, AL27, AM1, AM6, AM7, AN12, AN17, AN34, AP1, AP8, AP34	_		_
GV <sub>DD</sub>	A2, E2, G5, G6, J5, K4, K5, L4, N4, P5, R6, T6, U5, V1, W5, Y5, AA4, AB3, AC4, AD5, AF3, AG5, AH2, AH5, AH6, AJ6, AK6, AK8, AK9, AL6	Power for DDR DRAM I/O voltage (2.5 V)	GV <sub>DD</sub>	—
LV <sub>DD1</sub>	C9, D11	Power for three speed Ethernet #1 and for Ethernet management interface I/O (2.5 V, 3.3 V)	LV <sub>DD1</sub>	
LV <sub>DD2</sub>	C6, D9	Power for three speed Ethernet #2 I/O (2.5 V, 3.3 V)	LV <sub>DD2</sub>	_
V <sub>DD</sub>	E19, E29, F7, F9, F11,F13, F15, F17, F18, F21, F23, F25, F29, H29, J6, K29, M29, N6, P29, T29, U30, V6, V29, W29, AB29, AC5, AD29, AF6, AF29, AH29, AJ8, AJ12, AJ14, AJ16, AJ18, AJ20, AJ21, AJ23, AJ25, AJ26, AJ27, AJ28, AJ29, AK10	Power for core (1.2 V nominal, 1.3 V for 667 MHz)	V <sub>DD</sub>	_
OV <sub>DD</sub>	B22, B28, C16, C17, C24, C26, D13, D15, D19, D29, E31, F28, G33, H30, L29, L32, N32, P31, R31, U32, W31, Y29, AA29, AC30, AE31, AF30, AG29, AJ17, AJ30, AK11, AL15, AL19, AL21, AL29, AL30, AM20, AM23, AM24, AM26, AM28, AN11, AN13	PCI, 10/100 Ethernet, and other standard (3.3 V)	OV <sub>DD</sub>	_
MVREF1	МЗ	I	DDR reference voltage	_

#### Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

#### Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MVREF2	AD2	I	DDR reference voltage	_

Notes:

1. This pin is an open-drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to OV<sub>DD</sub>.

2. This pin is an open-drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to OV<sub>DD</sub>.

3. During reset, this output is actively driven rather than three-stated.

4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.

5. This pin should have a weak pull-up if the chip is in PCI host mode. Follow the PCI specifications.

6. This pin must always be tied to GND.

7. This pin must always be left not connected.

8. Thermal sensitive resistor.

9. It is recommended that MDIC0 be tied to GND using an 18.2  $\Omega$  resistor and MDIC1 be tied to DDR power using an 18.2  $\Omega$  resistor.

10.TSEC1\_TXD[3] is required an external pull-up resistor. For proper functionality of the device, this pin must be pulled up or actively driven high during a hard reset. No external pull-down resistors are allowed to be attached to this net.

11. A weak pull-up resistor (2–10 k $\Omega$ ) should be placed on this pin to LV<sub>DD1</sub>.

12. For systems that boot from local bus (GPCM)-controlled NOR flash, a pullup on LGPL4 is required.

#### Thermal

(edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

 $T_J = T_A + (R_{\theta JA} \times P_D)$ 

where:

 $T_J$  = junction temperature (°C)

 $T_A$  = ambient temperature for the package (°C)

 $R_{\theta JA}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

### 20.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, use the thermal characterization parameter ( $\Psi_{JT}$ ) to determine the junction temperature and a measure of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

 $T_J$  = junction temperature (°C)

 $T_T$  = thermocouple temperature on top of package (°C)

 $\Psi_{JT}$  = junction-to-ambient thermal resistance (°C/W)

 $P_D$  = power dissipation in the package (W)

The thermal characterization parameter is measured per the JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

### 20.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

Some application environments require a heat sink to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$