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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Obsolete
PowerPC e300
1 Core, 32-Bit
533MHz
-
DDR, DDR2
No
-
10/100/1000Mbps (2)
-
USB 2.0 + PHY (2)
1.8V, 2.5V, 3.3V
0°C ~ 105°C (TA)
-
672-LBGA
672-LBGA (35x35)
https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8349zuajf

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Electrical Characteristics

2.1.2 Power Supply Voltage Specification

Table 2 provides the recommended operating conditions for the MPC8349EA. Note that the values in Table 2 are the recommended and tested operating conditions. Proper device operation outside these conditions is not guaranteed.

Parameter	Symbol	Recommended Value	Unit	Notes
Core supply voltage for 667-MHz core frequency	V _{DD}	1.3 V ± 60 mV	V	1
Core supply voltage	V _{DD}	1.2 V ± 60 mV	V	1
PLL supply voltage for 667-MHz core frequency	AV_{DD}	1.3 V ± 60 mV	V	1
PLL supply voltage	AV_{DD}	1.2 V ± 60 mV	V	1
DDR and DDR2 DRAM I/O voltage	GV _{DD}	2.5 V ± 125 mV 1.8 V ± 90 mV	V	—
Three-speed Ethernet I/O supply voltage	LV _{DD1}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	—
Three-speed Ethernet I/O supply voltage	LV _{DD2}	3.3 V ± 330 mV 2.5 V ± 125 mV	V	_
PCI, local bus, DUART, system control and power management, I ² C, and JTAG I/O voltage	OV _{DD}	3.3 V ± 330 mV	V	—

Table 2. Recommended C	Operating Co	nditions
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Note:

¹ GV_{DD}, LV_{DD}, OV_{DD}, AV_{DD}, and V_{DD} must track each other and must vary in the same direction—either in the positive or negative direction.

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8349EA.



Table 15 provides the DDR capacitance when $GV_{DD}(typ) = 2.5$ V.

Table 15. DDR SDRAM Capacitance for GV_{DD}(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C _{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C _{DIO}	_	0.5	pF	1

Note:

1. This parameter is sampled. $GV_{DD} = 2.5 V \pm 0.125 V$, f = 1 MHz, $T_A = 25^{\circ}C$, $V_{OUT} = GV_{DD}/2$, V_{OUT} (peak-to-peak) = 0.2 V.

Table 16 provides the current draw characteristics for MV_{REF}.

Table 16. Current Draw Characteristics for MV_{REF}

Parameter/Condition	Symbol	Min	Max	Unit	Note
Current draw for MV _{REF}	I _{MVREF}		500	μA	1

Note:

1. The voltage regulator for MV_{REF} must supply up to 500 μA current.

6.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

6.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

Table 17 provides the input AC timing specifications for the DDR2 SDRAM when $GV_{DD}(typ) = 1.8 \text{ V}$.

Table 17. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GV_{DD} of 1.8 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	_	MV _{REF} – 0.25	V	_
AC input high voltage	V _{IH}	MV _{REF} + 0.25	—	V	_

Table 18 provides the input AC timing specifications for the DDR SDRAM when $GV_{DD}(typ) = 2.5 \text{ V}$.

Table 18. DDR SDRAM Input AC Timing Specifications for 2.5-V Interface

At recommended operating conditions with GV_{DD} of 2.5 ± 5%.

Parameter	Symbol	Min	Мах	Unit	Notes
AC input low voltage	V _{IL}	—	MV _{REF} – 0.31	V	—
AC input high voltage	V _{IH}	MV _{REF} + 0.31	—	V	—

6.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20 shows the DDR and DDR2 output AC timing specifications.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions with GV_{DD} of (1.8 or 2.5 V) ± 5%.

Parameter	Symbol ¹	Min	Max	Unit	Notes
ADDR/CMD/MODT output setup with respect to MCK	t _{DDKHAS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
ADDR/CMD/MODT output hold with respect to MCK	t _{DDKHAX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output setup with respect to MCK	t _{DDKHCS}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	—		
MCS(n) output hold with respect to MCK	t _{DDKHCX}			ns	3
400 MHz		1.95	—		
333 MHz		2.40	—		
266 MHz		3.15	—		
200 MHz		4.20	_		
MCK to MDQS Skew	t _{DDKHMH}	-0.6	0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t _{DDKHDS,} t _{DDKLDS}			ps	5
400 MHz		700	—		
333 MHz		775	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQ/MECC/MDM output hold with respect to MDQS	t _{DDKHDX,} t _{DDKLDX}			ps	5
400 MHz		700	—		
333 MHz		900	—		
266 MHz		1100	—		
200 MHz		1200	—		
MDQS preamble start	t _{DDKHMP}	$-0.5\times t_{MCK}-0.6$	$-0.5\times t_{MCK}+0.6$	ns	6

Figure 7 shows the DDR SDRAM output timing diagram.



Figure 8 provides the AC test load for the DDR bus.



Figure 8. DDR AC Test Load

7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8349EA.

7.1 DUART DC Electrical Characteristics

Table 21 provides the DC electrical characteristics for the DUART interface of the MPC8349EA.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Мах	Unit
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	-0.3	0.8	V
Input current (0.8 V \leq V _{IN} \leq 2 V)	I _{IN}	—	±5	μA

8.2.1.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with LV_{DD}/OV_{DD} of 3.3 V ± 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit
GTX_CLK clock period	t _{GTX}	—	8.0	—	ns
GTX_CLK duty cycle	t _{GTXH} /t _{GTX}	43.75	—	56.25	%
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	^t GTKHDX	0.5	—	5.0	ns
GTX_CLK clock rise time (20%-80%)	t _{GTXR}	—	—	1.0	ns
GTX_CLK clock fall time (80%–20%)	t _{GTXF}		_	1.0	ns

Notes:

1. The symbols for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)(reference)(state)} for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the clock reference (K) going to the high state (H) relative to the time date input signals (D) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. In general, the clock reference symbol is based on three letters representing the clock of a particular function. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

8.2.1.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with LV_DD/OV_DD of 3.3 V \pm 10%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit
RX_CLK clock period	t _{GRX}	_	8.0	_	ns
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	40	_	60	%
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	_	_	ns
RXD[7:0], RX_DV, RX_ER hold time to RX_CLK	t _{GRDXKH}	0.5	_	_	ns

Local Bus

Figure 21 through Figure 26 show the local bus signals.



Figure 21. Local Bus Signals, Nonspecial Signals Only (DLL Enabled)



Figure 22. Local Bus Signals, Nonspecial Signals Only (DLL Bypass Mode)





Figure 23. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Enabled)



Figure 24. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 2 (DLL Bypass Mode)

JTAG

Parameter	Symbol	Condition	Min	Max	Unit
Output low voltage	V _{OL}	I _{OL} = 8.0 mA	_	0.5	V
Output low voltage	V _{OL}	I _{OL} = 3.2 mA	_	0.4	V

Table 40. JTAG Interface DC Electrical Characteristics (continued)

11.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE Std. 1149.1 (JTAG) interface of the MPC8349EA. Table 41 provides the JTAG AC timing specifications as defined in Figure 28 through Figure 31.

Table 41. JTAG AC Timing Specifications (Independent of CLKIN)¹

At recommended operating conditions (see Table 2).

Parameter		Symbol ²	Min	Max	Unit	Notes
JTAG external clock frequency of operation		f _{JTG}	0	33.3	MHz	—
JTAG external clock cycle ti	me	t _{JTG}	30	_	ns	—
JTAG external clock pulse w	vidth measured at 1.4 V	t _{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times		t _{JTGR} , t _{JTGF}	0	2	ns	—
TRST assert time		t _{TRST}	25	—	ns	3
Input setup times:	Boundary-scan data TMS, TDI	t _{JTDVKH} t _{JTIVKH}	4 4	_ _	ns	4
Input hold times:	Boundary-scan data TMS, TDI	t _{JTDXKH} t _{JTIXKH}	10 10		ns	4
Valid times:	Boundary-scan data TDO	t _{jtkldv} t _{jtklov}	2 2	11 11	ns	5
Output hold times:	Boundary-scan data TDO	t _{jtkldx} t _{jtklox}	2 2		ns	5

12 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8349EA.

12.1 I²C DC Electrical Characteristics

Table 42 provides the DC electrical characteristics for the I²C interface of the MPC8349EA.

Table 42. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 10%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	$0.7 \times OV_{DD}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	_
Low level output voltage	V _{OL}	0	$0.2\times\text{OV}_{\text{DD}}$	V	1
Output fall time from $V_{IH}(\text{min})$ to $V_{IL}(\text{max})$ with a bus capacitance from 10 to 400 pF	t _{I2KLKV}	$20 + 0.1 \times C_B$	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t _{i2KHKL}	0	50	ns	3
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I	-10	10	μA	4
Capacitance for each I/O pin	Cl	—	10	pF	_

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. C_B = capacitance of one bus line in pF.

3. Refer to the MPC8349EA Integrated Host Processor Family Reference Manual, for information on the digital filter used.

4. I/O pins obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.

12.2 I²C AC Electrical Specifications

Table 43 provides the AC timing parameters for the I²C interface of the MPC8349EA. Note that all values refer to $V_{IH}(min)$ and $V_{IL}(max)$ levels (see Table 42).

Table 43. I²C AC Electrical Specifications

Parameter	Symbol ¹	Min	Мах	Unit
SCL clock frequency	f _{I2C}	0	400	kHz
Low period of the SCL clock	t _{I2CL}	1.3	—	μS
High period of the SCL clock	t _{I2CH}	0.6	—	μS
Setup time for a repeated START condition	t _{I2SVKH}	0.6	—	μS
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{I2SXKL}	0.6	-	μs
Data setup time	t _{I2DVKH}	100	—	ns
Data hold time:CBUS compatible masters I ² C bus devices	t _{i2DXKL}	$\overline{0^2}$	0.9 ³	μS

13 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8349EA.

13.1 PCI DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the PCI interface of the MPC8349EA.

Parameter	Symbol	Test Condition	Min	Мах	Unit
High-level input voltage	V _{IH}	$V_{OUT} \ge V_{OH}$ (min) or	2	OV _{DD} + 0.3	V
Low-level input voltage	V _{IL}	$V_{OUT} \le V_{OL}$ (max)	-0.3	0.8	V
Input current	I _{IN}	$V_{IN}^{1} = 0 V \text{ or } V_{IN} = OV_{DD}$	_	±5	μA
High-level output voltage	V _{OH}	OV _{DD} = min, I _{OH} = -100 μA	OV _{DD} – 0.2	_	V
Low-level output voltage	V _{OL}	OV _{DD} = min, I _{OL} = 100 μA	_	0.2	V

Table 44. PCI DC Electrical Characteristics

Note:

1. The symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1.

13.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus of the MPC8349EA. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the device is configured as a host or agent device. Table 45 provides the PCI AC timing specifications at 66 MHz.

Table 45. PCI AC Timing	Specifications at 66 MHz ¹
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Parameter	Symbol ²	Min	Мах	Unit	Notes
Clock to output valid	^t PCKHOV	—	6.0	ns	3
Output hold from clock	t _{PCKHOX}	1		ns	3
Clock to output high impedance	t _{PCKHOZ}	—	14	ns	3, 4
Input setup to clock	t _{PCIVKH}	3.0	_	ns	3, 5
Input hold from clock	t _{PCIXKH}	0	_	ns	3, 5
REQ64 to PORESET setup time	t _{PCRVRH}	5	—	clocks	6

18.3 Pinout Listings

Table 55 provides the pin-out listing for the MPC8349EA, 672 TBGA package.

Table 55. MPC8349EA (TBGA) Pinout Listing

Signal	Signal Package Pin Number		Power Supply	Notes
	PCI1 and PCI2 (One 64-Bit or Two 32-Bit)			
PCI1_INTA/IRQ_OUT	B34	0	OV _{DD}	2
PCI1_RESET_OUT	C33	0	OV _{DD}	_
PCI1_AD[31:0]	G30, G32, G34, H31, H32, H33, H34, J29, J32, J33, L30, K31, K33, K34, L33, L34, P34, R29, R30, R33, R34, T31, T32, T33, U31, U34, V31, V32, V33, V34, W33, W34	I/O	OV _{DD}	—
PCI1_C/BE[3:0]	J30, M31, P33, T34	I/O	OV _{DD}	
PCI1_PAR	P32	I/O	OV _{DD}	_
PCI1_FRAME	M32	I/O	OV _{DD}	5
PCI1_TRDY	N29	I/O	OV _{DD}	5
PCI1_IRDY	M34	I/O	OV _{DD}	5
PCI1_STOP	N31	I/O	OV _{DD}	5
PCI1_DEVSEL	N30	I/O	OV _{DD}	5
PCI1_IDSEL	J31	I	OV _{DD}	_
PCI1_SERR	N34	I/O	OV _{DD}	5
PCI1_PERR	N33	I/O	OV _{DD}	5
PCI1_REQ[0]	D32	I/O	OV _{DD}	_
PCI1_REQ[1]/CPCI1_HS_ES	D34	I	OV _{DD}	_
PCI1_REQ[2:4]	E34, F32, G29	I	OV _{DD}	_
PCI1_GNT0	C34	I/O	OV _{DD}	_
PCI1_GNT1/CPCI1_HS_LED	D33	0	OV _{DD}	_
PCI1_GNT2/CPCI1_HS_ENUM	E33	0	OV _{DD}	_
PCI1_GNT[3:4]	F31, F33	0	OV _{DD}	_
PCI2_RESET_OUT/GPIO2[0]	W32	I/O	OV _{DD}	_
PCI2_AD[31:0]/PCI1[63:32]	AA33, AA34, AB31, AB32, AB33, AB34, AC29, AC31, AC33, AC34, AD30, AD32, AD33, AD34, AE29, AE30, AH32, AH33, AH34, AM33, AJ31, AJ32, AJ33, AJ34, AK32, AK33, AK34, AM34, AL33, AL34, AK31, AH30	I/O	OV _{DD}	
PCI2_C/BE[3:0]/PCI1_C/BE[7:4]	AC32, AE32, AH31, AL32	I/O	OV _{DD}	—
PCI2_PAR/PCI1_PAR64	AG34	I/O	OV _{DD}	_

Package and Pin Listings

Table 55. MPC8349EA (TBGA) Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
MPH1_PWRFAULT/ DR_RX_ERROR_PWRFAULT	E27	I	OV _{DD}	
MPH1_PCTL0/DR_TX_VALID_PCTL0	A29	0	OV _{DD}	—
MPH1_PCTL1/DR_TX_VALIDH_PCTL1	D28	0	OV _{DD}	—
MPH1_CLK/DR_CLK	B29	I	OV _{DD}	—
	USB Port 0			
MPH0_D0_ENABLEN/ DR_D8_CHGVBUS	C29	I/O	OV _{DD}	—
MPH0_D1_SER_TXD/ DR_D9_DCHGVBUS	A30	I/O	OV _{DD}	—
MPH0_D2_VMO_SE0/DR_D10_DPPD	E28	I/O	OV _{DD}	
MPH0_D3_SPEED/DR_D11_DMMD	B30	I/O	OV _{DD}	
MPH0_D4_DP/DR_D12_VBUS_VLD	C30	I/O	OV _{DD}	—
MPH0_D5_DM/DR_D13_SESS_END	A31	I/O	OV _{DD}	—
MPH0_D6_SER_RCV/DR_D14	B31	I/O	OV _{DD}	—
MPH0_D7_DRVVBUS/ DR_D15_IDPULLUP	C31	I/O	OV _{DD}	—
MPH0_NXT/DR_RX_ACTIVE_ID	B32		OV _{DD}	—
MPH0_DIR_DPPULLUP/DR_RESET	A32	I/O	OV _{DD}	—
MPH0_STP_SUSPEND/ DR_TX_READY	A33	I/O	OV _{DD}	—
MPH0_PWRFAULT/DR_RX_VALIDH	C32	I	OV _{DD}	—
MPH0_PCTL0/DR_LINE_STATE0	D31	I/O	OV _{DD}	—
MPH0_PCTL1/DR_LINE_STATE1	E30	I/O	OV _{DD}	_
MPH0_CLK/DR_RX_VALID	B33	I	OV _{DD}	—
	Programmable Interrupt Controller			
MCP_OUT	AN33	0	OV _{DD}	2
IRQ0/MCP_IN/GPIO2[12]	C19	I/O	OV _{DD}	—
IRQ[1:5]/GPIO2[13:17]	C22, A22, D21, C21, B21	I/O	OV _{DD}	—
IRQ[6]/GPIO2[18]/CKSTOP_OUT	A21	I/O	OV _{DD}	—
IRQ[7]/GPIO2[19]/CKSTOP_IN	C20	I/O	OV _{DD}	
	Ethernet Management Interface			
EC_MDC	A7	0	LV _{DD1}	
EC_MDIO	E9	I/O	LV _{DD1}	11

Package and Pin Listings

Signal	Package Pin Number	Pin Type	Power Supply	Notes
	Gigabit Reference Clock			•
EC_GTX_CLK125	C8	I	LV _{DD1}	_
Three	Speed Ethernet Controller (Gigabit Eth	ernet 1)		
TSEC1_COL/GPIO2[20]	A17	I/O	OV _{DD}	—
TSEC1_CRS/GPIO2[21]	F12	I/O	LV _{DD1}	—
TSEC1_GTX_CLK	D10	0	LV _{DD1}	3
TSEC1_RX_CLK	A11	I	LV _{DD1}	—
TSEC1_RX_DV	B11	I	LV _{DD1}	—
TSEC1_RX_ER/GPIO2[26]	B17	I/O	OV _{DD}	—
TSEC1_RXD[7:4]/GPIO2[22:25]	B16, D16, E16, F16	I/O	OV _{DD}	—
TSEC1_RXD[3:0]	E10, A8, F10, B8	I	LV _{DD1}	—
TSEC1_TX_CLK	D17	I	OV _{DD}	—
TSEC1_TXD[7:4]/GPIO2[27:30]	A15, B15, A14, B14	I/O	OV _{DD}	—
TSEC1_TXD[3:0]	A10, E11, B10, A9	0	LV _{DD1}	10
TSEC1_TX_EN	B9	0	LV _{DD1}	—
TSEC1_TX_ER/GPIO2[31]	A16	I/O	OV _{DD}	—
Three	Speed Ethernet Controller (Gigabit Eth	ernet 2)		
TSEC2_COL/GPIO1[21]	C14	I/O	OV _{DD}	—
TSEC2_CRS/GPIO1[22]	D6	I/O	LV _{DD2}	—
TSEC2_GTX_CLK	A4	0	LV _{DD2}	—
TSEC2_RX_CLK	B4	I	LV _{DD2}	—
TSEC2_RX_DV/GPIO1[23]	E6	I/O	LV _{DD2}	—
TSEC2_RXD[7:4]/GPIO1[26:29]	A13, B13, C13, A12	I/O	OV _{DD}	—
TSEC2_RXD[3:0]/GPIO1[13:16]	D7, A6, E8, B7	I/O	LV _{DD2}	
TSEC2_RX_ER/GPIO1[25]	D14	I/O	OV _{DD}	—
TSEC2_TXD[7]/GPIO1[31]	B12	I/O	OV _{DD}	—
TSEC2_TXD[6]/ DR_XCVR_TERM_SEL	C12	0	OV _{DD}	_
TSEC2_TXD[5]/ DR_UTMI_OPMODE1	D12	0	OV _{DD}	—
TSEC2_TXD[4]/ DR_UTMI_OPMODE0	E12	0	OV _{DD}	_
TSEC2_TXD[3:0]/GPIO1[17:20]	B5, A5, F8, B6	I/O	LV _{DD2}	—

			Input Clock Frequency (MHz) ²			
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67
				csb_clk Freq	uency (MHz)	
Low	0110	6:1	100	150	200	
Low	0111	7:1	116	175	233	
Low	1000	8:1	133	200	266	
Low	1001	9:1	150	225	300	
Low	1010	10 : 1	166	250	333	
Low	1011	11 : 1	183	275		1
Low	1100	12 : 1	200	300		
Low	1101	13 : 1	216	325		
Low	1110	14 : 1	233			
Low	1111	15 : 1	250			
Low	0000	16 : 1	266			
High	0010	2:1				133
High	0011	3:1			100	200
High	0100	4 : 1			133	266
High	0101	5:1			166	333
High	0110	6:1			200	
High	0111	7:1			233	
High	1000	8:1				

Table 59. CSB Frequency Options for Host Mode (continued)

¹ CFG_CLKIN_DIV selects the ratio between CLKIN and PCI_SYNC_OUT.

² CLKIN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 60. CSB Frequency Options for Agent Mode

			In	put Clock Fre	equency (MHz) ²	
CFG_CLKIN_DIV at Reset ¹	SPMF	<i>csb_clk</i> : Input Clock Ratio ²	16.67	25	33.33	66.67	
				<i>csb_clk</i> Freq	uency (MHz)		
Low	0010	2 : 1				133	
Low	0011	3 : 1			100	200	
Low	0100	4 : 1		100	133	266	
Low	0101	5 : 1		125	166	333	

where:

 $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)

 $R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

 $R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed-circuit board, or change the thermal dissipation on the printed-circuit board surrounding the device.

The thermal performance of devices with heat sinks has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Table 64 shows heat sink thermal resistance for TBGA of the MPC8349EA.

Host Sink Assuming Thermal Grosse	Air Flow	$35 \times 35 \text{ mm TBGA}$	
neat Sink Assuming Merinai Grease		Thermal Resistance	
AAVID $30 \times 30 \times 9.4$ mm pin fin	Natural convection	10	
AAVID $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.5	
AAVID $30 \times 30 \times 9.4$ mm pin fin	2 m/s	5.6	
AAVID 31 \times 35 \times 23 mm pin fin	Natural convection	8.4	
AAVID 31 \times 35 \times 23 mm pin fin	1 m/s	4.7	
AAVID 31 \times 35 \times 23 mm pin fin	2 m/s	4	
Wakefield, $53 \times 53 \times 25$ mm pin fin	Natural convection	5.7	
Wakefield, $53 \times 53 \times 25$ mm pin fin	1 m/s	3.5	
Wakefield, $53 \times 53 \times 25$ mm pin fin	2 m/s	2.7	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	Natural convection	6.7	
MEI, 75 \times 85 \times 12 no adjacent board, extrusion	1 m/s	4.1	
MEI, $75 \times 85 \times 12$ no adjacent board, extrusion	2 m/s	2.8	
MEI, $75 \times 85 \times 12$ mm, adjacent board, 40 mm side bypass	1 m/s	3.1	

Table 64. Heat Sink and Thermal Resistance of MPC8349EA (TBGA)

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

have a low ESR (equivalent series resistance) rating to ensure the quick response time. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors are 100–330 μ F (AVX TPS tantalum or Sanyo OSCON).

21.4 Connection Recommendations

To ensure reliable operation, connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to OV_{DD} , GV_{DD} , or LV_{DD} as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD} , GV_{DD} , LV_{DD} , OV_{DD} , and GND pins of the MPC8349EA.

21.5 Output Buffer DC Impedance

The MPC8349EA drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 43). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N) \div 2$.



Figure 43. Driver Impedance Measurement

Two measurements give the value of this resistance and the strength of the driver current source. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term} . The measured voltage is

22.1 Part Numbers Fully Addressed by This Document

Table 66 shows an analysis of the Freescale part numbering nomenclature for the MPC8349EA. The individual part numbers correspond to a maximum processor core frequency. Each part number also contains a revision code that refers to the die mask revision number. For available frequency configuration parts including extended temperatures, refer to the device product summary page on our website listed on the back cover of this document or, contact your local Freescale sales office.

MPC	nnnn	е	t	рр	aa	а	r
Product Code	Part Identifier	Encryption Acceleration	Temperature ¹ Range	Package ²	Processor Frequency ³	Platform Frequency	Revision Level
MPC	8349	Blank = Not included E = included	Blank = 0 to 105°C C = -40 to 105°C	ZU =TBGA VV = PB free TBGA	e300 core speed AG = 400 AJ = 533 AL = 667	D = 266 F = 333 ⁴	B = 3.1

Table 66. Part Numbering Nomenclature

Notes:

1. For temperature range = C, processor frequency is limited to with a platform frequency of 266 and up to 533 with a platform frequency of 333

2. See Section 18, "Package and Pin Listings," for more information on available package types.

- Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by Part Number Specifications may support other maximum core frequencies.
- 4. ALF marked parts support DDR1 data rate up to 333 MHz (at 333 MHz CSB as the 'F' marking implies) and DDR2 data rate up to 400 MHz (at 200 MHz CSB). AJF marked parts support DDR1 and DDR2 data rate up to 333 MHz (at a CSB of 333 MHz).

Table 67 shows the SVR settings by device and package type.

Table 67. SVR Settings

Device	Package	SVR (Rev. 3.0)
MPC8349EA	TBGA	8050_0030
MPC8349A	TBGA	8051_0030

Document Revision History

22.2 Part Marking

Parts are marked as in the example shown in Figure 44.



Figure 44. Freescale Part Marking for TBGA Devices

23 Document Revision History

This table provides a revision history of this document.

Table (6 8 .	Docume	ent Rev	vision	History
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Rev. Number	Date	Substantive Change(s)
13	09/2011	 In Section 2.2, "Power Sequencing," added Section 2.2.1, "Power-Up Sequencing" and Figure 4. In Table 25, Table 29 and Table 31, removed the GTX_CLK125. In Table 34, updated t_{MDKHDX} Max value from 170ns to 70ns.
12	11/2010	 In Table 55 added note for pin LGPL4. In Section 21.7, "Pull-Up Resistor Requirements, updated the list of open drain type pins.
11	05/2010	 In Table 25 through Table 30, changed V_{IL}(min) to V_{IH}(max) to (20%–80%). Added Table 8, "EC_GTX_CLK125 AC Timing Specifications."
10	5/2009	 In Table 57, updated frequency for max csb_clk to 333 MHz and DDR2, from 100-200 to 100-133 at core frequency = 533MHz. In Section 18.1, "Package Parameters for the MPC8349EA TBGA, changed solder ball for TBGA and PBGA from 95.5 Sn/0.5 Cu/4 Ag to 96.5 Sn/3.5 Ag. In Table 66, footnote 1, changed 667(TBGA) to 533(TBGA). footnote 4, added data rate for DDR1 and DDR2.

Rev. Number	Date	Substantive Change(s)
9	2/2009	 Added footnote 6 to Table 7. In Section 9.2, "USB AC Electrical Specifications," clarified that AC table is for ULPI only. In Table 39, corrected t_{LBKHOV} parameter to t_{LBKLOV} (output data is driven on falling edge of clock in DLL bypass mode). Similarly, made the same correction to Figure 22, Figure 24, and Figure 25 for output signals. Added footnote 11 to Table 55. Added footnote 4 to Table 66. In Section 21.1, "System Clocking," removed "(AVDD1)" and "(AVDD2") from bulleted list. In Section 21.2, "PLL Power Supply Filtering," in the second paragraph, changed "provide five independent filter circuits," and "the five AVDD pins" to provide four independent filter circuits," and "the four AVDD pins." In Table 57, corrected the max csb_clk to 266 MHz. In Table 62, added PLL configurations 903, 923, A03, A23, and 503 for 533 MHz In Table 66, updated note 1 to say the following: "For temperature range = C, processor frequency is limited to 533 with a platform frequency of 266."
8	4/2007	 In Table 3, "Output Drive Capability," changed the values in the Output Impedance column and added USB to the seventh row. In Section 21.7, "Pull-Up Resistor Requirements,"deleted last two paragraphs and after first paragraph, added a new paragraph. Deleted Section 21.8, "JTAG Configuration Signals," and Figure 43, "JTAG Interface Connection."
7	3/2007	 In Table 57, "Operating Frequencies for TBGA," in the 'Coherent system bus frequency (<i>csb_clk</i>)' row, changed the value in the 533 MHz column to 100-333. In Table 63, "Suggested PLL Configurations," under the subhead, '33 MHz CLKIN/PCI_CLK Options,' added row A03 between Ref. No. 724 and 804. Under the subhead '66 MHz CLKIN/PCI_CLK Options,' added row 503 between Ref. No. 305 and 404. For Ref. No. 306, changed the CORE PLL value to 0000110. In Section 23, "Ordering Information," replaced first paragraph and added a note. In Section 23.1, "Part Numbers Fully Addressed by this Document," replaced first paragraph.
6	2/2007	 Page 1, updated first paragraph to reflect PowerQUICC II Pro information. In Table 18, "DDR and DDR2 SDRAM Input AC Timing Specifications," added note 2 to t_{CISKEW} and deleted original note 3; renumbered the remaining notes. In Figure 41, "JTAG Interface Connection," updated with new figure. In Section 23.1, "Part Numbers Fully Addressed by This Document," replaced third sentence of first paragraph directing customer to product summary page for available frequency configuration parts.
5	1/2007	 In Table 1, "Absolute Maximum Ratings," added (1.36 max for 667-MHz core frequency) to max V_{DD} and Av_{DD} values. In Table 2, "Recommended Operating Conditions," added a row showing nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts. In Table 4, "MPC8349EA Power Dissipation," added two footnotes to 667-MHz row showing nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts. In Table 54, "MPC83479EA (TBGA) Pinout Listing," updated V_{DD} nd AV_{DD} rows to show nominal core supply voltage and PLL supply voltage of 1.3 V for 667-MHz parts.
4	12/2006	Table 19, "DDR and DDR2 SDRAM Output AC Timing Specifications," modified T _{ddkhds} for 333 MHz from 900 ps to 775 ps.

Rev. Number	Date	Substantive Change(s)
3	11/2006	 Updated note in introduction. In the features list in Section 1, "Overview," updated DDR data rate to show 400 MHz for DDR2 for TBGA parts for silicon 3.x and 400 MHz for DDR2 for TBGA parts for silicon 3.x. In Section 23, "Ordering Information," replicated note from document introduction.
2	8/2006	 Changed all references to revision 2.0 silicon to revision 3.0 silicon. Changed VIH minimum value in Table 40, "JTAG Interface DC Electrical Characteristics," to OV_{DD} - 0.3. In Table 44, "PCI DC Electrical Characteristics," changed high-level input voltage values to min = 2 and max = OV_{DD} + 0.3; changed low-level input voltage values to min = (-0.3) and max = 0.8. Updated DDR2 I/O power values in Table 5, "MPC8347EA Typical I/O Power Dissipation." In Table 66, "Suggested PLL Configurations," deleted reference-number rows 902 and 703.
1	4/2006	 Removed Table 20, "Timing Parameters for DDR2-400." Changed ADDR/CMD to ADDR/CMD/MODT in Table 9, "DDR and DDR2 SDRAM Output AC Timing Specifications," rows 2 and 3, and in Figure 2, "DDR SDRAM Output Timing Diagram. Changed Min and Max values for V_{IH} and VIL in Table 40Table 44,"PCI DC Electrical Characteristics." In Table 55, "MPC8349EA (TBGA) Pinout Listing," and Table 52, "MPC8347EA (PBGA) Pinout Listing," modified rows for MDICO and MDIC1 signals and added note 'It is recommended that MDICO be tied to GRD using an 18 Ω resistor and MCIC1 be tied to DDR power using an 18 Ω resistor.' Table 55, "MPC8349EA (TBGA) Pinout Listing," in row AVDD3 changed power supply from "AVDD3" to '—.'
0	3/2006	Initial public release

Table 68. Document Revision History (continued)