Zilog - Z8018216ASC1838TR Datasheet

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018216asc1838tr

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source
  - Up to 5 Mbits/sec at 20 MHz PCLK (ESCC).
- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit
- NRZ, NRZI or FM encoding/decoding. Manchester Code Decoding (Encoding with External Logic).
- Baud Rate Generator in each Channel
- Digital Phase-Locked Loop (DPLL) for Clock Recovery
- Crystal Oscillator

The following features are implemented in the ESCC™ for the Z80182/Z8L182 only:

- New 32-bit CRC-32 (Ethernet Polynomial)
- ESCC Programmable Clock
  - programmed to be equal to system clock divided by one or two
  - programmed by Z80182 Enhancement Register

Note: The ESCC™ programmable clock must be programmed to divide-by-two mode when operating above the following conditions:

– PHI > 20 MHz at 5.0V

– PHI > 10 MHz at 3.0V

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

TIMER DATA REGISTERS

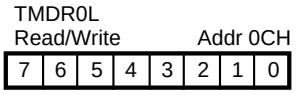


Figure 23. Timer 0 Data Register L

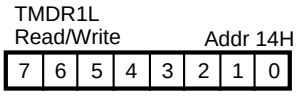
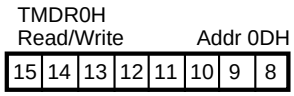
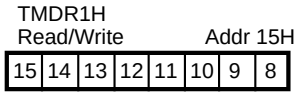


Figure 24. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 25. Timer 0 Data Register H



When Read, read Data Register L before reading Data Register H.

Figure 26. Timer 1 Data Register H

TIMER RELOAD REGISTERS

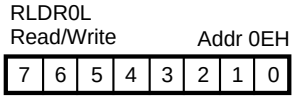


Figure 27. Timer 0 Reload Register L

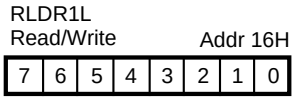


Figure 28. Timer 1 Reload Register L

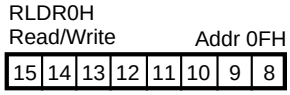


Figure 29. Timer 0 Reload Register H

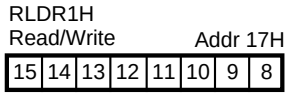


Figure 30. Timer 1 Reload Register H

FREE RUNNING COUNTER

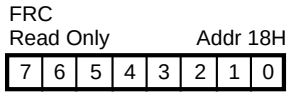


Figure 32. Free Running Counter

CPU CONTROL REGISTER

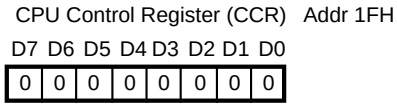
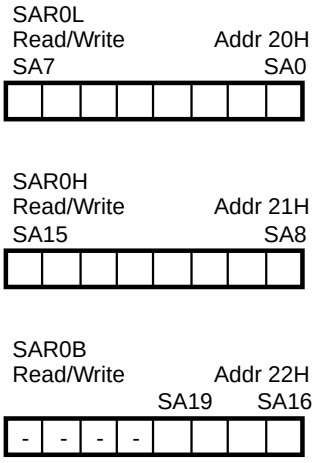


Figure 33. CPU

Note: See Figure 49 for full description.

DMA REGISTERS



Bits 0-2 (3) are used for SAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	RDR1 (ASCI1)
x	x	1	1	Not Used

Figure 34. DMA 0 Source Address Registers

SYSTEM CONTROL REGISTERS

IL — Addr 33H

Bit	IL7	IL6	IL5	-	-	-	-	-
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W					

Interrupt Vector Low

Figure 46. Interrupt Vector Low Register

ITC — Addr 34H

Bit	TRAP	UFO	-	-	-	ITE2	ITE1	ITE0
Upon Reset	0	0	1	1	1	0	0	1
R/W	R/W	R				R/W	R/W	R/W

/INT Enable 2, 1, 0
Undefined Fetch Object
TRAP

Figure 47. INT/TRAP Control Register

RCR — Addr 36H

Bit	REFE	REFW	-	-	-	-	CYC1	CYC0
Upon Reset	1	1	1	1	1	1	0	0
R/W	R/W	R/W					R/W	R/W

Cycle Select
Refresh Wait State
Refresh Enable

CYC1, 0	Interval of Refresh Cycle
00	10 states
01	20 states
10	40 states
11	80 states

Figure 48. Refresh Control Register

ADDITIONAL FEATURES ON THE Z182 MPU

The following is a detailed description of the enhancements to the Z8S180 from the standard Z80180 in the areas of STANDBY, IDLE, and STANDBY-QUICK RECOVERY modes.

Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce the current consumption. The Z8S180 has added two additional power-down modes, STANDBY and IDLE, to reduce the current consumption even further. The differences among these power-down modes are summarized in Table 10.

Table 10. Power Down Modes

Power-Down Modes	CPU Core	On-Chip I/O	OSC.	CLKOUT	Recovery Source	Recovery Time (Minimum)
SLEEP	Stop	Running	Running	Running	RESET, Interrupts	1.5 Clock
I/O STOP	Running	Stop	Running	Running	By Programming	-
SYSTEM STOP	Stop	Stop	Running	Running	RESET, Interrupts	1.5 Clock
IDLE†	Stop	Stop	Running	Stop	RESET, Interrupts, BUSREQ	8 +1.5 Clock
STANDBY†	Stop	Stop	Stop	Stop	RESET, Interrupts, BUSREQ	2^{17} +1.5 Clock (Normal Recovery) 2^{6} +1.5 Clock (Quick Recovery)

Notes:
† IDLE and STANDBY modes are only offered in Z8S180. Note that the minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.

STANDBY Mode

The Z8S180 has been designed to save power. Two low-power programmable power-down modes have been added; STANDBY mode and IDLE mode. The STANDBY/IDLE mode is selected by multiplexing D6 and D3 of the CPU Control Register (CCR, I/O Address = 1FH). To enter STANDBY mode:

1. Set D6 and D3 to 1 and 0, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY mode, it behaves similar to the SYSTEM STOP mode which currently exists on the Z80180, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to typically 50 μA..

Since the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter has been added in the Z8S180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down 2^{17} counts before acknowledgment is sent to the interrupt source.

The recovery source needs to remain asserted for duration of the 2^{17} count, otherwise standby will be resumed.

The following is a description of how the part exits STANDBY for different interrupts and modes of operation.

STANDBY Mode Exit with /RESET

The /RESET input needs to be asserted for a duration long enough for the crystal oscillator to stabilize and then exit from the STANDBY mode. When /RESET is de-asserted, it goes through the normal reset timing to start instruction execution at address (logical and physical) 0000H.

The clocking is resumed within the Z8S180 and at the system clock output after /RESET is asserted when the crystal oscillator is restarted, but not yet stabilized.

CONTROL REGISTERS

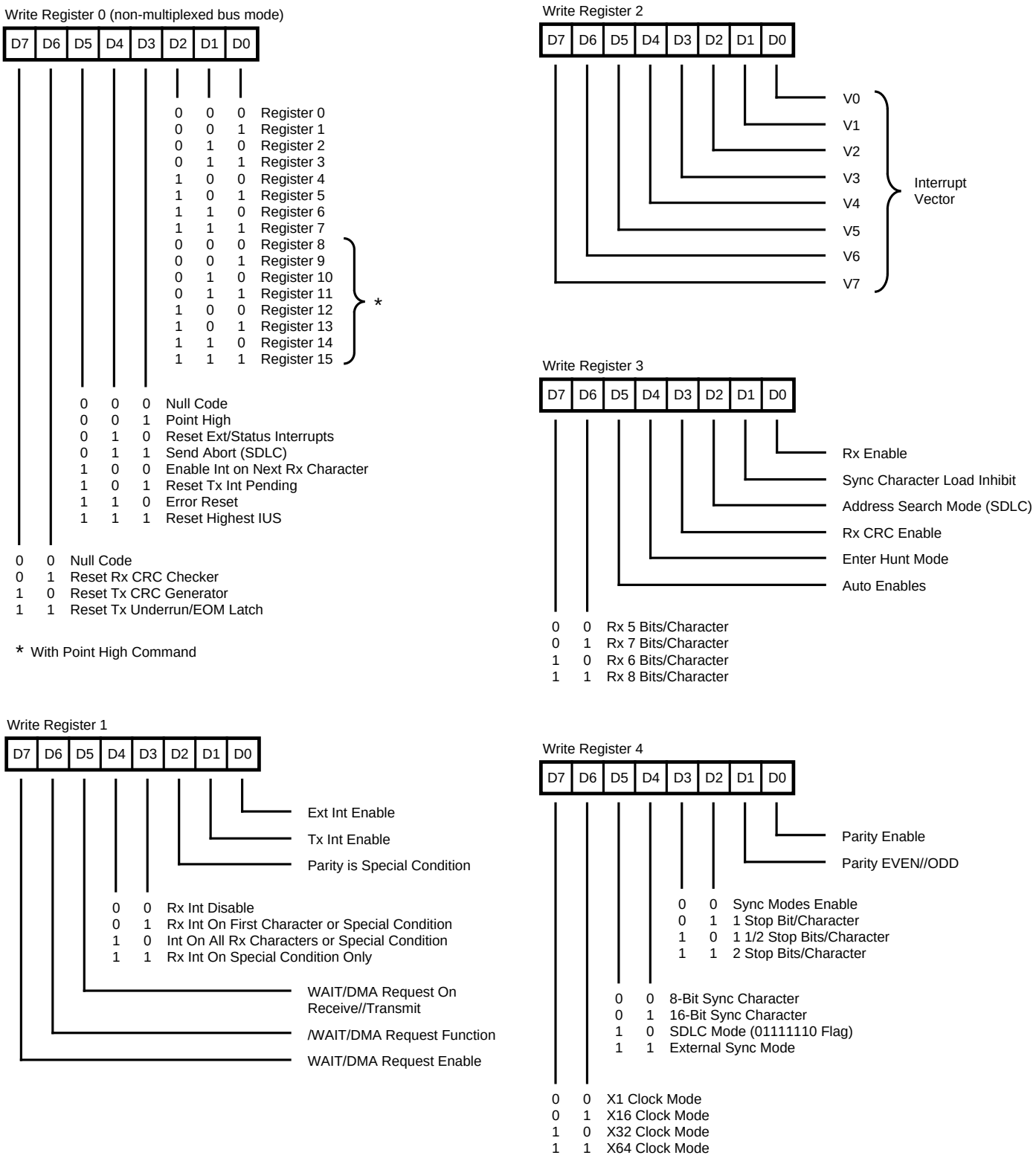
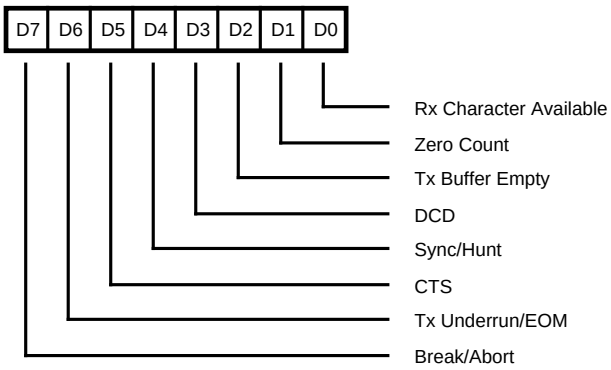
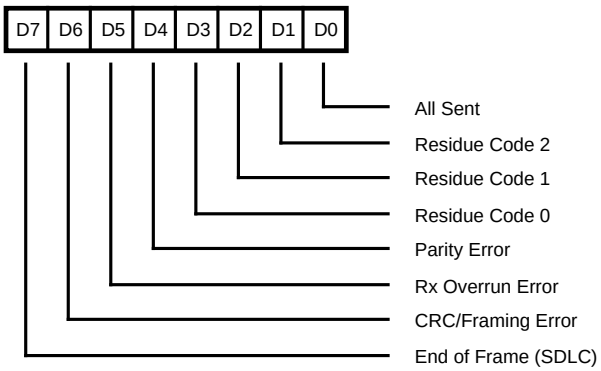


Figure 52. Write Register Bit Functions

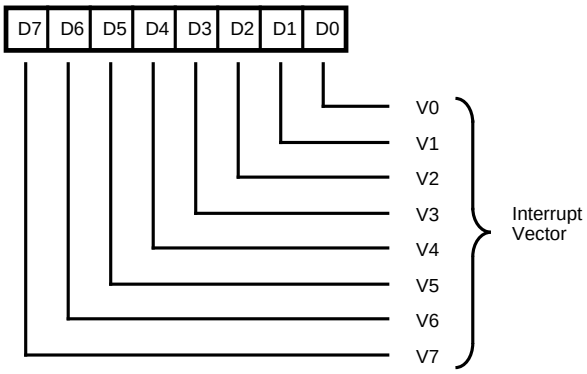
Read Register 0



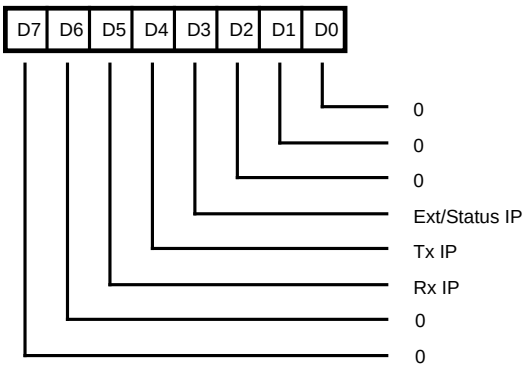
Read Register 1



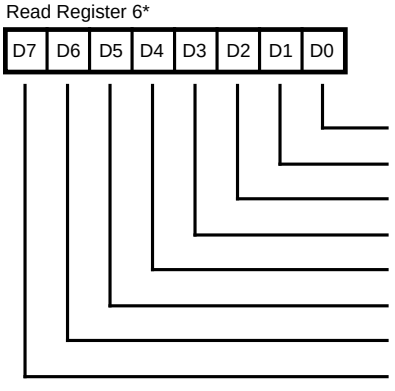
Read Register 2



Read Register 3



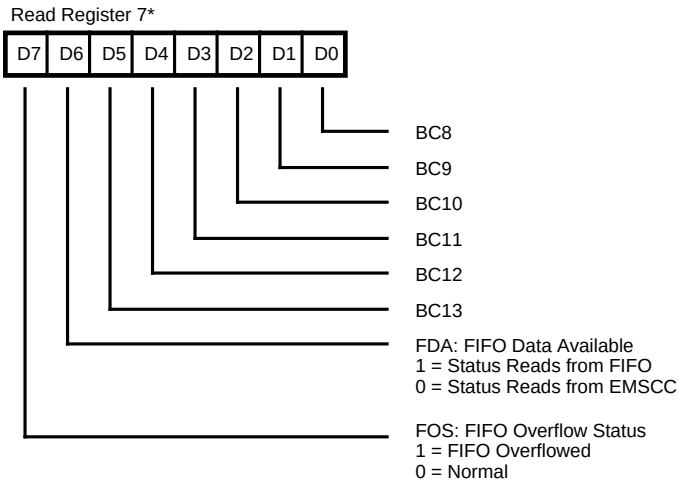
Read Register 6*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Read Register 7*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Figure 52. Write Register Bit Functions (Continued)

INTERRUPT EDGE/PIN MUX REGISTER (Continued)

Bit 0. Programming this bit to 1 selects a 16 cycle wait delay on recovery from HALT. Halt Recovery is disabled if bit 5 of the enhancement register is set to 1. A 0 selects no wait delay on Halt recovery.

If Halt Recovery is selected, the following pins assume the following states during halt and during the recovery, whether it is in HALT, SLP, IDLE or STBY Modes:

Address	=	Z
Data Bus	=	Z
RD	=	Z
WR	=	Z
MREQ/MRD	=	Z
M1	=	1
ST	=	1
IORQ	=	1
BUSACK	=	1
RFSH	=	1
E	=	Note 3
IOCS	=	Z
MWR	=	1 ***(Note 4)***

Notes:

1. This assumes that BUSREQ is not activated during the halt.

2. This assumes that the refresh is not enabled. This would not be a logical case since the address bus is tri-stated during the Halt mode.

3. There is no control on the E line during the halt recovery so transitions on the pin are possible.

4. This is only true if MWR function is enabled.

The Halt recovery mode is implemented by applying wait states to the next CPU operation following the exit from halt. All signals listed above are forced to their specified state (unless otherwise noted) during halt and also during the recovery state. Sixteen cycles after the halt pin goes High the signals are released to their normal state, then eight wait states are inserted to allow proper access to accommodate slow memories.

After the first memory access, the wait states will be inserted as programmed in the wait state generators.

In addition, if bit 4 of the Z80182 Enhancement Register is set, the TxDA pin will be tri-stated during Halt and Recovery modes.

16550 MIMIC REGISTERS

The Z80182/Z8L182 contains the following set of registers for interfacing with the PC/XT/AT.

- Receive Buffer Register
- Transmit Holding Register
- Interrupt Enable Register
- Interrupt Identification Register
- FIFO Control Register
- Line Control Register
- Modem Control Register
- Line Status Register
- Modem Status Register
- Scratch Register
- Divisor Latch Least/Most Significant Bytes
- FIFO Control Register

These registers emulate the 16550 UART and enable the PC/XT/AT to interface with them as with an actual 16550 UART. This allows the Z80182/Z8L182 to be software compatible with existing modem software.

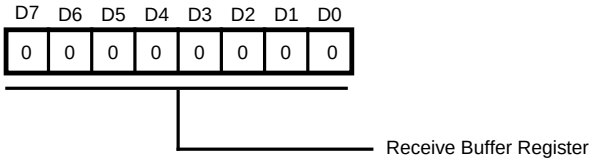


Figure 69. Receive Buffer Register
(PC Read Only, Address 00H, DLAB=0, R/W=Read)
(Z180™ MPU Write Only, Address XXF0H)

Receive Buffer Register

When the Z180 has assembled a byte of data to pass to the PC/XT/AT, it places it in the Receive Buffer Register. If the Received Data Available interrupt is enabled then an interrupt is generated for the PC/XT/AT and the Data Ready bit is set (if the Receive Timer is enabled, the interrupt and setting of the Data Ready bit is delayed until after the timer times out). Also the shadowed bits of the Line Status Register are transferred to their respective bits when the Z180 MPU writes to the Receive Buffer Register (See Line Status Register Bits 1, 2, 3 and 4). This allows a simultaneous setting of error bits when the data is written to the Receive Buffer Register. In FIFO, mode this address is used to read (PC) and write (Z180) the Receive FIFO.

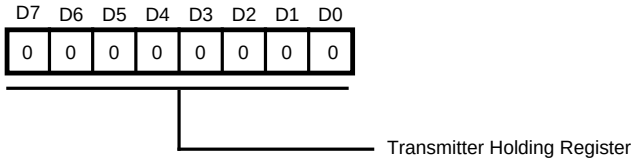


Figure 70. Transmit Holding Register
(PC Write Only, Address 00H, DLAB=0, R/W=Write)
(Z180 MPU Read Only, Address xxF0H)

Transmit Holding Register

When the PC/XT/AT writes to the Transmit Holding Register, the Z80182/Z8L182 responds by setting the appropriate bit in the IP register and by generating an interrupt to the Z180 MPU if it is enabled. When the Z180 MPU reads this register the Transmit Holding Register empty flag is set (if the transmitter timer is enabled , this bit is set after the timer times out). In FIFO mode of operation, this address is used to read (Z180) and write (PC) the Transmitter FIFO.

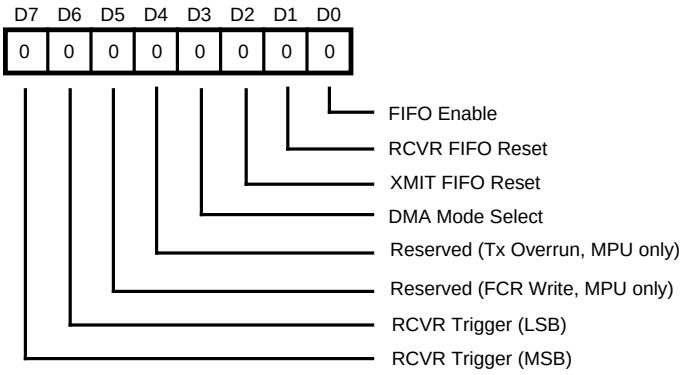


Figure 71. FIFO Control Register
(PC Write Only, Address 02H)
(Z180 MPU Read Only, Address xxE9H)

16550 MIMIC REGISTERS (Continued)

FIFO Control Register

Bit 6 and Bit 7 RCVR trigger LSB and MSB bits
This 2-bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs (see Table 18).

Bit 4 and Bit 5
Reserved for future use (PC side). Note: From the MPU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side will clear a previously set bit 4 or bit 5.

Bit 3 DMA mode select
Setting this bit to 1 will cause the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A 1 in this bit enables multi-byte DMA).

Bit 2 XMIT FIFO Reset
Setting this bit to 1 will cause the transmitter FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 1 RCVR FIFO Reset
Setting this bit to 1 will cause the receiver FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 0 FIFO Enable
The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be 1 when writing to the other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared. This feature can be forced in a disabled state by the MPU.

Table 18. Receive Trigger Level

b7	b6	Trigger Level, Number of Bytes
0	0	1
0	1	4
1	0	8
1	1	14

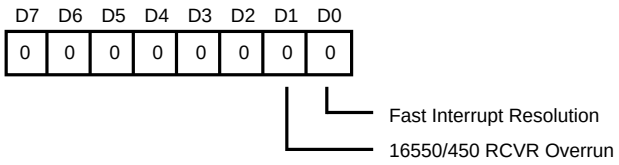


Figure 72. MIMIC Modification Register
(Z180 MPU Write only, Address xxE9h)

Bit 7-2 Reserved. Program to zero.

Bit 1 RCVR Overrun Modification
The actual 16450/16550 device allows the last position in FIFO to be overwritten by DCE during receiver overrun condition. When this bit is enabled (programmed to 1) the last position in FIFO can be overwritten by Z180 during receiver overrun. This feature is disabled by default. When this modification is not enabled, the MIMIC will ignore any write to RBR during an overrun condition.

Bit 0 Fast MIMIC-ESCC Interrupt Resolution
When enabling this modification, the internal MIMIC IEO signal into the ESCC IEI input is forced Low when the MIMIC Interrupt line becomes active. This is required to prevent the ESCC from putting it's vector on the databus during an INTACK cycle (given that the MIMIC is programmed to have higher interrupt priority).

When disabled, the internal MIMIC IEO becomes deasserted only after an interrupt acknowledge cycle. In this case, it is possible for the ESCC to force it's interrupt vector onto the data bus even when the MIMIC has a pending interrupt and is higher in priority.

Although this bit is disabled by default, it is advised that this bit is enabled to prevent interrupt conflict between MIMIC and ESCC interrupts.

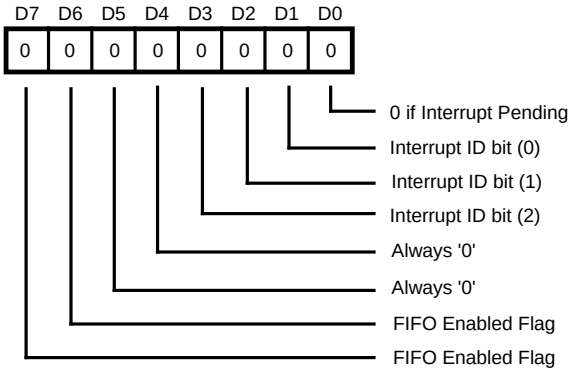


Figure 73. Interrupt Identification Register
(PC Read Only, Address 02H)
(Z180 MPU no access)

Interrupt Identification Register

Bit 7 and Bit 6 FIFO's Enabled
These bits will read 1 if the FIFO mode is enabled on the MIMIC.

Bit 5 and Bit 4 Always Read 0
Reserved bits.

Bits 3-1 Interrupt ID Bits
This 3-bit field is used to determine the highest priority interrupt pending (see Table 19).

Bit 0 Interrupt Pending
This bit is logic 0 and interrupt is pending.

When the PC accesses the IIR, the contents of the register and all pending interrupts are frozen. Any new interrupts will be recorded, but not acknowledged, during the IIR access.

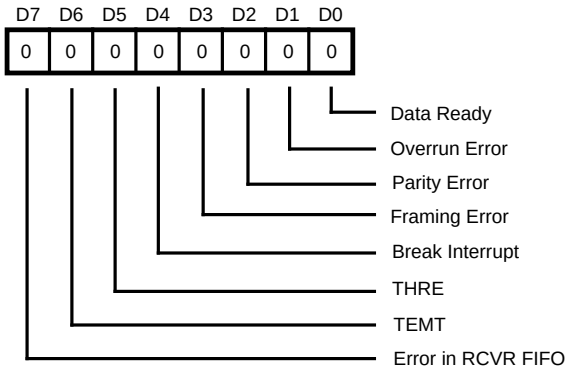


Figure 74. Line Status Register
(PC Read Only, Address 05H)
(Z180 MPU Read/Write bits 6, 4, 3, 2, Address xxF5H)

Table 19. Interrupt Identification Field

b3	b2	b1	Priority	Interrupt Source	INT Reset Control
0	1	1	Highest	Overrun, Parity, Framing error or Break detect bits set by MPU	Read Line Status Register
0	1	0	2nd	Received Data trigger level	RCVR FIFO drops below trigger level
1	1	0	2nd	Receiver Timeout with data in RCVR FIFO.	Read RCVR FIFO
0	0	1	3rd	Transmitter Holding Register Empty.	Writing to the Transmitter Holding Register or reading the Interrupt Identification Register when the THRE is the source of the interrupt.
0	0	0	4th	MODEM status: CTS, DSR, RI or DCD	Reading the MODEM status register.

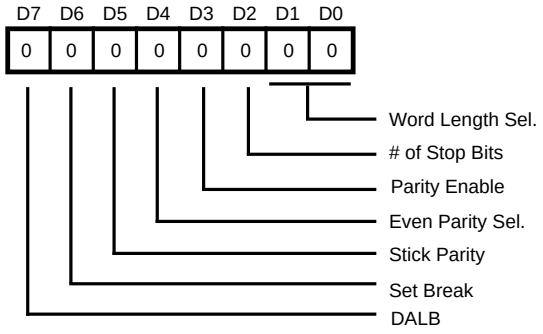


Figure 76. Line Control Register
(PC Read/Write, Address 03H)
(Z180 MPU Read Only, Address xxF3H)

Line Control Register

Bit 7 Divisor Latch Access Bit (DALB)
This bit allow access to the divisor latch by the PC/XT/AT. If this bit is set to 1, access to the Transmitter, Receiver and Interrupt Enable Registers is disabled. When an access is made to address 0 the Divisor Latch Least Significant byte is accessed. If an access is made to address 1, the Divisor Latch Most Significant byte is accessed.

Bit 6 - Bit 0
These bits do not affect the Z80182/Z8L182 directly, however they can be read by the Z180 MPU and the 16550 MIMIC modes can be emulated by the Z180 MPU.

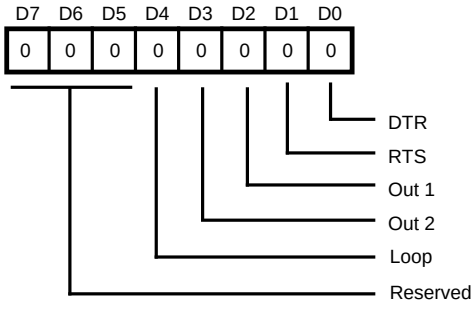


Figure 77. Modem Control Register
(PC Read/Write, Address 04H)
(Z180 MPU Read Only, Address xxF4H)

Modem Control Register

Bit 7-5 Reserved
Reserved for future use, always 0.

Bit 4 Loop
When this bit is set to 1, D3-D0 field reflects the status of Modem Status Register, as follows:

RI = Out 1
DCD = Out 2
DSR = DTR
CTS = RTS

Emulation of the 16550 UART loop back feature must be done by the Z180 MPU, except in the above conditions.

Bit 3 Out 2
This bit controls the tri-state on the HINTR pin if bits 2 and 1 are 10. Otherwise it can be read by the Z180 MPU.

Bits 2, 1, 0
These bits have no direct control of the 16550 MIMIC interface and the Z180 MPU must emulate the function if it is to be implemented.

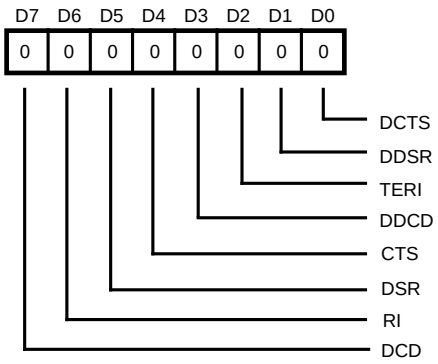


Figure 78. Modem Status Register
(PC Read Only, Address 06H)
(Z180 MPU Read/Write bits 7-4, Address xxF6H)

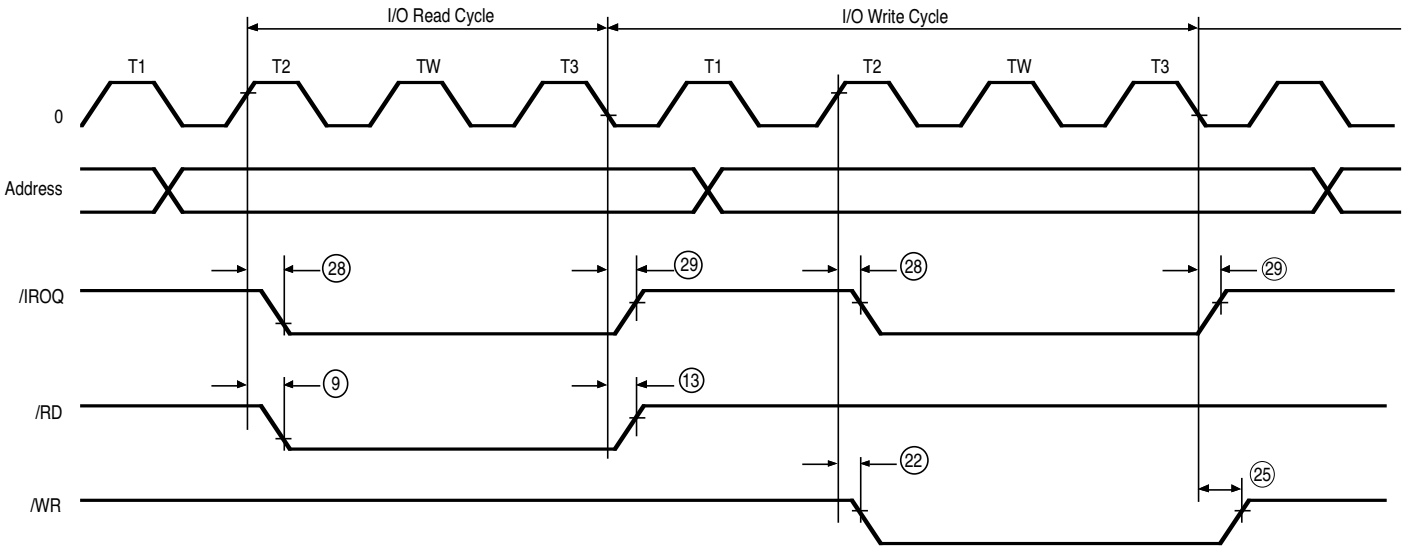
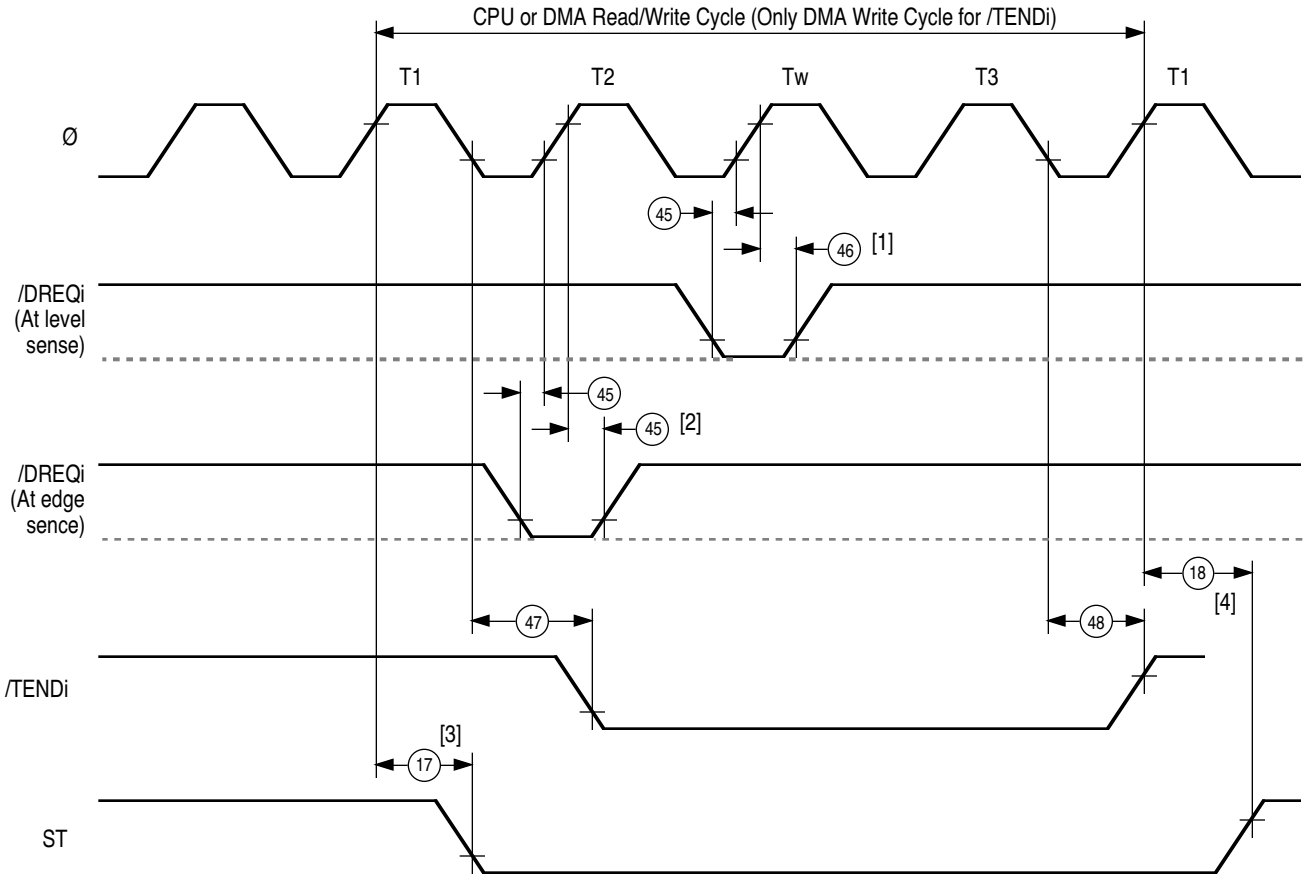


Figure 92. CPU Timing



DMA Control Signals
[1] tDRQS and tDRQH are specified for the rising edge of clock followed by T3.
[2] tDRQS and tDRQH are specified for the rising edge of clock.
[3] DMA cycle starts.
[4] CPU cycle starts.

Figure 93. DMA Control Signals

TIMING DIAGRAMS (Continued)

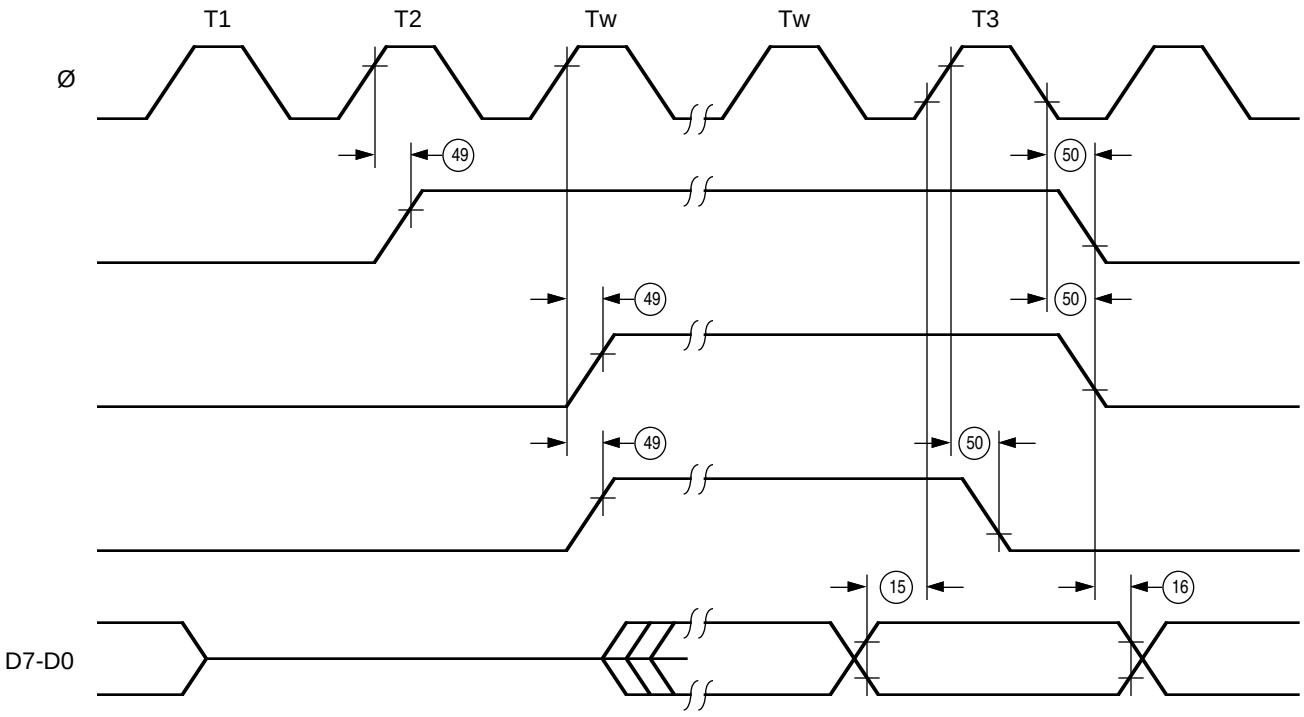


Figure 94. E Clock Timing
(Memory Read/Write Cycle
I/O Read/Write Cycle)

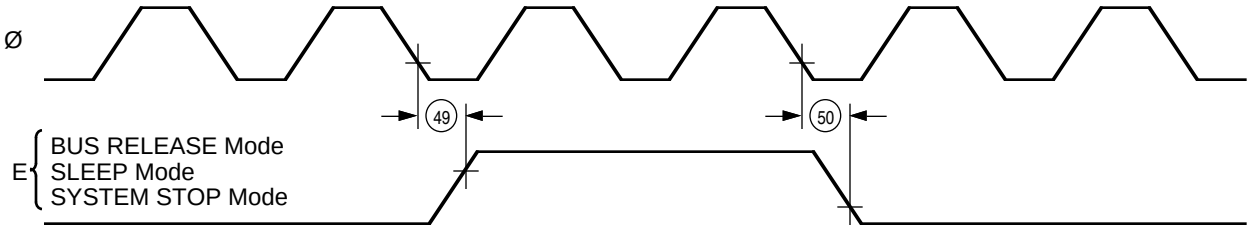


Figure 95. E Clock Timing

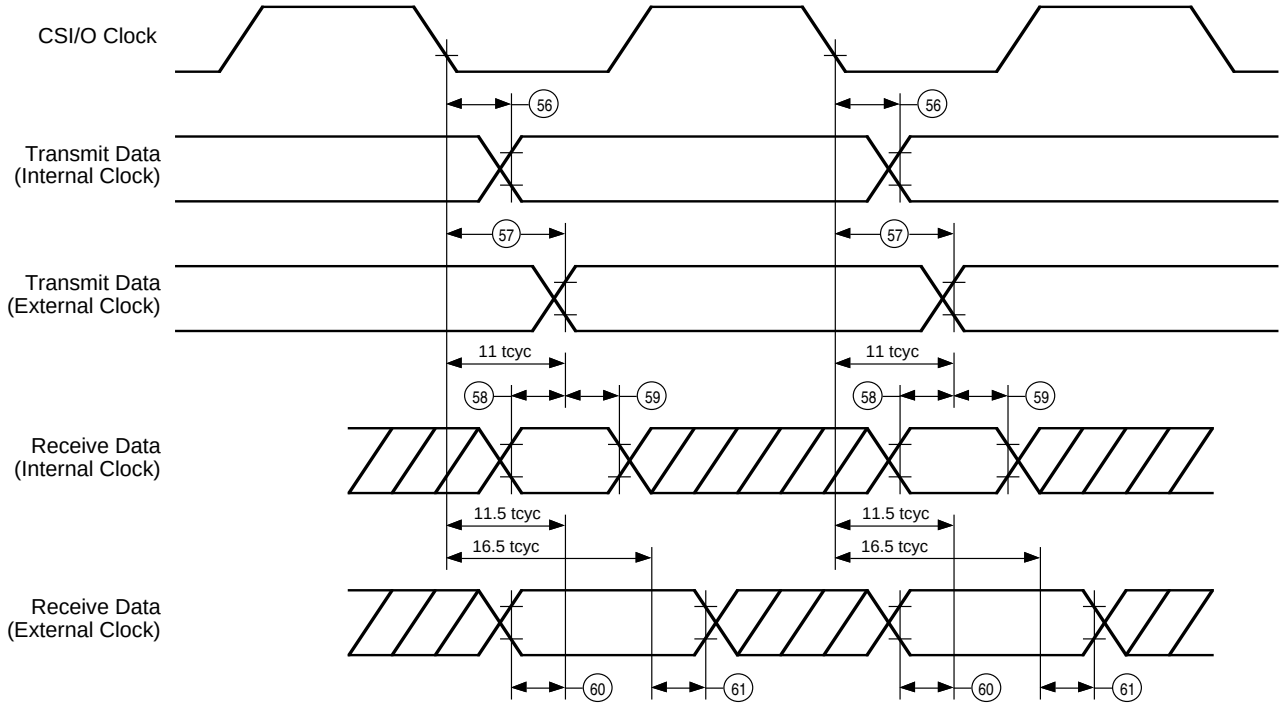


Figure 99. CSI/O Receive/Transmit Timing

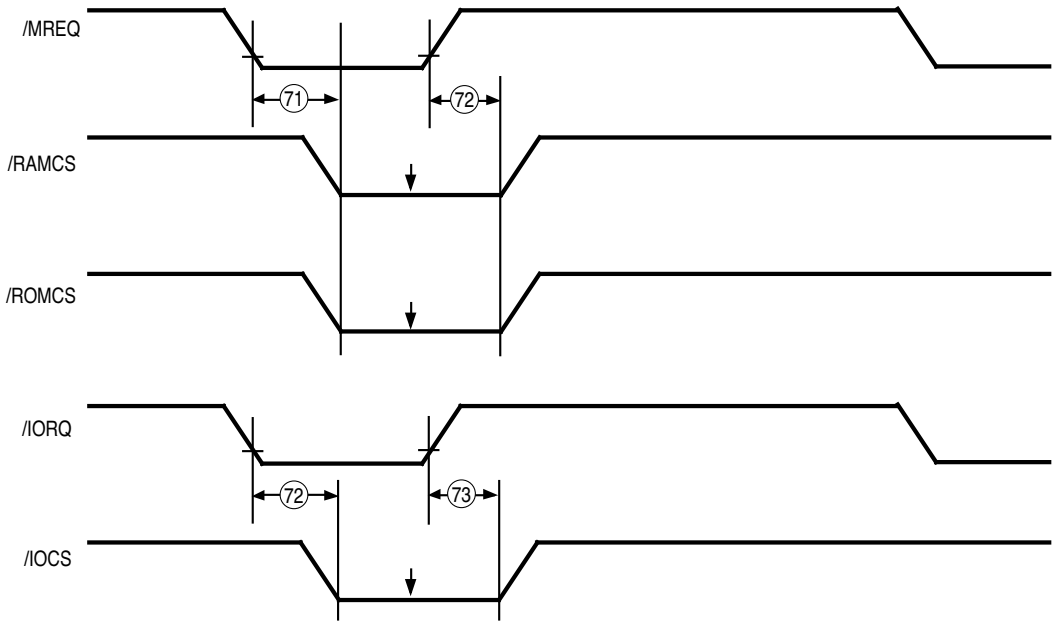


Figure 100 /ROMCS and /RAMCS Timing

Z8S180 AC CHARACTERISTICS (Continued)

No.	Sym	Parameter	Z8L180 20 MHz Min	Z8L180 20 MHz Max	Z8S180 33 MHz Min	Z8S180 33 MHz Max	Unit	Note
41	tRFD1	Clock Rise to /RFSH Fall Delay		20		15	ns	
42	tRFD2	Clock Rise to /RFSH Rise Delay		20		15	ns	
43	tHAD1	Clock Rise to /HALT Fall Delay		15		15	ns	
44	tHAD2	Clock Rise to /HALT Rise Delay		15		15	ns	
45	tDRQS	/DREQi Setup Time to Clock Rise	20		15		ns	
46	tDRQH	/DREQi Hold Time from Clock Rise	20		15		ns	
47	tTED1	Clock Fall to /TENDi Fall Delay		25		15	ns	
48	tTED2	Clock Fall to /TENDi Rise Delay		25		15	ns	
49	tED1	Clock Rise to E Rise Delay		30		15	ns	
50	tED2	Clock Edge to E Fall Delay		30		15	ns	
51	PWEH	E Pulse Width (High)	25		20		ns	
52	PWEL	E Pulse Width (Low)	50		40		ns	
53	tEr	Enable Rise Time		10		10	ns	
54	tEf	Enable Fall Time		10		10	ns	
55	tTOD	Clock Fall to Timer Output Delay		75		50	ns	
56	tSTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		75		60	ns	
57	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5 tcyc+100		7.5 tcyc+100	ns	
58	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)		1	1		tcyc	
59	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)		1	1		tcyc	
60	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)		1	1		tcyc	
61	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)		1	1		tcyc	
62	tRES	/RESET Setup time to Clock Fall	40		25		ns	
63	tREH	/RESET Hold time from Clock Fall	25		15		ns	
64	tOSC	Oscillator Stabilization Time		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		10		5	ns	
66	tEXf	External Clock Fall Time (EXTAL)		10		5	ns	
67	tRr	/RESET Rise Time		50		50	ms	[2]
68	tRf	/RESET Fall Time		50		50	ms	[2]
69	tIr	Input Rise Time (Except EXTAL, /RESET)		50		50	ns	[2]
70	tIf	Input Fall Time (Except EXTAL, /RESET)		50		50	ns	[2]
71	TdCS	/MREQ Valid to /ROMCS, /RAMCS Valid Delay		15		10	ns	
72	TdIOCS	/IORQ Valid to /IOCS Valid Delay		15		10	ns	

Notes:
These AC parameters values are preliminary and subject to change without notice.
[1] All specifications reflect 100% output drive (disabled slew rate limiting feature).
[2] Specification 1 through 5 refer to PHI clock output.
[3] Exceeds characterization (data propagation delay needs to be analyzed).

16550 MIMIC TIMING

Refer to Figures 106 thru 112 for MIMIC AC Timing.

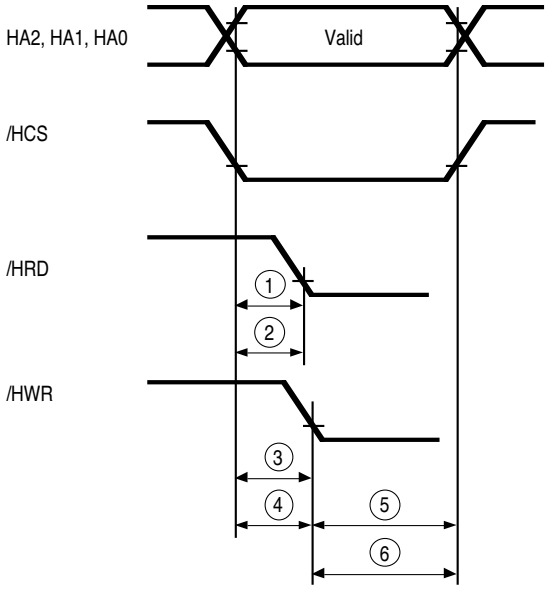


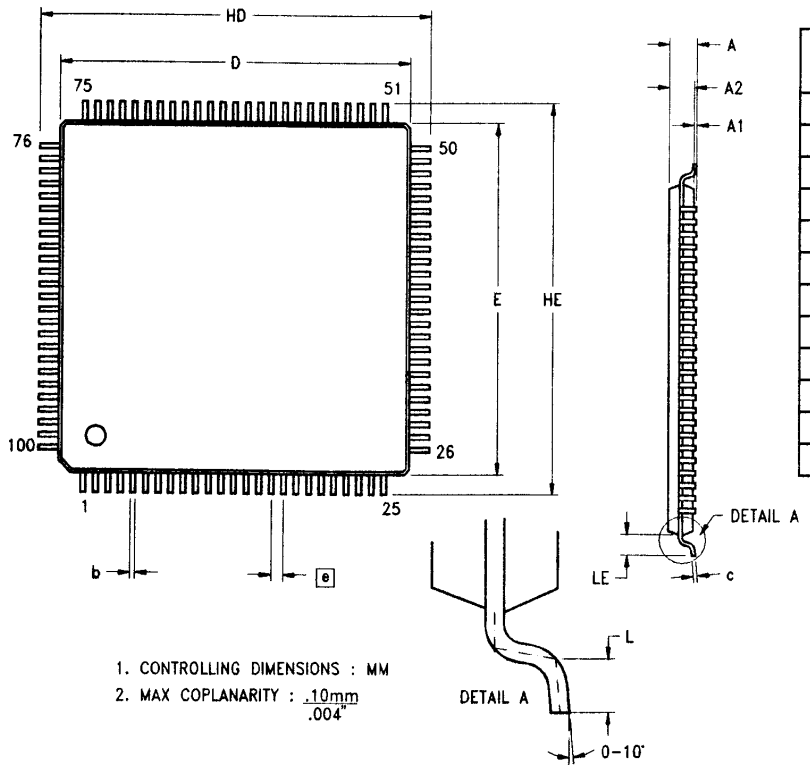
Figure 110. PC Host /RD /WR Timing

Table H. PC Host /RD /WR Timing

No	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
1	tAR	/HRD Delay from Address	30		30		ns
2	tCSR	/HRD Delay from /HCS	30		30		ns
3	tAW	/HWR Delay from Address	30		30		ns
4	tCSW	/HWR Delay from /HCS	30		30		ns
5	tAh	Address Hold Time	20		20		ns
6	tCSh	/HCS Hold Time	20		20		ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.C06	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 TYP		.0197 TYP	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

100-Pin VQFP Package Diagram

ORDERING INFORMATION

Z8L182	Z80182
20 MHz	**33 MHz**
Z8L18220ASC	Z8018233ASC
Z8L18220FSC	Z8018233FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

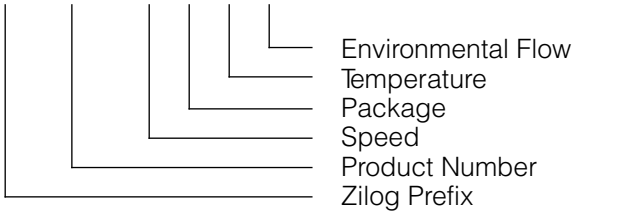
Preferred Package
A = VQFP (Very Small QFP)
F = Plastic Quad Flatpack

Preferred Temperature
S = 0°C to +70°C

Speeds
20 = 20 MHz
33 = 33 MHZ

Environmental
C = Plastic Standard
D = Plastic Stressed
E = Hermetric Standard

Example:
Z 80182 20 F S C is a Z80182, 20 MHz, QFP, 0°C to +70°C, Plastic Standard Flow



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