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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018216asg

Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 4.

Table 4. Multiplexed Port Pins

Port Mode Function	ASCI/ESCC Mode Function
PB7	RxS,/CTS1
PB6 Select with bit 6=1	RxA1
PB5 System Config Reg.	TxA1
PB4	RxA0
PB3	TxA0
PB2 Select with bit 5=1	/DCD0
PB1 System Config Reg.	/CTS0 (Note 1)
PB0	/RTS0
PC7	Always Reads /INT2 Ext. Status
PC6	Always Reads /INT1 Ext. Status
PC5	/W//REQA
PC4	/SYNCA
PC3 Select with bit 7=1	/DTR//REQA
PC2 System Config Reg.	/RTSA (Note 2)
PC1	/CTSA
PC0	/DCDA

Note 1:
When the Port function (PB1) is selected, the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

Note 2:
Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functions.

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source
  - Up to 5 Mbits/sec at 20 MHz PCLK (ESCC).
- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit
- NRZ, NRZI or FM encoding/decoding. Manchester Code Decoding (Encoding with External Logic).
- Baud Rate Generator in each Channel
- Digital Phase-Locked Loop (DPLL) for Clock Recovery
- Crystal Oscillator

The following features are implemented in the ESCC™ for the Z80182/Z8L182 only:

- New 32-bit CRC-32 (Ethernet Polynomial)
- ESCC Programmable Clock
  - programmed to be equal to system clock divided by one or two
  - programmed by Z80182 Enhancement Register

Note: The ESCC™ programmable clock must be programmed to divide-by-two mode when operating above the following conditions:

– PHI > 20 MHz at 5.0V

– PHI > 10 MHz at 3.0V

Z85230 ESCC™ BLOCK DIAGRAM

For a detailed description of the Z85230 ESCC, refer to the ESCC Technical Manual. The following figure is the block diagram of the discrete ESCC, which was integrated into the Z182. The /INT line is internally connected to "INTO of the Z182.

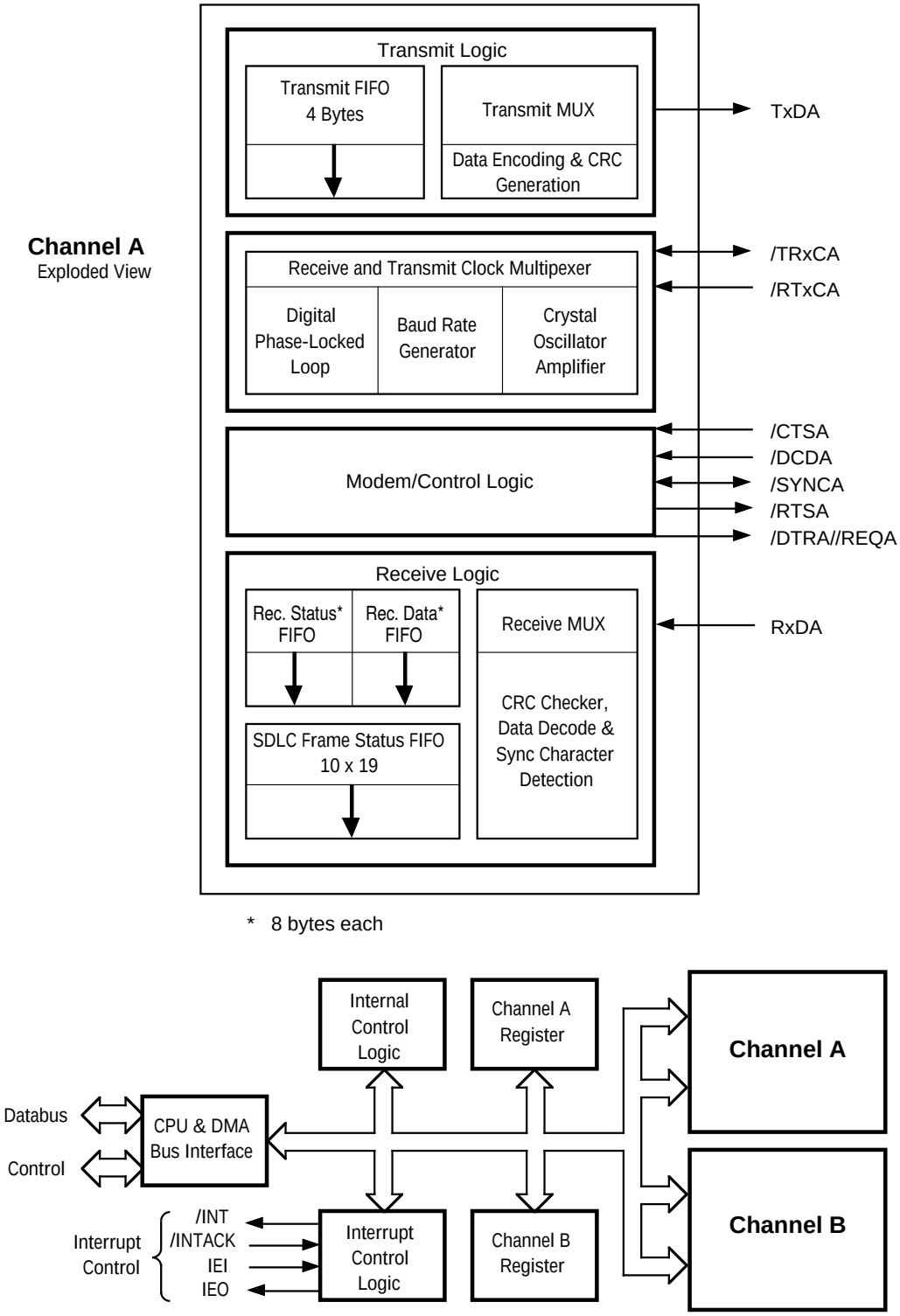


Figure 5. ESCC Block Diagram

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only). The Ports are controlled through two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

PROGRAMMING

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for Z182 peripheral access. The full sixteen address lines are decoded for on-chip Z180 MPU access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers through the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated through the System Configuration Register and the Interrupt Edge/Pin MUX Register.

Table 7. Z80182/Z8L182 MPU Registers

Register Name	MPU Addr	PC Addr
Z80182/Z8L182 MPU Control Registers	0000H to 00x3FH (Relocatable to 0040H to 007FH or 0080H to 00BFH)	None

Note:
"x" indicates don't care condition

Table 8. Z80182/Z8L182 MIMIC Register MAP

Register Name	MPU Addr/Access		PC Addr/Access	
MMC MIMIC Master Control Register	xxFFH	R/W	None	
IUS/IP Interrupt Pending	xxFEH	R/Wb7	None	
IE Interrupt Enable	xxFDH	R/W	None	
IVEC Interrupt Vector	xxFCH	R/W	None	
TTCR Transmit Time Constant	xxFAH	R/W	None	
RTCR Receive Time Constant	xxFBH	R/W	None	
FSCR FIFO Status and Control	xxECH	R/W7-4	None	
RTTC Receive Timeout Time Constant	xxEAH	R/W	None	
TTTC Transmit Timeout Time Constant	xxEBH	R/W	None	
RBR Receive Buffer Register	xxF0H	W only	00H	DLAB=0 R only
THR Transmit Holding Register	xxF0H	R only	00H	DLAB=0 W only
IER Interrupt Enable Register	xxF1H	R only	01H	DLAB=0 R/W
IIR Interrupt Identification	None		02H	R only
FCR FIFO Control Register	xxE9H	R only	02H	W only
MM REGISTER	XXE9H	W only	None	
LCR Line Control Register	xxF3H	R only	03H	R/W
MCR Modem Control Register	xxF4H	R only	04H	R/W
LSR Line Status Register	xxF5H	R/Wb6432	05H	R only
MSR Modem Status Register	xxF6H	R/Wb7-4	06H	R only
SCR Scratch Register	xxF7H	R only	07H	R/W
DLL Divisor Latch (LSByte)	xxF8H	R only	00H	DLAB=1 R/W
DLM Divisor Latch (MSByte)	xxF9H	R only	01H	DLAB=1 R/W

PROGRAMMING (Continued)

Table 9. Z80182/Z8L182 ESCC, PIA and MISC Registers

Register Name	MPU Addr/Access		PC Addr/Access
WSG Chip Select Register	xxD8H	R/W	None
Z80182 Enhancements Register	xxD9H	R/W	None
PC Data Direction Register	xxDDH	R/W	None
PC Data Register	xxDEH	R/W	None
Interrupt Edge/Pin MUX Control	xxDFH	R/W	None
ESCC Chan A Control Register	xxE0H	R/W	None
ESCC Chan A Data Register	xxE1H	R/W	None
ESCC Chan B Control Register	xxE2H	R/W	None
ESCC Chan B Data Register	xxE3H	R/W	None
PB Data Direction Register	xxE4H	R/W	None
PB Data Register	xxE5H	R/W	None
RAMUBR RAM Upper Boundary Register	xxE6H	R/W	None
RAMLBR RAM Lower Boundary Register	xxE7H	R/W	None
ROM Address Boundary Register	xxE8H	R/W	None
PA Data Direction Register	xxEDH	R/W	None
PA Data Register	xxEEH	R/W	None
System Configuration Register	xxEFH	R/W	None

ASCI CHANNELS CONTROL REGISTERS (Continued)

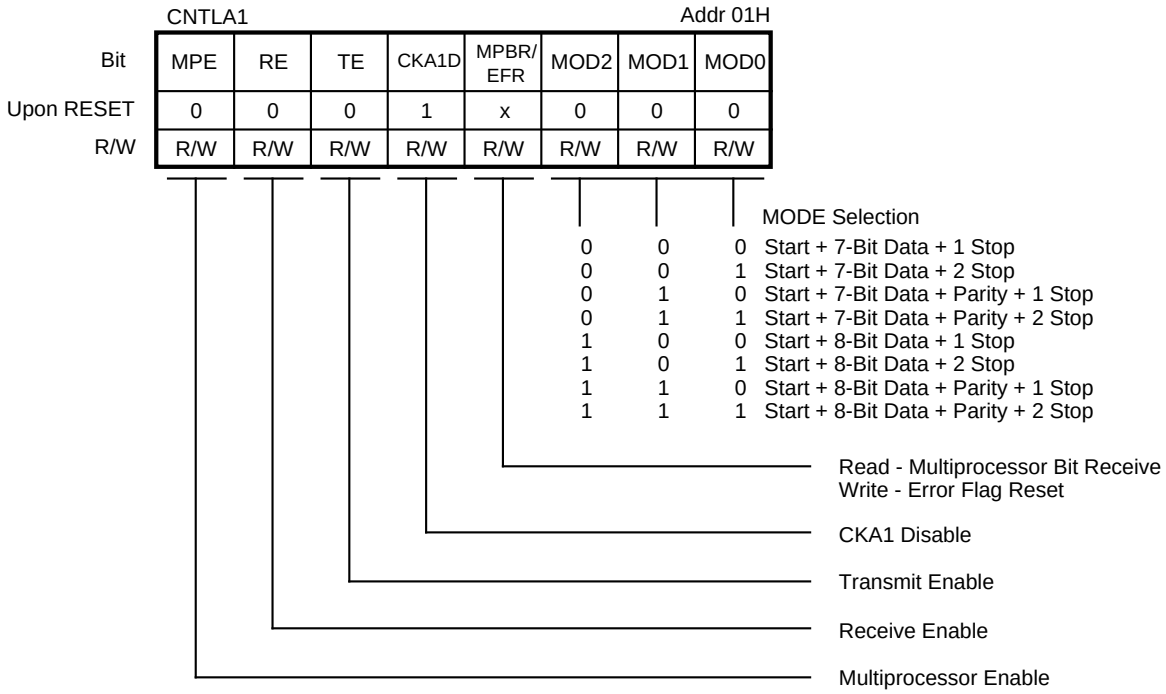


Figure 10b. ASCI Control Register A (Ch. 1)

ASCI CHANNELS CONTROL REGISTERS (Continued)

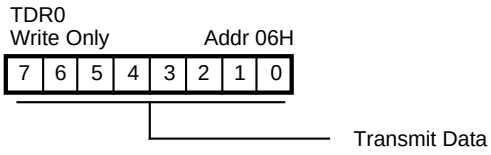


Figure 15. ASCI Transmit Data Register (Ch. 0)

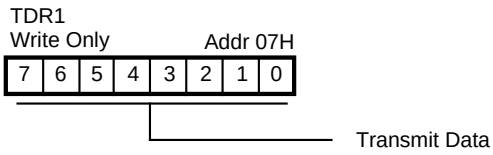


Figure 16. ASCI Transmit Data Register (Ch. 1)

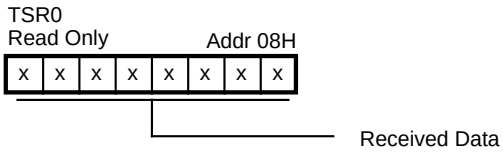


Figure 17. ASCI Receive Data Register (Ch. 0)

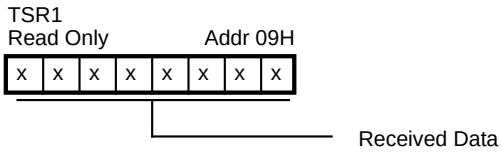


Figure 18. ASCI Receive Data Register (Ch. 1)

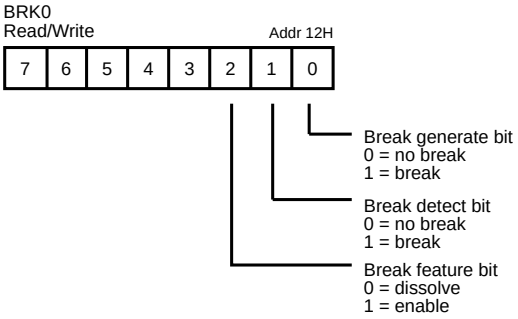


Figure 19. ASCI Break Control Register (Ch. 0)

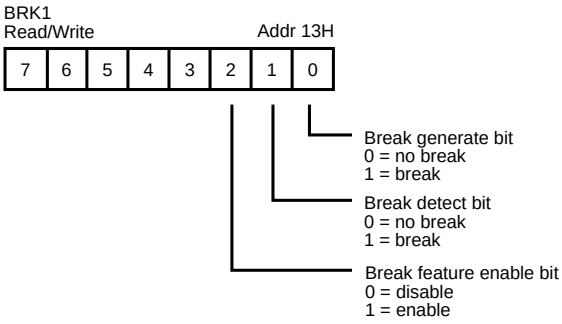
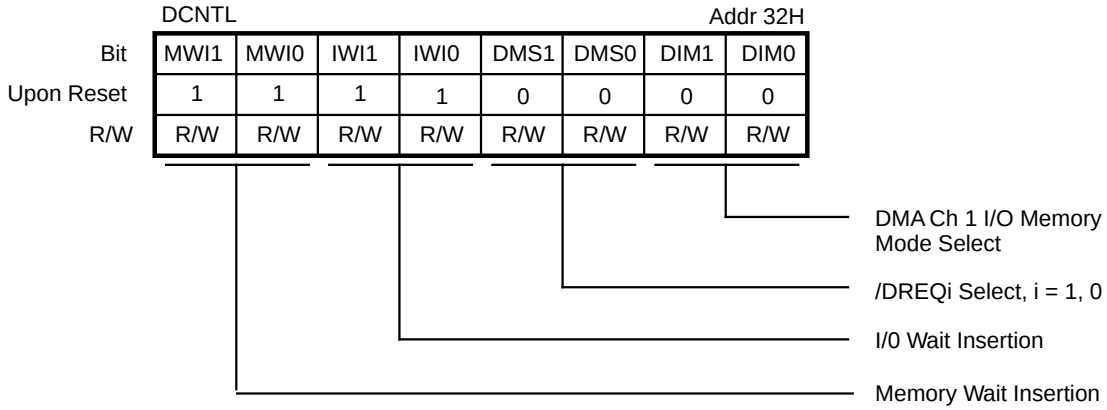


Figure 20. ASCI Break Control Register (Ch. 1)



*

MWI1, 0	No. of Wait States
00	0
01	1
10	2
11	3

IWI1, 0	No. of Wait States
00	1
01	2
10	3
11	4

DMSi	Sense
1	Edge Sense
0	Level Sense

DM1, 0	Transfer Mode	Address Increment/Decrement	
00	M - I/O	MAR1+1	IAR1 Fixed
01	M - I/O	MAR1-1	IAR1 Fixed
10	I/O - M	IAR1 Fixed	MAR1+1
11	I/O - M	IAR1 Fixed	MAR1-1

Note:
* If using ROM/RAM Chip Select wait state generators, the Z180 wait state generator should be set to 0.

Figure 42. DMA/WAIT Control Register

Z85230 ESCC™ CONTROL REGISTERS

See Figures 52 and 53 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification /Technical Manual.

The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. ***It is recommended that /TRxCB be programmed as an output with proper baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.***

Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

Z80182 ENHANCEMENTS REGISTER

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode
If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit is used to allow DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TxDA Tri-state
The TxDA pin can be tri-stated on assertion of the /HALT pin. This prevents the TxDA from driving and external device when /HALT output is used to force other devices into power-down modes. This feature is disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider
The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock will be Z180's PHI clock divided by two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5V or 10 MHz/3V, this bit should be set for ESCC divide-by-two mode.

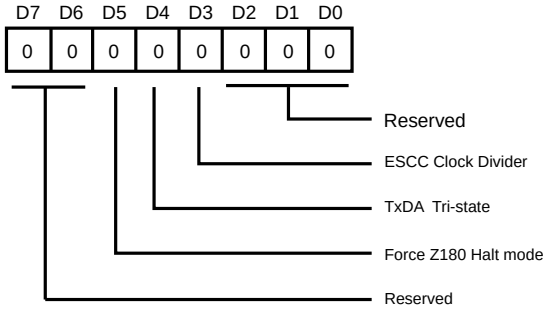


Figure 82. Z80182 Enhancements Register
(Z180 MPU Read/Write, Address xxD9H)

PARALLEL PORTS REGISTERS

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output. The Ports consist of two registers the Port Direction Control Register and the Port Data Register. The Port and direction register can be accessed in any page of I/O space since only the lowest eight address lines are decoded. Bits PC7 and PC6 are input only bits and have the special function of reading the external value of the /INT2 and /INT1 pins. Writing '1' to these bits will clear the edge detect interrupt logic when operating /INT2 and/or /INT1 in edge detect mode.

When Port B and Port C bits 5-0 are deselected in the System Configuration Register, the Data and Data Direction Registers are still available as read/write scratch registers. If a Port is deselected and if the DDR bit is a '0', then the written value to that bit will be latched and this value can be read back. If a Port is deselected and if the DDR bit is a '1', then you could read only the external pin value; any write to that bit is latched but can be read back only with DDR=0.

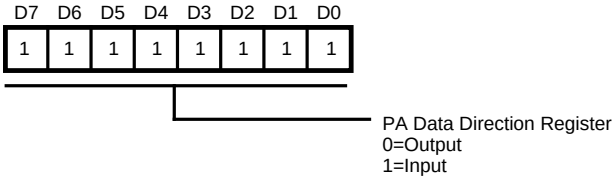


Figure 83. PA, Port A, Data Direction Register
(Z180 MPU Read/Write, Address xxEDH)

The data direction register determines which are inputs and outputs in the PA Data Register. When a bit is set to 1 the corresponding bit in the PA Data Register is an input. If the bit is 0, then the corresponding bit is an output.

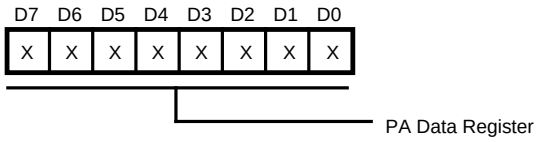


Figure 84. PA, Port A, Data Register
(Z180 MPU Read/Write, Address xxEEH)

When the Z180 MPU writes to the PA Data Register the data is stored in the internal buffer. The values of the PA Data Register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PA Data Register the data on the external pins is returned.

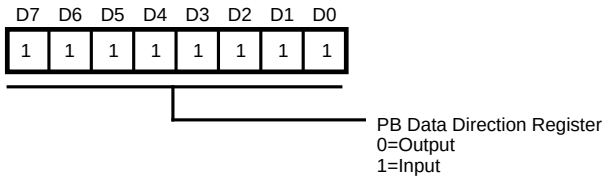


Figure 85. PB, Port B, Data Direction Register
(Z180 MPU Read/Write, Address xxE4H)

The data direction register determines which are inputs and outputs in the PB Data Register. When a bit is set to 1 the corresponding bit in the PB Data Register is an input. If the bit is 0 then the corresponding bit is an output.

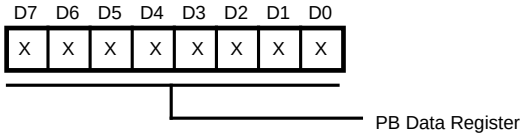


Figure 86. PB, Port B, Data Register
(Z180 MPU, Address xxE5H)

When the Z180 MPU writes to the PB Data Register the data is stored in the internal buffer. The values of Port B data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PB Data Register, the data on the external pins is returned.

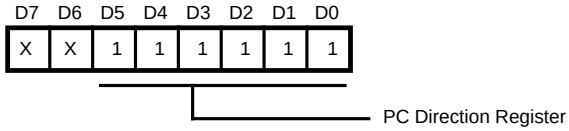


Figure 87. PC, Port C, Data Direction Register
(Z180 MPU Read/Write, Address xxDDH)

Z80182/Z8L182 MIMIC DMA CONSIDERATIONS

For the PC Interface, the 16550 device has two modes of operation that need to be supported by the MIMIC. In single transfer mode, the DMA request line for the receiver goes active whenever there is at least one character in the RCVR FIFO. For the transmitter, the DMA request line is active on an empty XMIT FIFO and inactive on non-empty.

In multi-transfer mode, the RCVR DMA goes active at the trigger level and inactive on RCVR FIFO empty. The XMIT DMA is active on non-full XMIT FIFO and inactive on a full XMIT FIFO.

Bit 3 in the FCR controls the DMA mode for the PC interface. If a 1 is programmed into this bit, multi-byte DMA is enabled. A 0 in this bit (default) enables single byte DMA.

As specified, the 16550 does not have any means of handling the error status bits in the FIFO in this multi-transfer mode. Such DMA transfers would require blocks with some checksum or other error checking scheme.

For the MPU interface, the DMA is controlled by a non-empty transmit FIFO and by a non-full receive FIFO conditions (THRE and the DR bits in the LSR). If the delay timers are enabled, the respective shadow bits are used for DMA control. The effect of the DMA logic is to request DMA service when at least one byte of data is available to be read or written to the FIFO's by the Z180. The Z180's DMA channel can be programmed to trigger on edge or on level.

EMULATION MODES

The Z80182/Z8L182 provides four modes of operation. The modes are selected by the EV1 and EV2 pins. These four modes allow the system development and commercial production to be done with the same device. The four emulation modes are shown in Table 20.

Table 20. EV2 and EV1, Emulation Mode Control

	EV2	EV1	EV Description
Mode 0	0	0	Normal Mode, on-chip Z180 bus master
Mode 1	0	1	Emulation Adapter Mode
Mode 2	1	0	Emulator Probe Mode
Mode 3	1	1	RESERVED, for Test Use Only

Mode 0 Normal Mode

This is the normal operating mode for the Z80182/Z8L182.

Mode 1 Emulation Adapter Mode

The Emulation Adaptor Mode enables system development for the Z182 with a readily available Z180 emulator. The Emulator provides the Z180™ MPU and Z180 peripheral functions to the target system, with their signals passing through the emulation adapter. In Emulation Adaptor Mode the Z182s, Z180 MPU and Z180 peripheral signals are tri-state or physically disconnected. The Z182 continues to provide its ESCC, MIMIC, chip select, and Port functions and signals to the target system. The Mode 1 effects on the Z182 are shown in Table 21. Note that INT1-2 Edge Detect Logic cannot be used in Emulation Adaptor EV Mode 2.

TIMING DIAGRAMS (Continued)

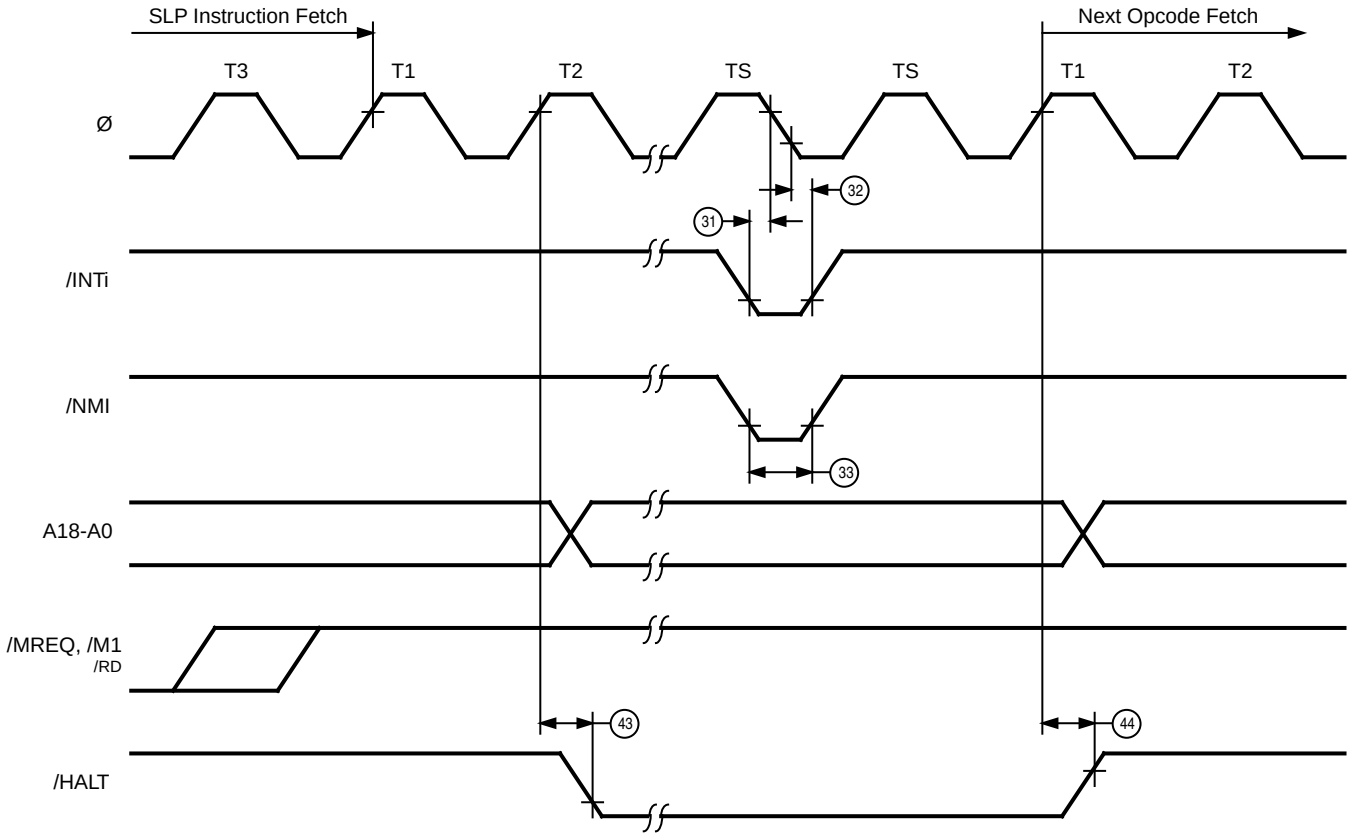


Figure 98. SLEEP Execution Cycle

Z8S180 AC CHARACTERISTICS

Table A. Z8L180 and Z8S180 Timings

No.	Sym	Parameter	Z8L180 20 MHz Min	Z8L180 20 MHz Max	Z8S180 33 MHz Min	Z8S180 33 MHz Max	Unit	Note
1	tcyc	Clock Cycle Time	50	2000	30	2000	ns	[1]
2	tCHW	Clock Pulse Width (High)	15		10		ns	[1]
3	tCLW	Clock Pulse Width (Low)	15		10		ns	[1]
4	tcf	Clock Fall Time		10		5	ns	[1]
5	tcr	Clock Rise Time		10		5	ns	[1]
6	tAD	Address Valid from Clock Rise		15		15	ns	
7	tAS	Address Valid to /MREQ, /IORQ, /MRD Fall	5		5		ns	
8	tMED1	Clock Fall to /MREQ Fall Delay		15		10	ns	
9	tRDD1	Clock Fall to /RD, /MRD (/IOC=1)		25		15	ns	
		Clock Rise to /RD, /MRD Fall (/IOC=0)		35		15	ns	
10	tM1D1	Clock Rise to /M1 Fall delay		35		15	ns	
11	tAH	Address Hold time (/MREQ, /IORQ, /RD, /WR/MRD)	5		5		ns	
12	tMED2	Clock Fall to /MREQ Rise Delay		25		15	ns	
13	tRDD2	Clock Fall to /RD, /MRD Rise Delay		25		15	ns	
14	tM1D2	Clock Rise to /M1 Rise Delay		40		15	ns	
15	tDRS	Data Read Setup Time	15		15		ns	
16	tDRH	Data Read Hold Time	0		0		ns	
17	tSTD1	Clock Edge to ST Fall		30		15	ns	
18	tSTD2	Clock Edge to ST Rise		30		15	ns	
19	tWS	/WAIT Setup Time to Clock Fall	15		10		ns	[2]
20	tWH	/WAIT Hold Time from Clock Fall	10		5		ns	
21	tWDZ	Clock Rise to Data Float Delay		35		20	ns	
22	tWRD1	Clock Rise to /WR,/MWR Fall Delay		25		15	ns	
23	tWDD	Clock Fall to Write Data Delay		25		15	ns	
24	tWDS	Write Data Setup Time to /WR,/MWR Fall	10		10		ns	
25	tWRD2	Clock Fall to /WR Rise		25		15	ns	
26	tWRP	/WR Pulse Width (Memory Write Cycles)	75		45		ns	
26a		/WR Pulse Width (I/O Write Cycles)	130		70		ns	
27	tWDH	Write Data Hold Time from /WR Rise	10		5		ns	
28	tIOD1	Clock Fall to /IORQ Fall Delay (/IOC=1)		25		15	ns	
		Clock Rise to /IORQ Fall Delay (/IOC=0)		25		15	ns	
29	tIOD2	Clock Fall /IOQR Rise Delay		25		15	ns	
30	tIOD3	/M1 Fall to /IORQ Fall Delay	100		80		ns	
31	tINTS	/INT Setup Time to Clock Fall	20		15		ns	
32	tINTH	/INT Hold Time from Clock Fall	10		10		ns	
33	tNMIW	/NMI Pulse Width	35		25		ns	
34	tBRS	/BUSREQ Setup Time to Clock Fall	10		10		ns	
35	tBRH	/BUSREQ Hold Time from Clock Fall	10		10		ns	
36	tBAD1	Clock Rise to /BUSACK Fall Delay		25		15	ns	
37	tBAD2	Clock Fall to /BUSACK Rise Delay		25		15	ns	
38	tBZD	Clock Rise to Bus Floating Delay Time		40		30	ns	
39	tMEWH	/MREQ Pulse Width (High)	35		25		ns	
40	tMEWL	/MREQ Pulse Width (Low)	35		25		ns	

ESCC Timing

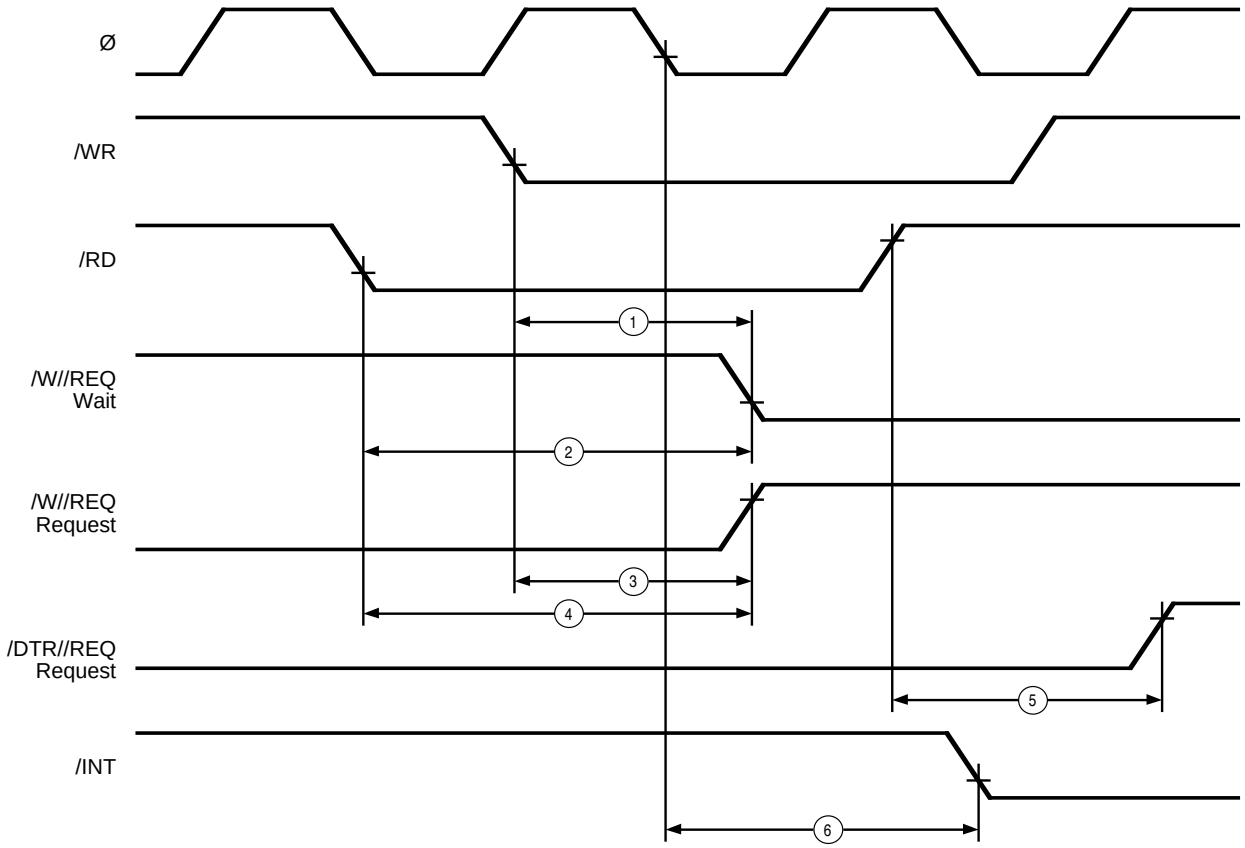


Figure 104. ESCC AC Parameter

Table B. ESCC Timing Parameters

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Unit
1	TdWR(W)	/WR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50	
3	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		65	
4	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		65	
5	TdRdr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay		TBD	
6	TdPC(INT)	Clock to /INT Valid Delay		160	

General-Purpose I/O Port Timing

This figure shows the timing for the Ports A, B and C. Parameters referred to in this figure appear in Tables D and E.

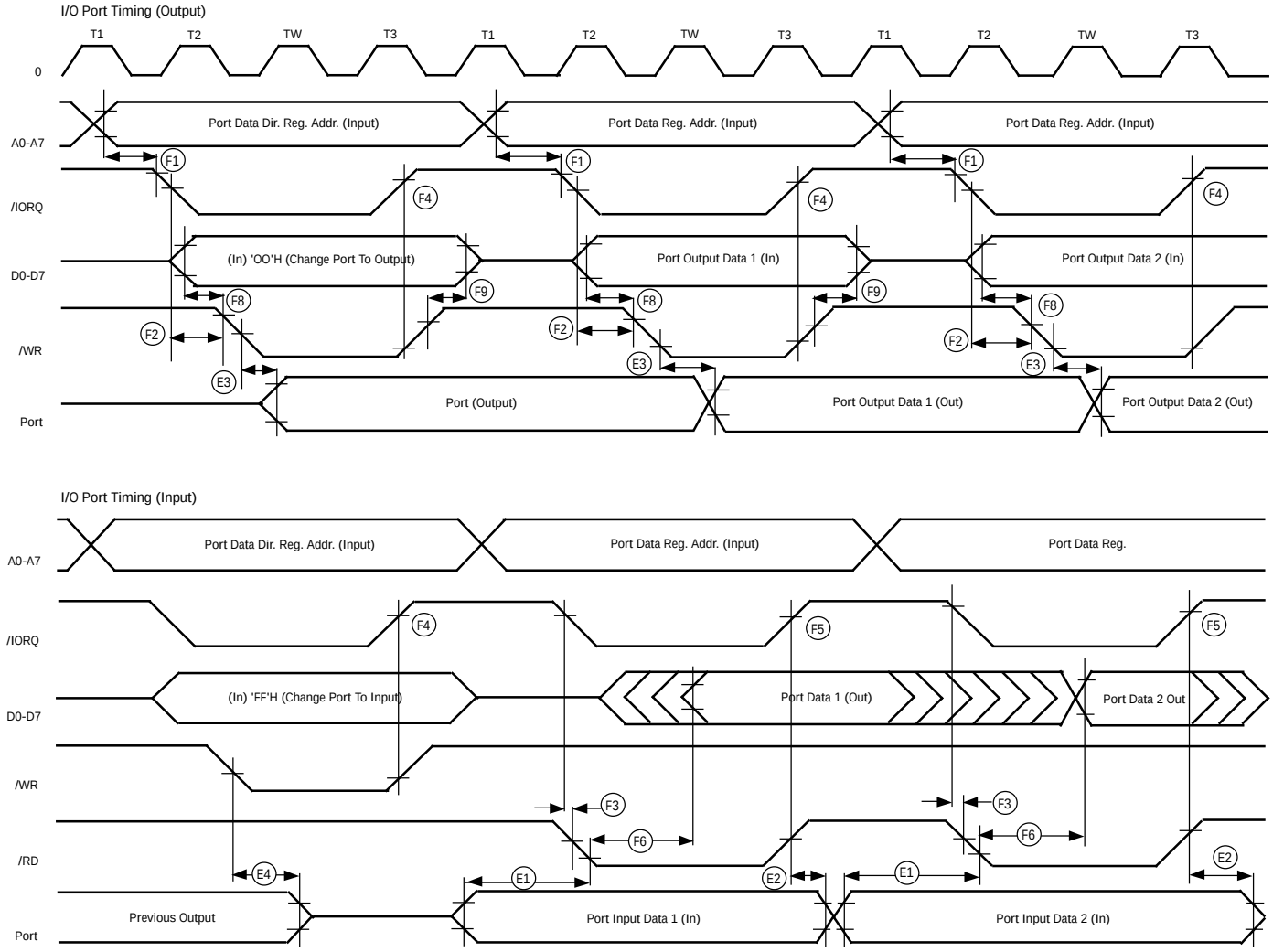


Figure 107. PORT Timing

Read Write External Bus Master Timing

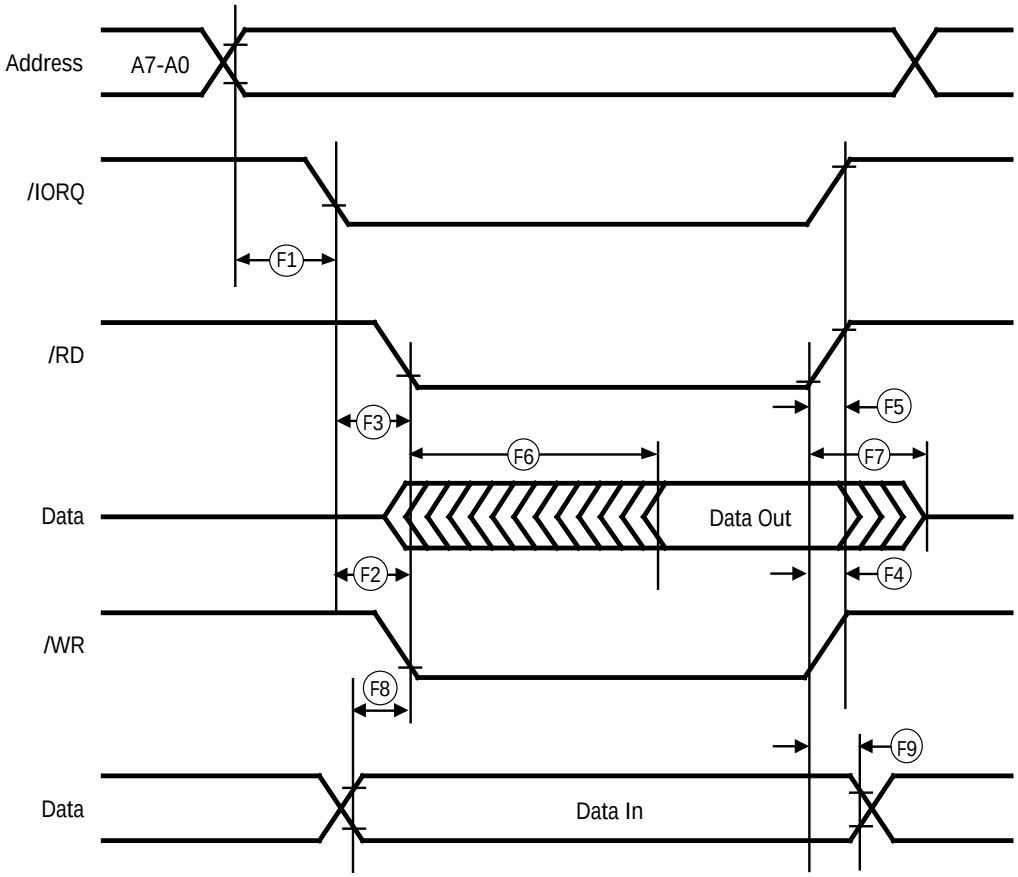


Figure 108. Read/Write External Bus Master Timing

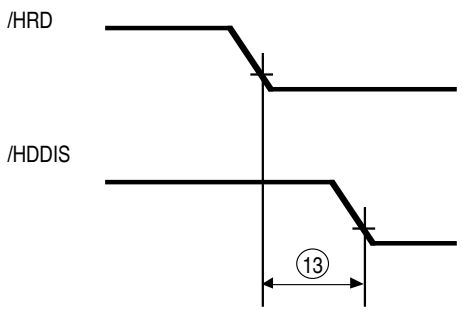


Figure 113. Driver Enable Timing

Table J. Driver Enable Timing

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
13	tRDD	/HRD to Driver Enable/Disable		60		60	ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

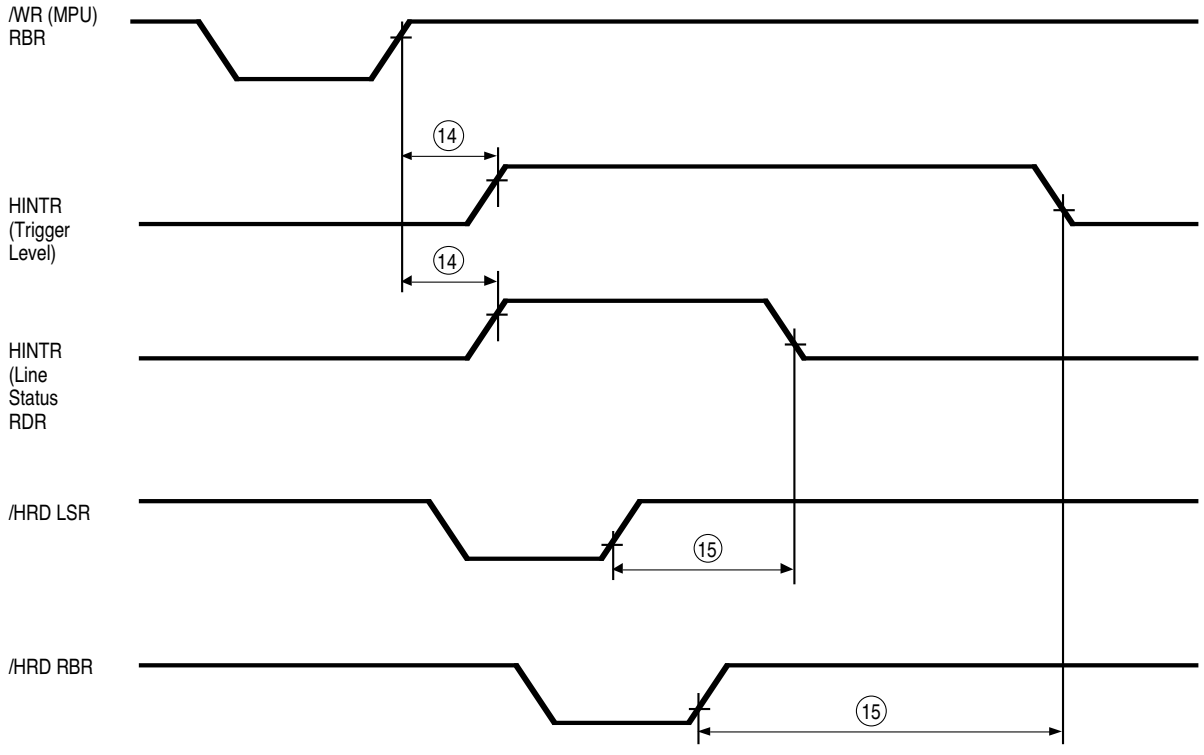


Figure 114. Interrupt Timing RCVR FIFO