Zilog - Z8018216ASG1838 Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-LQFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018216asg1838

Z180 CPU SIGNALS (Continued)

/NMI. *Non-maskable interrupt (input, negative edge triggered).* /NMI has a higher priority than /INT and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.

/INT0. *Maskable Interrupt Request 0 (input/output active Low).* This signal is generated by external I/O devices. The CPU will honor this request at the end of the current instruction cycle as long as the /NMI and /BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the /M1 and /IORQ signals become active. The internal Z180 MPU's /INT0 source is: /INT0 or ESCC or the MIMIC. This input is level triggered. /INT0 is an open-drain output, so you can connect other open-drain interrupts onto the circuit in addition to haveing a pull-up to VCC.

/INT1, /INT2. *Maskable Interrupt Requests 1 and 2 (inputs, active Low).* This signal is generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the /NMI, /BUSREQ, and /INT0 signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for /INT0, during this cycle neither the /M1 or /IORQ signals become active. These pins may be programmed to provide an active Low level on rising or falling edge interrupts. The level of the external /INT1 and /INT2 pins may be read through bits PC6 and PC7 of parallel Port C. Pin /INT1/PC6 multiplexes /INT1 and PC6. Pin /INT2/PC7 multiplexes /INT2 and PC7.

/RFSH. *Refresh (input/output, active Low, tri-state).* Together with /MREQ, /RFSH indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7-A0) contain the refresh address. This signal is analogous to the /REF signal of the Z64180.

Z180 MPU UART AND SIO SIGNALS

CKA0, CKA1. *Asynchronous Clocks 0 and 1 (bi-directional, active High).* These pins are the transmit and receive clocks for the synchronous channels. CKA0 is multiplexed with /DREQ0 on the CKA0//DREQ0 pin. CKA1 is multiplexed with /TEND0 on the CKA1//TEND0 pin.

CKS. *Serial Clock (bi-directional, active High).* This line is clock for the CSIO channel and is multiplexed with the ESCC signal (/W//REQB) and the 16550 MIMIC interface signal /HTxRDY on the CKS//W//REQB//HTxRDY pin.

/DCD0. *Data Carrier Detect 0 (input, active Low).* This is a programmable modem control signal for ASCI channel 0. /DCD0 is multiplexed with the PB2 (parallel Port B, bit 2) on the /DCD0/PB2 pin.

/RTS0. *Request to Send 0 (output, active Low).* This is a programmable modem control signal for ASCI channel 0. This pin is multiplexed with PB0 (parallel Port B, bit 0) on the /RTS0/PB0 pin.

/CTS0. *Clear to Send 0 (input, active Low).* This line is a modem control signal for the ASCI channel 0. This pin is multiplexed with PB1 (parallel Port B, bit 1) on the /CTS0 /PB1 pin.

TxA0. *Transmit Data 0 (output, active High).* This signal is the transmitted data from the ASCI channel 0. This pin is multiplexed with PB3 (parallel Port B, bit 3) on the TxA0/PB3 pin.

TxS. *Clocked Serial Transmit Data (output, active High).* This line is the transmitted data from the CSIO channel. TxS is multiplexed with the ESCC signal (/DTR//REQB) and the 16550 MIMIC interface signal HINTR on the TxS//DTR //REQB//HINTR pin.

RxA0. *Receive Data 0 (input, active High).* This signal is the receive data to ASCI channel 0. This pin is multiplexed with PB4 (parallel Port B, bit 4) on the RxA0/PB4.

RxS. *Clocked Serial Receive Data (input, active High).* This line is the receive data for the CSIO channel. RxS is multiplexed with the /CTS1 signal for ASCI channel 1 and with PB7 (parallel Port B, bit 7) on the RxS//CTS1/PB7 pin.

RxA1. *Received Data ASCI channel 1 (input, active High).* This pin is multiplexed with PB6 (parallel Port B, bit 6) on the RxA1/PB6 pin.

TxA1. *Transmitted Data ASCI Channel 1 (output, active High).* This pin is multiplexed with PB5 (parallel Port B, bit 5) on the TxA1/PB5 pin.

MULTIPLEXED PIN DESCRIPTIONS

A18/$T_{OUT.}$ During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, The T_{OUT} function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/T_{OUT}. Therefore, the selection of T_{OUT} will not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

CKA0//DREQ0. During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, /DREQ0 function is always selected.

CKA1//TEND0. During Reset, this pin is initialized as CKA1 pin. If CKA1D bit in the ASCI control register Ch1(CNTLA1) is set to 1, /TEND0 function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

RxS//CTS1. During Reset, this pin is initialized as the RxS pin. If CTS1E bit in the ASCI status register Ch1 (STAT1) is set to 1, /CTS1 function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 2 specifies. On Reset, both bits 1 and 2 are 0, so /TEND1,TxS,CKS are selected.

Table 2. Triple Multiplexed Pins

Bit 1	Bit 2	Master Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/RTSB,/DTR//REQB,/W//REQB
1	0	/TEND1,TxS,CKS
1	1	/HRxRDY,//HTxRDY,HINTR

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is 0, then the Z80182/Z8L182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is 1, then Z80182/Z8L182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182/Z8L182 Mode 0 is always selected as shown in Table 3.

Table 3. Mode 0 and Mode 1 Multiplexed Pins

Z80182/Z8L182 Mode 0	Z80182/Z8L182 Mode 1
TxDB	/HDDIS
RxDB	HA1
/TRxCB	HA0
/RTxCB	HA2
/SYNCB	/HCS
/CTSB	/HWR
/DCDB	/HRD
PA7-PA0	HD7-HD0

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

16550 MIMIC FIFO DESCRIPTION (Continued)

The PC interface may be interrupted when 1, 4, 8 or 14 bytes are available in the receiver FIFO by setting bits 6 and 7 in the FCR (FIFO Control Register, PC address 02H) to the appropriate value. If the FIFO is not empty, but below the above trigger value, a timeout interrupt is available if the receiver FIFO is not written by the MPU or read by the PC from an interval determined by the Character Timeout Timer. This is an additional Timer with MPU access only that is used to emulate the 16550 4 character timeout delay.

The Receive FIFO timeout timers are designed to reload and begin countdown after every read or write of the Rx FIFO, regardless of the Rx trigger level or number of bytes in the FIFO. Therefore, it is possible to get Timeout interrupts more often than Receive data interrupts. In order to closely emulate a 16550, a receive timeout timer enhancement is provided. When enabling this feature, the timeout timer will not begin counting down until the character emulation timer for each byte of data in the Rx FIFO has expired. ***Note: Enabling this feature will facilitate increased 16550 compatibility but may impede throughput.*** If the Receive Timeout interrupt occurs, the PC HOST will only be allowed to read up to 4-5 consecutive characters before the Data Ready bit is forced to zero (even if there is still more data in FIFO). This is required to maintain character pacing.

The timer receives the ESCC /TRxCB as its input clock. Software must determine the correct values to program into the Receiver Timeout register and the ESCC TRxCB to achieve the correct delay interval for timeout. These interrupts are cleared by the FIFO reaching the trigger point or by resetting the Timeout Interval Timer by FIFO MPU write or PC read access.

With FIFO mode enabled, the MPU is interrupted when the receiver FIFO is empty, corresponding to bit 5 being set in the IUS/IP register (MPU access only). This bit corresponds to a PC read of the receive buffer in non-FIFO (16450) mode. The interrupt source is cleared when the FIFO becomes non-empty or the MPU reads the IUS/IP register.

The transmitter FIFO is 16-byte FIFO with PC write and MPU read access (Figure 8). In FIFO mode, the PC receives an interrupt when the transmitter becomes empty corresponding to bit 5 being set in the LSR. This bit and the interrupt source are cleared when the transmit FIFO becomes non-empty or the Interrupt Identification Register (IIR) register is read by the PC.

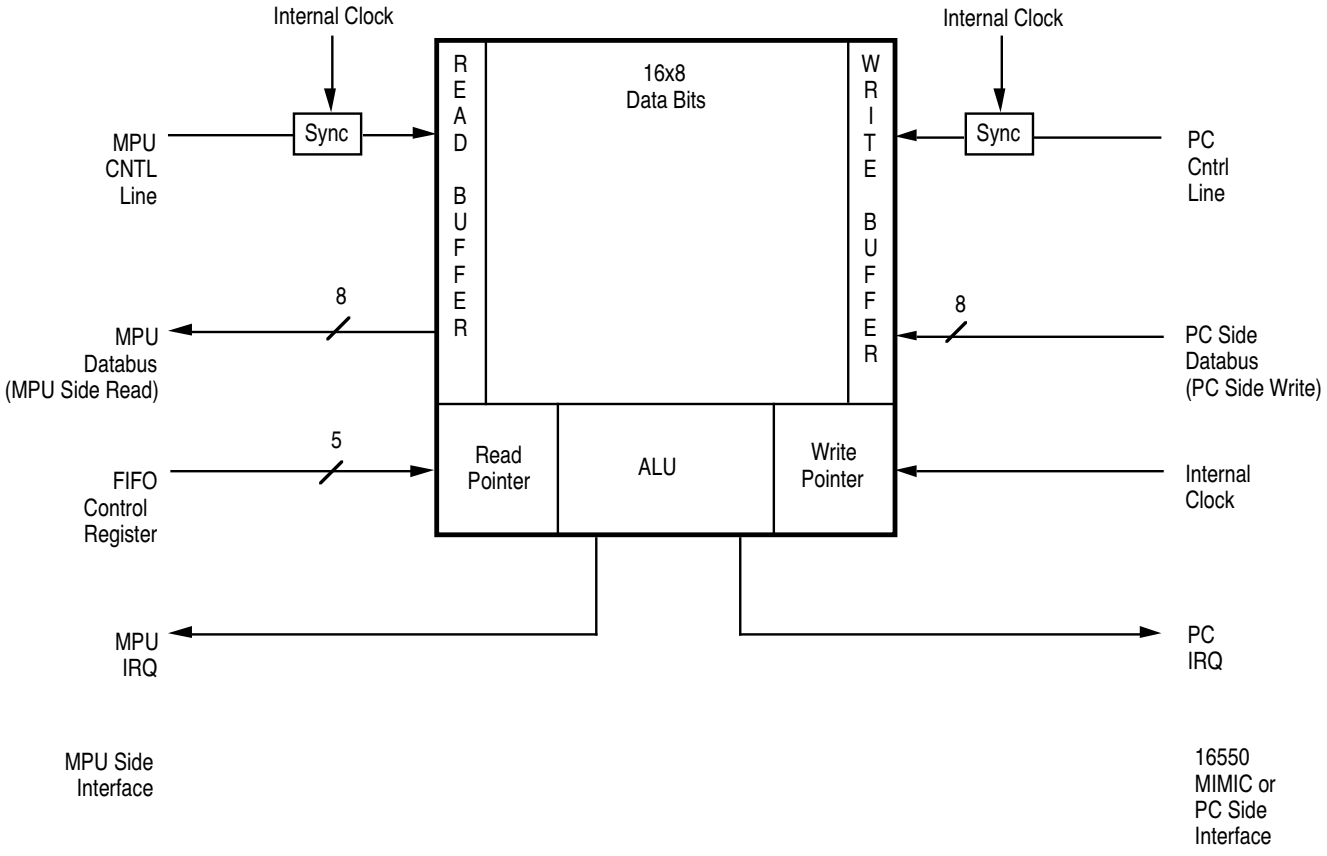


Figure 8. 16550 MIMIC Transmitter FIFO Block Diagram

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

Z182 MPU CONTROL REGISTERS

Figures 10 through 50 refer to the Z80182/Z8L182 MPU Control registers. For additional information, refer to the Z8S180 Product Specification and Technical Manual.

ASCI CHANNELS CONTROL REGISTERS

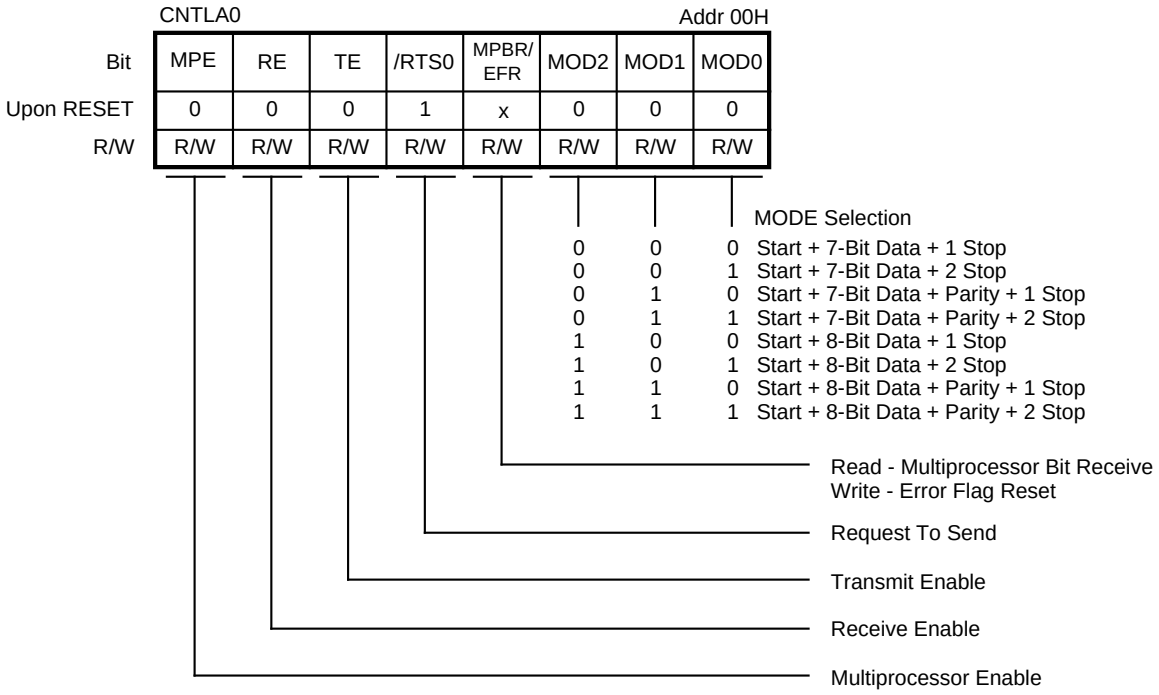


Figure 10a. ASCI Control Register A (Ch. 0)

FREE RUNNING COUNTER

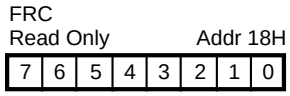


Figure 32. Free Running Counter

CPU CONTROL REGISTER

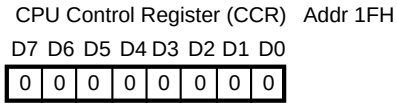
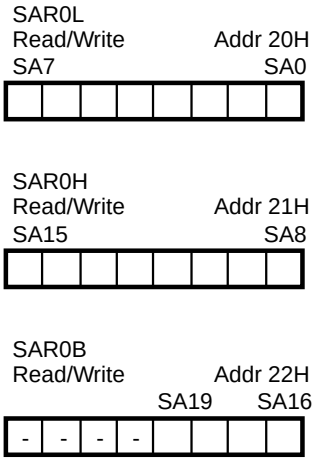


Figure 33. CPU

Note: See Figure 49 for full description.

DMA REGISTERS



Bits 0-2 (3) are used for SAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	RDR1 (ASCI1)
x	x	1	1	Not Used

Figure 34. DMA 0 Source Address Registers

DMA REGISTERS (Continued)

DSTAT — Addr 30H

Bit	DE1	DE0	/DWE1	/DWE0	DIE1	DIE0	-	DIME
Upon Reset	0	0	1	1	0	0	1	0
R/W	R/W	R/W	W	W	R/W	R/W		R

- DIME: DMA Master Enable
- DIE1, DIE0: DMA Interrupt Enable 1, 0
- /DWE1, /DWE0: DMA Enable Bit Write Enable 1, 0
- DE1, DE0: DMA Enable Ch 1, 0

Figure 40. DMA Status Register

DMODE — Addr 31H

Bit	-	-	DM1	DM0	SM1	SM0	MMOD	-
Upon Reset	1	1	0	0	0	0	0	1
R/W			R/W	R/W	R/W	R/W	R/W	

- MMOD: Memory MODE Select
- SM1, SM0: Ch 0 Source Mode 1, 0
- DM1, DM0: Ch 0 Destination Mode 1, 0

DM1, 0	Destination	Address
00	M	DAR0+1
01	M	DAR0-1
10	M	DAR0 Fixed
11	I/O	DAR0 Fixed

SM1, 0	Source	Address
00	M	SAR0+1
01	M	SAR0-1
10	M	SAR0 Fixed
11	I/O	SAR0 Fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

Figure 41. DMA Mode Registers

CONTROL REGISTERS (Continued)

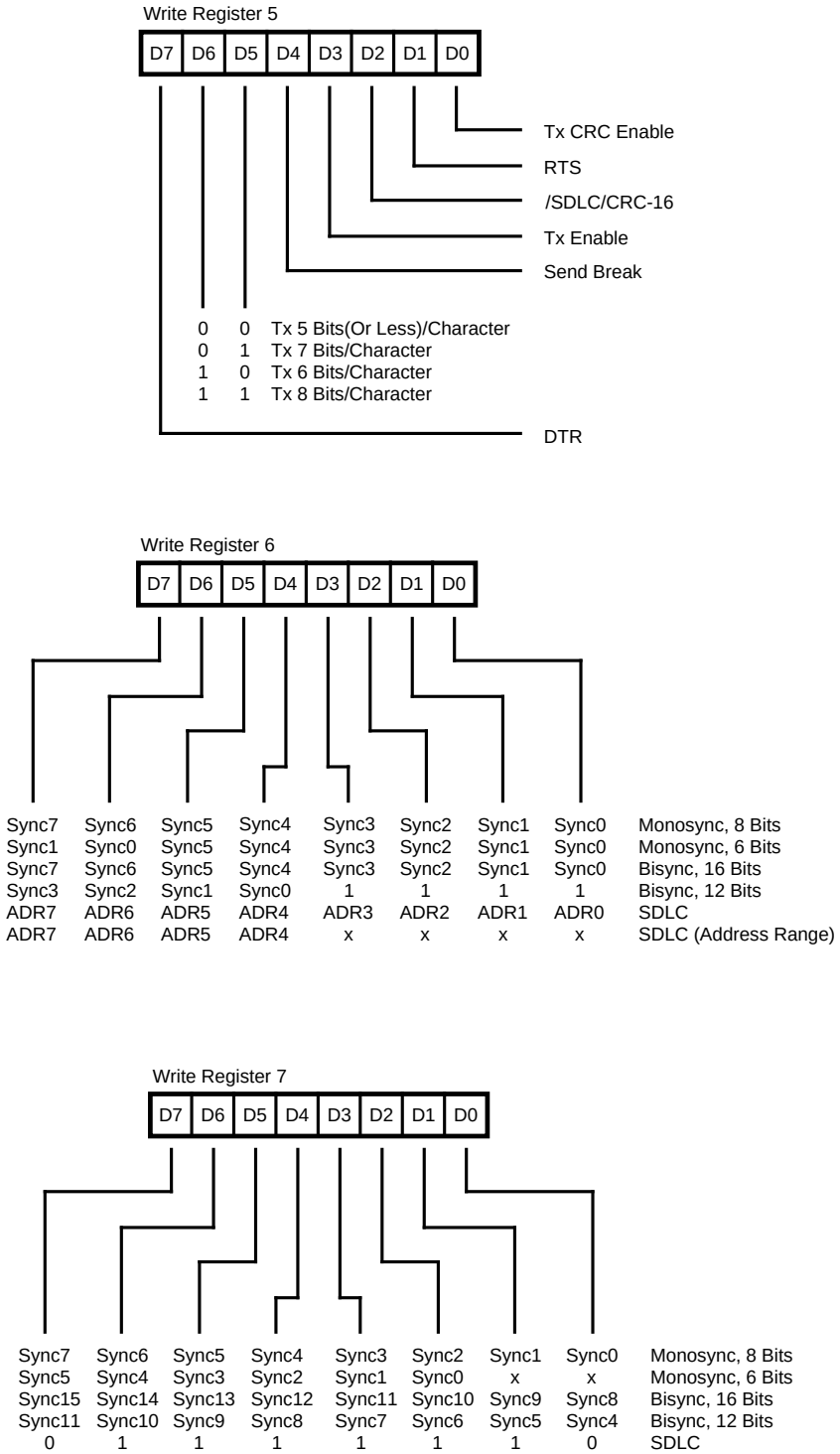


Figure 52. Write Register Bit Functions (Continued)

CONTROL REGISTERS (Continued)

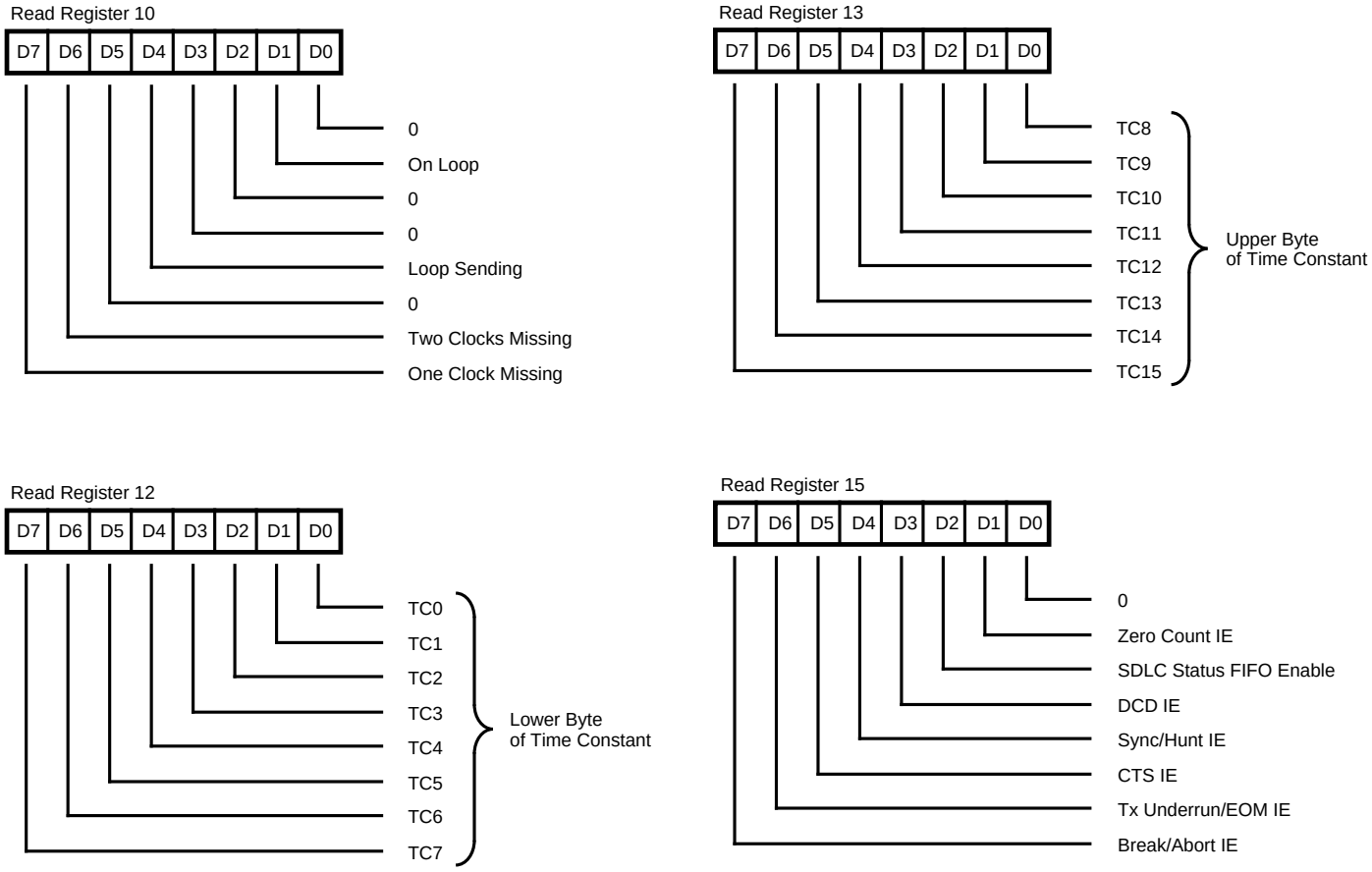


Figure 53. Read Register Bit Functions

INTERRUPT EDGE/PIN MUX REGISTER

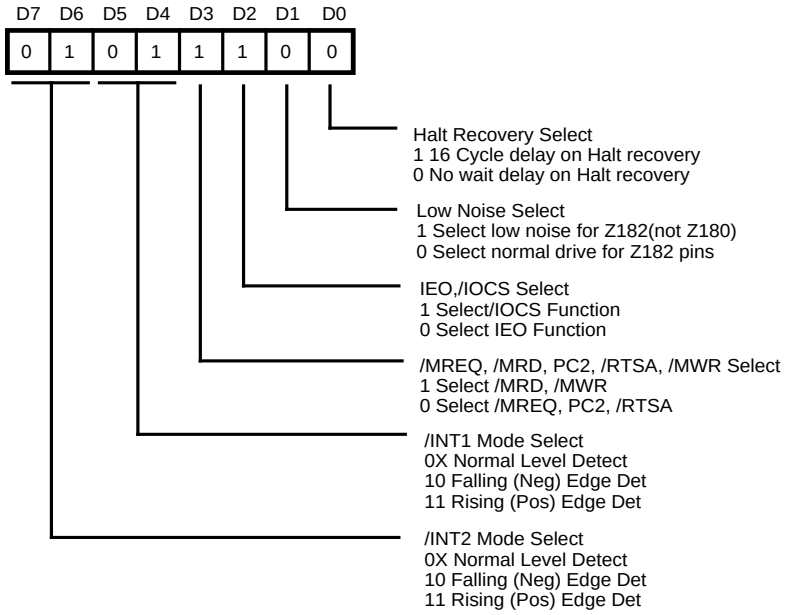


Figure 59. Interrupt Edge/Pin MUX Register
(Z180 MPU Read/Write, Address xxDFH)

Bits 7-6. These bits control the interrupt capture logic for the external /INT2 PIN. When programmed as '0X', the /INT2 pin performs as the normal level detecting interrupt pin. When programmed as 10 the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT2 of the Z180. This interrupt must be cleared by writing a 1 to bit 7 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge.

Bits 5-4. These bits control the interrupt capture logic for the external /INT1 PIN. When programmed as '0X', the /INT1 pin performs as the normal level detecting interrupt pin. When programmed as 10, the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT1 of the Z180. This interrupt must be cleared by writing a 1 to bit 6 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge. Edge detect logic cannot be used in Emulation Adaptor EV mode 1.

Bit 3. Programming this bit to 1 selects the /MRD and the /MWR functions. The default for power up and /RESET conditions is 1, i.e., the /MRD and /MWR. By programming this bit to 0 the /MREQ Z180 function is enabled, as well as the PC2//RTSA function on the PC2//RTSA//MWR pin. If the /MREQ Z180 function is enabled, any external bus master must be prevented from asserting Z182's IRD signal unless accessing Z182's IO.

Bit 2. This bit selects the /IOCS function which is the default for power up and /RESET conditions. By programming this bit to 0 the IEO function is enabled for this multiplexed pin.

Bit 1. This bit selects the low noise or normal drive feature for the Z182 pins . The default at power up is normal drive for Z182 pins. By programming this bit to 1, low noise for the Z182 pins is chosen and the output drive capability of the following pins is reduced to 25% of the original drive capability:

- CKS
- CKA1/TEND0
- CKA0/DREQ0
- RxS/CTS1
- TxA1
- TxA0
- TxS

Programming this bit to 0 selects normal drive for the Z182 pins. Refer to the Z8S180 Product Specification for Low noise control of Z180 pins.

INTERRUPT EDGE/PIN MUX REGISTER (Continued)

Bit 0. Programming this bit to 1 selects a 16 cycle wait delay on recovery from HALT. Halt Recovery is disabled if bit 5 of the enhancement register is set to 1. A 0 selects no wait delay on Halt recovery.

If Halt Recovery is selected, the following pins assume the following states during halt and during the recovery, whether it is in HALT, SLP, IDLE or STBY Modes:

Address	=	Z
Data Bus	=	Z
RD	=	Z
WR	=	Z
MREQ/MRD	=	Z
M1	=	1
ST	=	1
IORQ	=	1
BUSACK	=	1
RFSH	=	1
E	=	Note 3
IOCS	=	Z
MWR	=	1 ***(Note 4)***

Notes:

1. This assumes that BUSREQ is not activated during the halt.

2. This assumes that the refresh is not enabled. This would not be a logical case since the address bus is tri-stated during the Halt mode.

3. There is no control on the E line during the halt recovery so transitions on the pin are possible.

4. This is only true if MWR function is enabled.

The Halt recovery mode is implemented by applying wait states to the next CPU operation following the exit from halt. All signals listed above are forced to their specified state (unless otherwise noted) during halt and also during the recovery state. Sixteen cycles after the halt pin goes High the signals are released to their normal state, then eight wait states are inserted to allow proper access to accommodate slow memories.

After the first memory access, the wait states will be inserted as programmed in the wait state generators.

In addition, if bit 4 of the Z80182 Enhancement Register is set, the TxDA pin will be tri-stated during Halt and Recovery modes.

16550 MIMIC INTERFACE REGISTERS

MIMIC Master Control Register (MMC)

The 16550 MIMIC interface is controlled by the MMC register. Setting it allows for different modes of operation such as using the 8-bit counters, DMA accesses, and which IRQ structure is used with the PC/XT/AT.

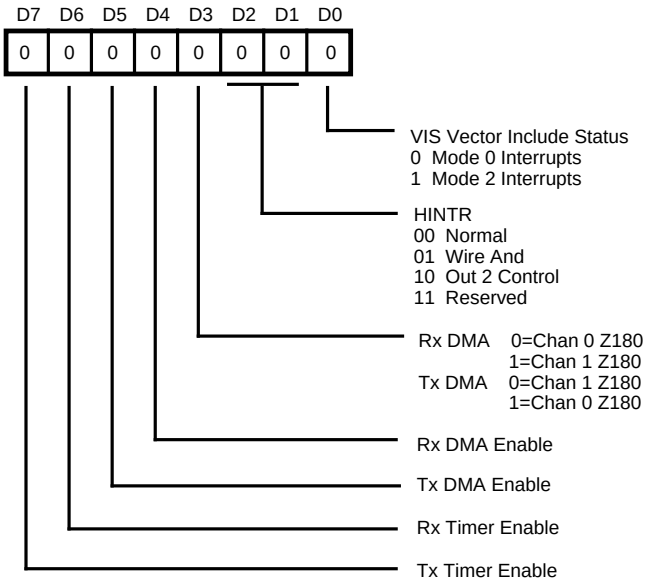


Figure 60. MIMIC Master Control Register
(Z180 MPU Read/Write, Address xxFFH)

Bit 7 Transmit Emulation Delay Counter Enable (Read/Write)
If bit 7 is set to 1, it enables the transmit delay timer. When the Z180 reads the Transmit Register, it loads the transmit delay timer from the Transmit Time Constant Register and enables the timer to count down to zero. This timer delays setting the Transmit Holding Register Empty (THRE) bit until the timer times out. If this bit is 0, then THRE is set immediately on a Z180 read of the Transmit Register. This bit also enables the emulation timer used in Transmitter Double Buffering.

Bit 6 Receive Emulation Delay Counter Enable (Read/Write)
If bit 6 is set to 1, it enables the receive delay timer. When the Z180 writes to the Receive Buffer, it loads the receive delay timer from the Receive Time Constant Register and enables the timer to count down to zero. This timer delays setting the Data Ready (DR) bit in the LSR until the timer times out. If this bit is 0 then DR is set immediately on a Z180 write to the Receive Buffer.

Both counters are single pass and stop on a count of Zero. Their purpose is to delay data transfer just as if the 16550 UART had to shift the data in and out. This is provided to alleviate any software problems a high speed continuous data transfer might cause to existing software. If this is not a concern, then data can be read and written as fast as the two machines can access the devices. In FIFO mode of operation , the timers are used to delay the status to the PC interface by the time required to actually shift the characters out, or in, if an actual UART were present.

Bit 5 Transmit DMA Enable (Read/Write)
If this bit is set to 1, it enables the Transmit DMA function.

Bit 4 Receive DMA Enable (Read/Write)
If this bit is set to 1, it enables the Receive DMA function.

Bit 3 Receive DMA Channel Select (Read/Write)
If bit 3 is set to 0, then Receive DMA transfer is done through Z180 DMA channel 0 and the Transmit DMA is done through DMA channel 1. If bit 3 is set to 1, then Receive DMA transfer is done through Z180 DMA channel 1 and the Transmit DMA is done through DMA channel 0.

Bits 2,1 Interrupt Select (Read/Write).
See Table 15.

Bit 0 Vector Include Status (Read/Write)
This bit is used to select the interrupt response mode of the Z180. A 0 in this bit enables Mode 0 interrupts; a 1 enables Mode 2 response.

Table 15. MIMIC Master Control Register Interrupt Select

Bit 2	Bit 1	HINTR Function
0	0	HINTR is set to normal 16550 MIMIC mode. A fully driven output is required when external priority arbiters are used.
0	1	A wired AND condition on the HINTR pin is possible to the PC/XT/AT. The interrupt is active High with only the pull-up of the HINTR pin driving; otherwise this pin is tri-state. Wired AND is needed when an external arbiter is not available.
1	0	HINTR is driven when out 2 of the Modem Control Register is 1. HINTR is tri-state when MCR out 2 is 0.
1	1	RESERVED

Interrupt Enable Register

The IE Register allows each of the 16550/8250 interrupts to the Z180™ MPU to be masked off individually or globally.

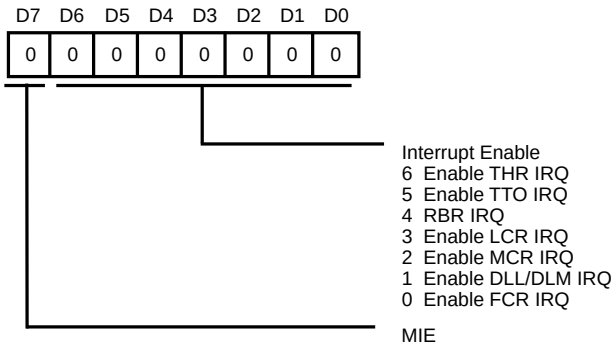


Figure 62. IE Register
(Z180 MPU, Address xxFDH)

Bit 7 Master Interrupt Enable (Read/Write)
If bit 7 is 0, all interrupts from the 16550 MIMIC are masked off. If this bit is 1, then interrupts are enabled individually by setting the appropriate bit.

Bit 6 Enable THR Interrupt (Read/Write)
If this bit is 1, it enables the Transmit Holding Register Interrupt.

Bit 5 Enable TTO Interrupt (Read/Write)
If this bit is 1, it enables the Transmitter Timeout Interrupt. This interrupts the CPU when characters remain in the FIFO below the trigger level and the FIFO is not read or written for the length of time in the transmitter timeout register.

Bit 4 Enable RBR Interrupt (Read/Write)
If this bit is 1, it enables the Receive Buffer Register Interrupt.

Bit 3 Enable LCR Interrupt (Read/Write)
If this bit is 1, it enables the Line Control Register interrupt.

Bit 2 Enable MCR Interrupt (Read/Write)
If this bit is 1, it enables the Modem Control Register Interrupt.

Bit 1 Enable DLL/DLM Interrupt (Read/Write)
If this bit is 1, it enables the Divisor Latch Least and Most Significant Byte interrupts.

Bit 0 Enable FCR Interrupt (Read/Write)
If this bit is 1 , then interrupts are enabled for a PC write to the FIFO control register (FCR) or for occurrence of Tx Overrun.

Priority of interrupts are in this order:

(Highest)	6	THR IRQ
	5	TTO IRQ
	4	RBR IRQ
	3	MCR IRQ
	2	LCR IRQ
	1	DLL IRQ
	1	DLM IRQ
(Lowest)	0	FCR or Tx OVERRUN IRQ

Interrupt Vector Register

The Interrupt Vector Register contains either the opcode (Z180 Interrupt Mode 0) or the modified vector used as the lower address for a Z180 interrupt service routine (Z180 Interrupt Mode 2), depending upon the VIS bit in the MMC Register (MIMIC Master Control Register). If the VIS bit is 0, then Z180 Mode 0 interrupt is selected; if VIS is 1, then Z180 Mode 2 is selected. Note that in Z180 Interrupt Mode 0, the data input to the MPU during the interrupt acknowledge cycle is an instruction opcode; in Z180 Interrupt Mode 2, this data (modified depending on the source of the interrupt) becomes part of an address from which to get the starting address of the interrupt service routine.

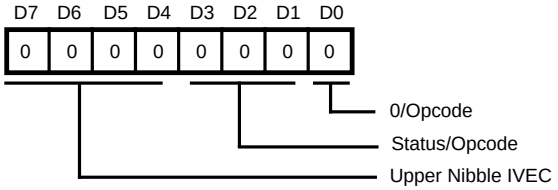


Figure 63. IVEC Register
(Z180 MPU, Address xxFCH)

Bits 7-4 Upper Nibble IVEC (Read/Write)
These four bits generate either an opcode for Z180 Interrupt Mode 0, or the upper four bits of the interrupt modified vector used as an 8-bit address to support the Z180 Interrupt Mode 2. These bits are read/write and always read back what was last written to them.

Bits 3-1 Interrupt Modified Vector/Opcode (Read/Write Table 16)
These three bits are the Interrupt Status bits when VIS in the MMC register is 1 (Z180 Interrupt Mode 2). If VIS bit is 0, then this field contains bit 3-bit 1 of the opcode. If the VIS bit is 0, then these bits contain what was last written to them.

DC CHARACTERISTICS

Z80182/Z8L182

(V_{CC} = 5V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL, NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL, NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL, NMI	–0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL, NMI	–0.3		0.8	V	
V_{OH1}	Output H Voltage	2.4			V	I_{OH} = –200 µA
	All outputs	V_{CC} –1.2				I_{OH} = –200 µA
V_{OH2}	Output H PHI	V_{CC} –0.6			V	I_{OH}= –200 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.2 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{TL}	Tri-state Leakage Current			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{CC}*	Power Dissipation*		60	120	mA	f = 20 MHz
	(Normal Operation)		100	200	mA	f = 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(SLEEP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(I/O STOP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		5	10	mA	f = 20 MHz
	(SYSTEM STOP mode)		9	17	mA	f = 33 MHz
	IDLE Mode		TBD	TBD	mA	f = 20 MHz
			TBD	TBD	mA	f = 33 MHz
	STANDBY Mode		50		µA	f = 0 MHz †
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:

These I_{CC} values are preliminary and subject to change without notice.

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
V_{CC} = 5.0V; (I_{OH} Low EMI) = -50 µA, I_{OL} (Low EMI) = 500 µA

† Device may take up to two seconds before stabilizing to steady state standby current.

TIMING DIAGRAMS (Continued)

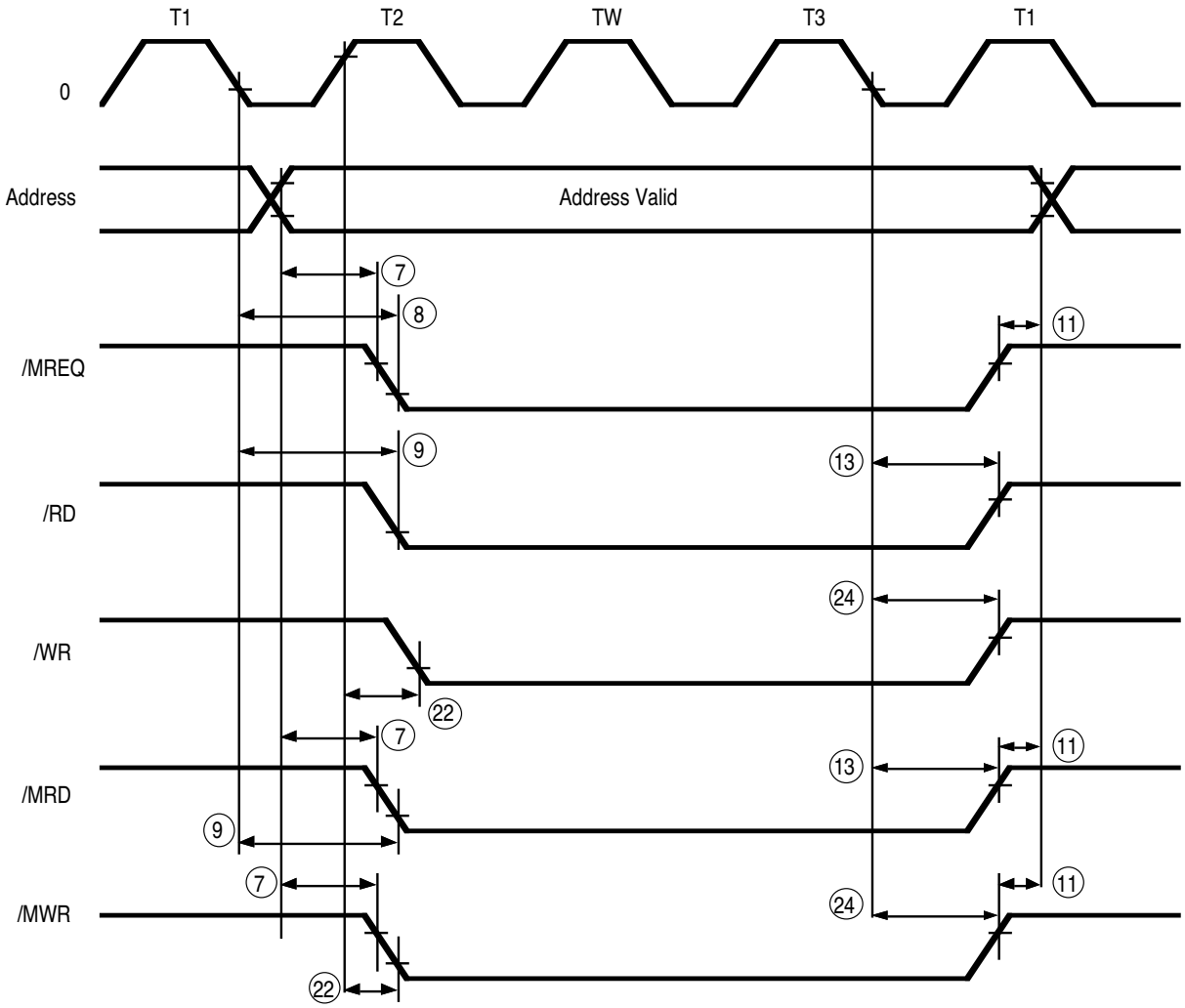


Figure 101. /MWR and /MRD Timing

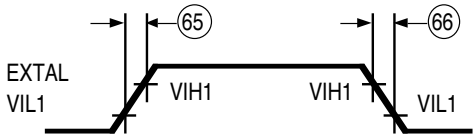


Figure 102. External Clock Rise Time and Fall Time

Figure 103. Input Rise and Fall Time
(Except EXTAL, /RESET)

Table C. Z85230 General Timing Table

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Notes
1	TdPC(REQ)	/PCLK to W/REQ Valid		70	
2	TdPC(W)	/PCLK to Wait Inactive		170	
3	TsRxC(PC)	/RxC to /PCLK Setup Time	N/A		[1,4]
4	TsRxD(RxCr)	RxD to /RxC Setup Time		0	[1]
5	ThRxD(RxCr)	RxD to /RxC Hold Time	45		[1]
6	TsRxD(RxCf)	RxD to /RxC Setup Time	0		[1,5]
7	ThRxD(RxCf)	RxD to /RxC Hold Time	45		[1,5]
8	TsSY(RxC)	/SYNC to /RxC Setup Time	–90		[1]
9	ThSY(RXC)	/SYNC to/RxC Hold Time	5TcPc		[1]
10	TsTxC(PC)	/TxC to /PCLK Setup Time	N/A		[2,4]
11	TdTxCf(TXD)	/TxC to TxD Delay		70	[2]
12	TdTxCr(TXD)	/TxC to TxD Delay		70	[2,5]
13	TdTxD(TRX)	TxD to TRxC Delay		70	
14	TwRTxh	RTxC High Width	70		[6]
15	TwRTxl	TRxC Low Width	70		[6]
16a	TcRTx	RTxC Cycle Time	200		[6,7]
16b	TxRx(DPLL)	DPLL Cycle Time Min	50		[7,8]
17	TcRTxx	Crystal Osc. Period	61	1000	[3]
18	TwTRxh	TRxC High Width	70		[6]
19	TwTRxl	TRxC Low Width	70		[6]
20	TcTRx	TRxC Cycle Time	200		[6,7]
21	TwExT	DCD or CTS Pulse Width	60		
22	TwSY	SYNC Pulse Width	60		

Notes:
These AC parameter values are preliminary and subject to change without notice.
[1] RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[2] TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[3] Both /RTxC and /SYNC have 30 pF capacitors to ground connected to them.
[4] Synchronization of RxC to PCLK is eliminated in divide by four operation.
[5] Parameter applies only to FM encoding/decoding.
[6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
[7] The maximum receive or transmit data rate is 1/4 PCLK.
[8] Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock should have a 50% duty cycle.

Table D. Z85230 System Timing Table

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Notes [4]
1	TdRxC(REQ)	/RxC to /W//REQ Valid	13	18	[2]
2	TdRxC(W)	/RxC to /Wait Inactive	13	18	[1,2]
3	TdRxC(SY)	/RxC to /SYNC Valid	9	13	[2]
4	TdRxC(INT)	/RxC to /INT Valid	15	22	[1,2]
5	TdTxC(REQ)	/TxC to /W//REQ Valid	8	12	[3]
6	TdTxC(W)	/TxC to /Wait Inactive	8	15	[1,3]
7	TdTxC(DRQ)	/TxC to /DTR//REQ Valid	7	11	[3]
8	TdTxC(INT)	/TxC to /INT Valid	9	14	[1,3]
9	TdSY(INT)	/SYNC to /INT Valid	2	6	[1]
10	TdExT(INT)	/DCD or /CTS to /INT Valid	3	9	[1]

Notes:
These AC parameters values are preliminary and subject to change without notice.
[1] Open-drain output, measured with open-drain test load.
[2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[4] Units equal to TcPc

Table E. I/O Port Timing

No.	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
1	TsPIA(RD)	Port Data Input Setup to /RD Fall	20		20	
2	ThPIA(RD)	Port Data Input Hold From /RD Rise	0		0	
3	$TdWR_F$(PIA)	Port Data Output Delay From /WR Fall		60		60
4	T_FWR_F(PIA)	Port Data Output Float From /WR Fall	0		0	

Table F. External Bus Master Timing

No.	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
1	TsA(IORQf)	Address to /IORQ Fall Setup	10		5	
2	TsIOf(WRf)	/IORQ Fall to /WR Fall Setup	0		0	
3	TsIOf(RDf)	/IORQ Fall to /RD Fall Setup	0		0	
4	ThIOR(WR_R)	/IORQ Rise From /WR Rise Hold	0		0	
5	ThIOR(RD_R)	/IORQ Rise From /RD Rise Hold	0		0	
6	TdRDf(DO)	/RD Fall to Data Out Valid Delay		50		45
7	T_HRD_R(DO)	/RD Rise to Data Out Valid Hold		0		0
8	$T_SD(WR_R)$	Data In to /WR Fall Setup	50		50	
9	THD(WR_R)	Data In From /WR Rise Hold	10	8	10	

16550 MIMIC TIMING

Refer to Figures 106 thru 112 for MIMIC AC Timing.

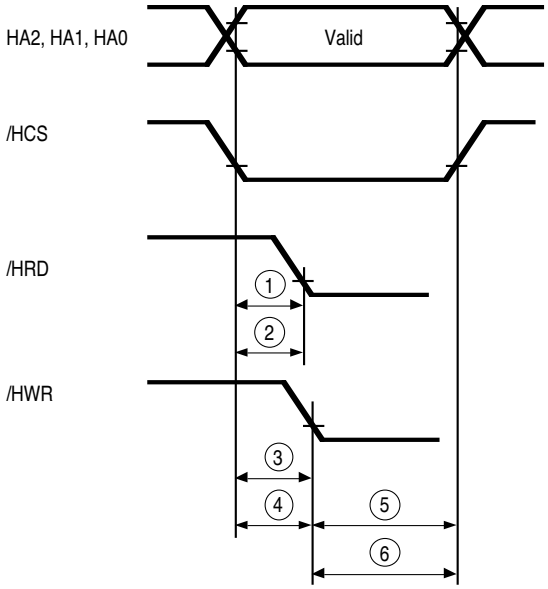


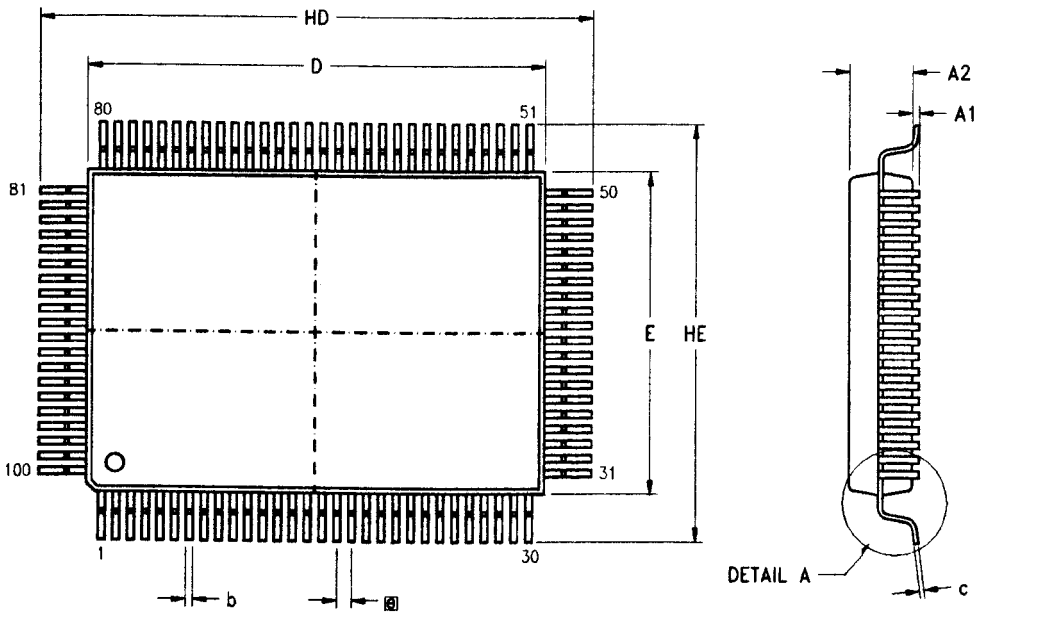
Figure 110. PC Host /RD /WR Timing

Table H. PC Host /RD /WR Timing

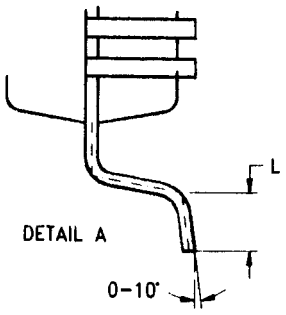
No	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
1	tAR	/HRD Delay from Address	30		30		ns
2	tCSR	/HRD Delay from /HCS	30		30		ns
3	tAW	/HWR Delay from Address	30		30		ns
4	tCSW	/HWR Delay from /HCS	30		30		ns
5	tAh	Address Hold Time	20		20		ns
6	tCSh	/HCS Hold Time	20		20		ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 TYP		.0256 TYP	
L	0.70	1.10	.028	.043



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

100-Pin QFP Package Diagram