Zilog - Z8018216FSC00TR Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018216fsc00tr

GENERAL DESCRIPTION (Continued)

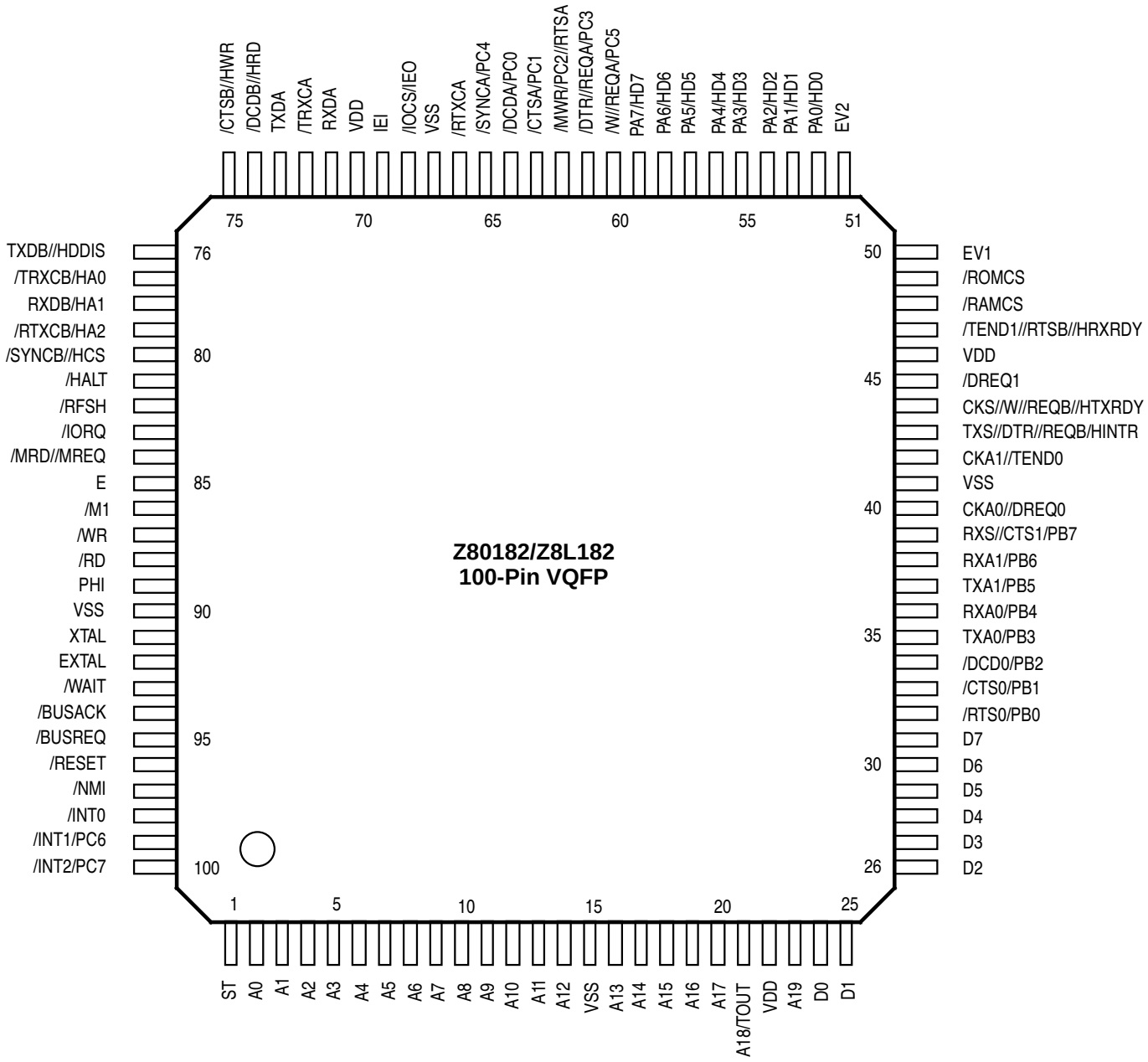


Figure 3. Z80182/Z8L182 100-Pin VQFP Pin Configuration

Z85230 ESCC SIGNALS (Continued)

/SYNCA, /SYNCB. *Synchronization (inputs/outputs, active Low).* These pins can act as either inputs, outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to /CTS and /DCD. In this mode, transitions on these lines affect the state of the Sync /Hunt status bits in Read Register 0, but have no other function. /SYNCA is also multiplexed with PC4 (parallel Port C, bit 4) on the /SYNCA/PC4 pin.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode /SYNC must be driven Low two receive clock cycles after the last bit in the sync character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.

In the Internal Synchronization mode, (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync character is recognized (regardless of the character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. In Z80182/Z8L182 mode 1 the /SYNCB signal is multiplexed with the 16550 MIMIC interface /HCS input on the /SYNCB //HCS pin.

/CTSA. *Clear To Send (input, active Low).* If this pin is programmed as auto enable, a Low on this input enables the channel A transmitter. If not programmed as auto enable, it may be used as a general-purpose input. The input is Schmitt-trigger buffered to accommodate slow rise-time input. The ESCC™ detects transitions on this input and can interrupt the Z180™ MPU on either logic level transitions. /CTSA is multiplexed with PC1 (parallel Port C, bit 1) on the /CTSA/PC1 pin.

/CTSB. *Clear To Send (input, active Low).* This pin is similar to /CTSA's functionality but is applicable to the channel B transmitter. In Z80182/Z8L182 mode, the /CTSB signal is multiplexed with the 16550 MIMIC interface /HWR input on the /CTSB //HWR pin.

/DCDA. *Data Carrier Detect (input, active Low).* This pin functions as receiver enables if it is programmed as an auto enable bit; otherwise, it may be used as a general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects transitions on this pin and can interrupt the Z180 MPU on either logic level transitions. /DCDA is also multiplexed with PC0 (parallel Port C, bit 0) on the /DCDA/PC0 pin.

/DCDB. *Data Carrier Detect (input, active Low).* This pin's functionality is similar to /DCDA but applicable to the channel B receiver. In Z80182/Z8L182 mode 1, /DCDB is multiplexed with the 16550 MIMIC interface /HRD input on the /DCDB//HRD pin.

/RTSA. *Request to Send (output, active Low).* When the Request to Send (RTS) bit in Write Register 5 channel A is set, the /RTSA signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with auto enables off, the /RTSA pin strictly follows the state of the RTS bit. The pin can be used as general-purpose output. /RTSA is multiplexed with PC2 (parallel Port C bit 2). This /RTSA or PC2 combination is pin multiplexed with /MWR (active when both the internal /MREQ and /WR are active) on the /MWR/PC2//RTSA pin. The default function of this pin on power-up is /MWR which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/RTSB. *Request to Send (output, active Low).* This pin is similar in functionality as /RTSA but is applicable on channel B. The /RTSB signal is multiplexed with the Z180 MPU /TEND1 signal and the 16550 MIMIC interface /HRxRDY signal on the /TEND1//RTSB//HRxRDY pin.

/DTR//REQA. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. /DTR//REQA is also multiplexed with PC3 (parallel Port C, bit 3) on the /DTR//REQA /PC3 pin.

/DTR//REQB. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. The /DTR//REQB signal is multiplexed with the Z180 MPU TxS signal and the 16550 MIMIC interface HINTR signal on the /TxS//DTR//REQB //HINTR pin.

/W//REQA. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This dual-purpose output can be programmed as Request (receive) lines for a DMA controller or as Wait lines to synchronize the Z180 MPU to the ESCC data rate. The reset state is Wait. The ESCC allows full duplex DMA transfers. /W//REQA is also multiplexed with PC5 (parallel Port C, bit 5) on the /W//REQA/PC5 pin.

/W//REQB. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

16550 MIMIC INTERFACE SIGNALS

HD7-HD0. *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

/HDDIS. *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

HA2-HA0. *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

/HCS. *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

/HWR. *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

/HRD. *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

HINTR. *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

/HTxRDY. *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

/HRxRDY. *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

PARALLEL PORTS

PA7-PA0. *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

PC7-PC0. *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

MULTIPLEXED PIN DESCRIPTIONS (Continued)

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
41	44	V_{SS}			
42	45	CKA1//TEND0			
43	46	TxS	/DTR//REQB	HINTR	SYS CONF REG Bit 1,2
44	47	CKS	/W//REQB	/HTxRDY	SYS CONF REG Bit 1,2
45	48	/DREQ1			
46	49	V_{DD}			
47	50	/TEND1	/RTSB	/HRxRDY	SYS CONF REG Bit 1,2
48	51	/RAMCS			
49	52	/ROMCS			
50	53	EV1			
51	54	EV2			
52	55	PA0	HD0		SYS CONF REG Bit 1
53	56	PA1	HD1		SYS CONF REG Bit 1
54	57	PA2	HD2		SYS CONF REG Bit 1
55	58	PA3	HD3		SYS CONF REG Bit 1
56	59	PA4	HD4		SYS CONF REG Bit 1
57	60	PA5	HD5		SYS CONF REG Bit 1
58	61	PA6	HD6		SYS CONF REG Bit 1
59	62	PA7	HD7		SYS CONF REG Bit 1
60	63	/W//REQA	PC5		SYS CONF REG Bit 7
61	64	/DTR//REQA	PC3		SYS CONF REG Bit 7
62	65	/MWR	PC2	RTSA	SYS CONF REG Bit 7 *
63	66	/CTSA	PC1		SYS CONF REG Bit 7
64	67	/DCDA	PC0		SYS CONF REG Bit 7
65	68	/SYNCA	PC4		SYS CONF REG Bit 7
66	69	/RTxCA			
67	70	V_{SS}			
68	71	/IOCS	IEO		INT EDG/PIN REG Bit 2
69	72	IEI			
70	73	V_{DD}			

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
71	74	RxDA			
72	75	/TRxCA			
73	76	TxDA			
74	77	/DCDB	/HRD		SYS CONF REG Bit 1
75	78	/CTSB	/HWR		SYS CONF REG Bit 1
76	79	TxDB	/HDDIS		SYS CONF REG Bit 1
77	80	/TRxCB	HA0		SYS CONF REG Bit 1
78	81	RxDB	HA1		SYS CONF REG Bit 1
79	82	/RTxCB	HA2		SYS CONF REG Bit 1
80	83	/SYNCB	/HCS		SYS CONF REG Bit 1
81	84	/HALT			
82	85	/RFSH			
83	86	/IORQ			
84	87	/MRD	/MREQ		INT EDG/PIN REG Bit 3
85	88	E			
86	89	/M1			
87	90	/WR			
88	91	/RD			
89	92	PHI			
90	93	V_{SS}			
91	94	XTAL			
92	95	EXTAL			
93	96	/WAIT			
94	97	/BUSACK			
95	98	/BUSREQ			
96	99	/RESET			
97	100	/NMI			
98	1	/INT0			
99	2	/INT1	PC6**		
100	3	/INT2	PC7**		

Notes:
* Also controlled by Interrupt Edge/Pin MUX Register
** PC7 and PC6 are inputs only and can read values of /INT1 and /INT2.

Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100% software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

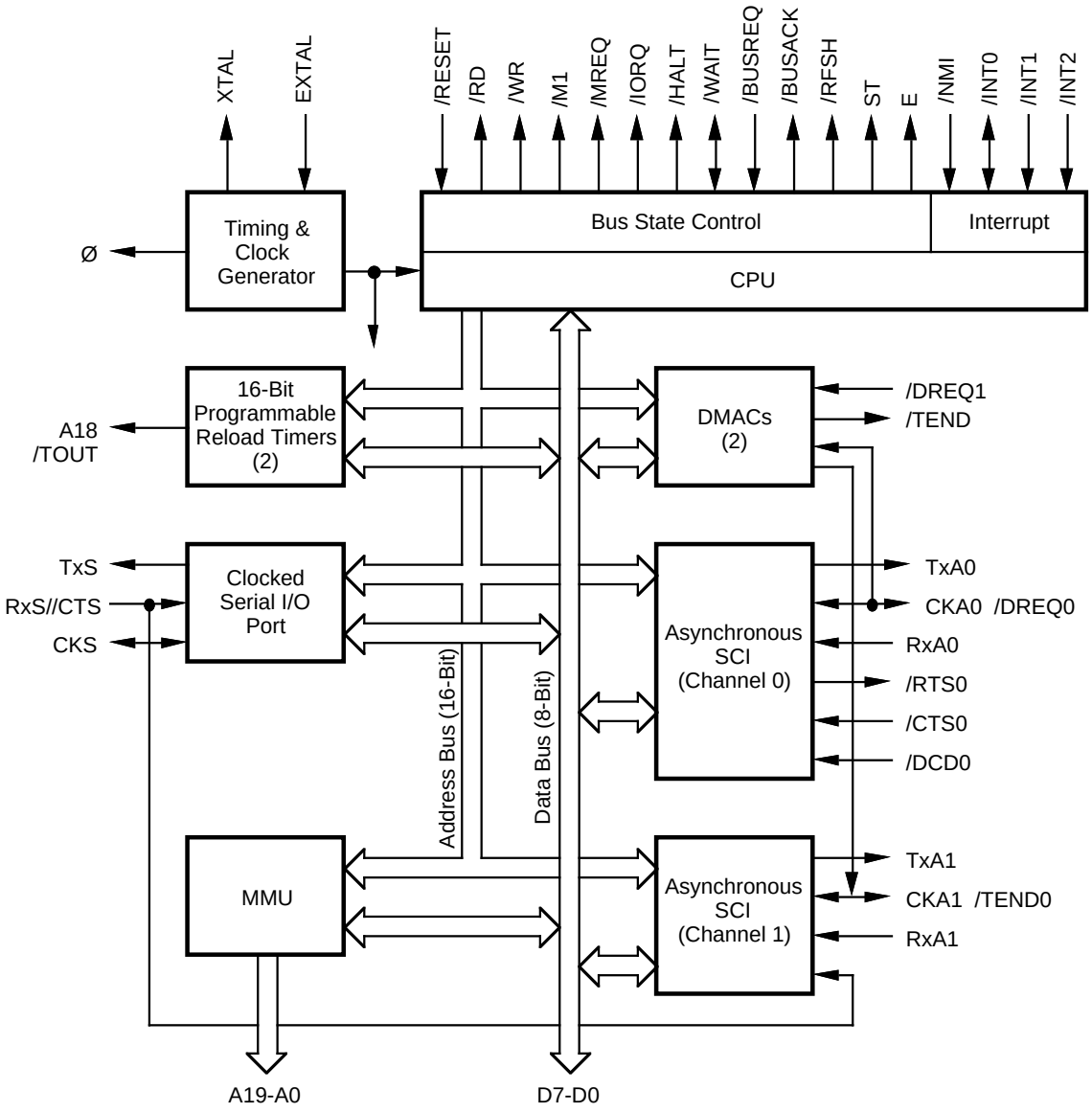


Figure 4. S180 MPU Block Diagram of Z182

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

16550 MIMIC INTERFACE FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has a 16550 MIMIC interface that allows it to mimic the 16550 device. It has all the interface pins necessary to connect to the PC/XT/AT bus. It contains the complete register set of the part with the same interrupt structure. The data path allows parallel transfer of data to and from the register set by the internal Z80180 of the Z80182/Z8L182. There is no shift register associated with the mimic of the 16550 UART. This interface saves the application from doing a serial transfer before performing data compression or error correction on the data.

Control of the register set is maintained by six priority encoded interrupts to the Z80182/Z8L182. When the PC/XT/AT writes to THR, MCR, LCR, DLL, DLM, FCR or reads the RBR, an interrupt to the Z80182/Z8L182 is generated. Each interrupt can be individually masked off or all interrupts can be disabled by writing a single bit. Both mode 0 and mode 2 interrupts are supported by the 16550 MIMIC interface.

Two eight-bit timers are also available to control the data transfer rate of the 16550 MIMIC interface. Their input is tied to the ESCC channel B divide clock, so a down count of 24 bits is possible. An additional two eight bit timers are available for programming the FIFO timeout feature (Four Character Time Emulation) for both Receive and Transmit FIFO's.

The 16550 MIMIC interface supports the PC/XT/AT interrupt structure as well as an additional mode that allows for a wired Logic AND interrupt structure.

The 16550 MIMIC interface is also capable of high speed parallel DMA transfers by using two control lines and the transmit and receive registers of the 16550 MIMIC interface.

All registers of the 16550 MIMIC interface are accessible in any page of I/O space since only the lowest eight address lines are decoded. See Figure 6 for a block diagram of the 16550 MIMIC interface.

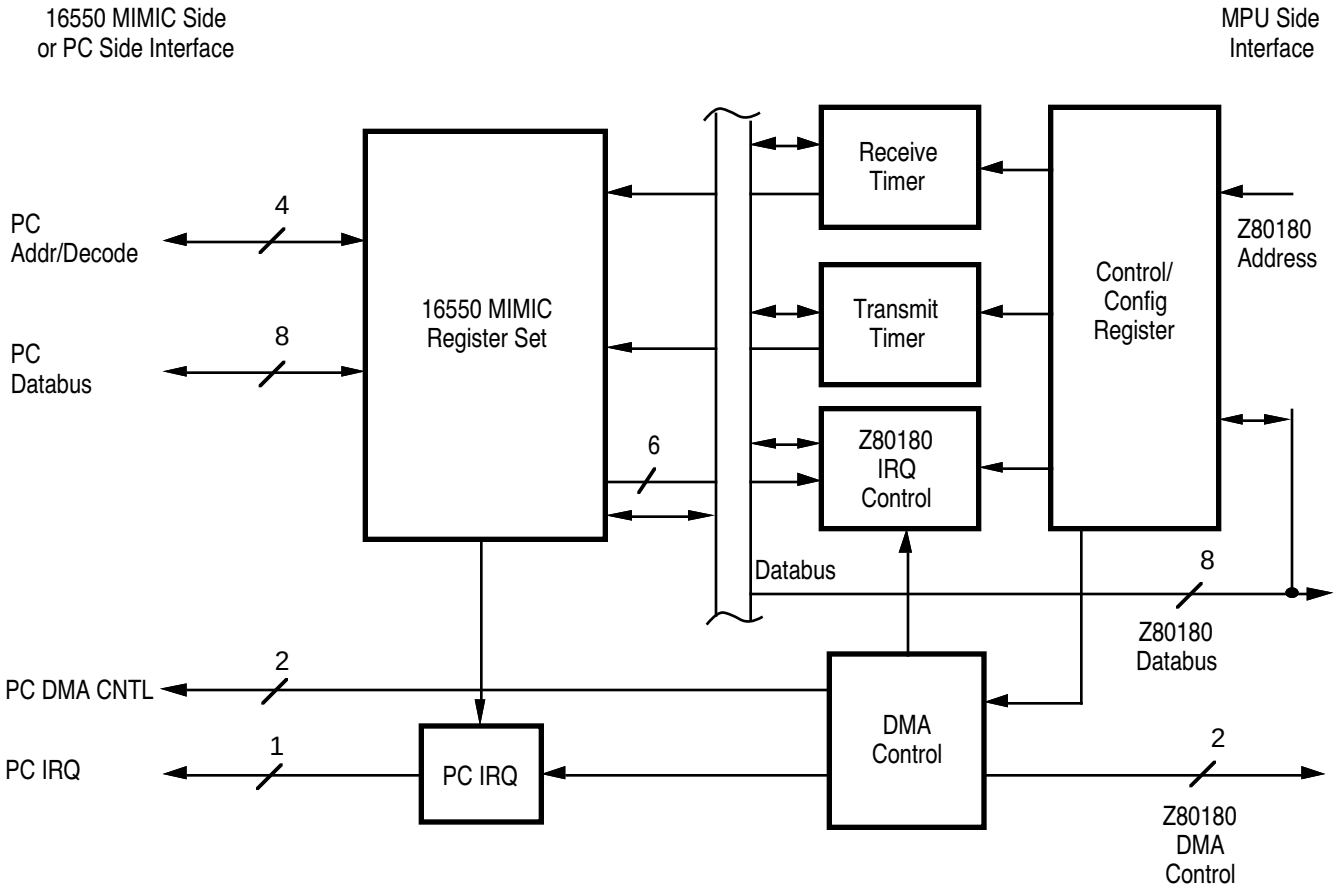


Figure 6. 16550 MIMIC Block Diagram

Z80182 MIMIC DOUBLE BUFFERING FOR THE TRANSMITTER

The Z80182 Rev DA implements double buffering for the transmitter in 16450 mode and sets the TEMT bit in the LSR Register automatically.

When this feature is enabled and character delay emulation is being used (see Figure 9):

1. The PC THRE bit in the LSR Register is set when the THR Register is empty;
2. PC Host writes to the 16450 THR Register;
3. Whenever the Z80182 TSR buffer is empty and one character delay timer is in a timed-out state, the byte from the THR Register is transferred to the TSR buffer; the timer is in timed-out state after FIFO Reset or after Host TEMT is set. This allows a dual write to THR when Host TEMT is set.
4. Restart character delay timer (timer reloads and counts down) with byte transfer from THR Register to the TSR buffer;
5. Whenever the TSR buffer is full, the TEMT bit in MPU LSR Register is reset with no delay;
6. MPU reads TSR buffer;
7. TEMT bit in LSR Register for MPU is set with no delay whenever the TSR buffer is empty;
8. When the TSR buffer is read by MPU and THR Register is empty and one character delay timer reaches zero, the TEMT bit in the LSR Register for Host is set from 0 to 1.

The PC THRE bit in the LSR Register is reset whenever the THR Register is full and set whenever THR Register is empty.

MPU IREQ and DMA Request for the transmit data is trigger whenever TSR buffer is full and cleared whenever TSR buffer is empty.

If character delay emulation is not used the TEMT bit in the LSR Register is set whenever both the THR Register and the TSR buffer are both empty. The Host TEMT bit is clear if there is data in either the TSR buffer of THR Register.

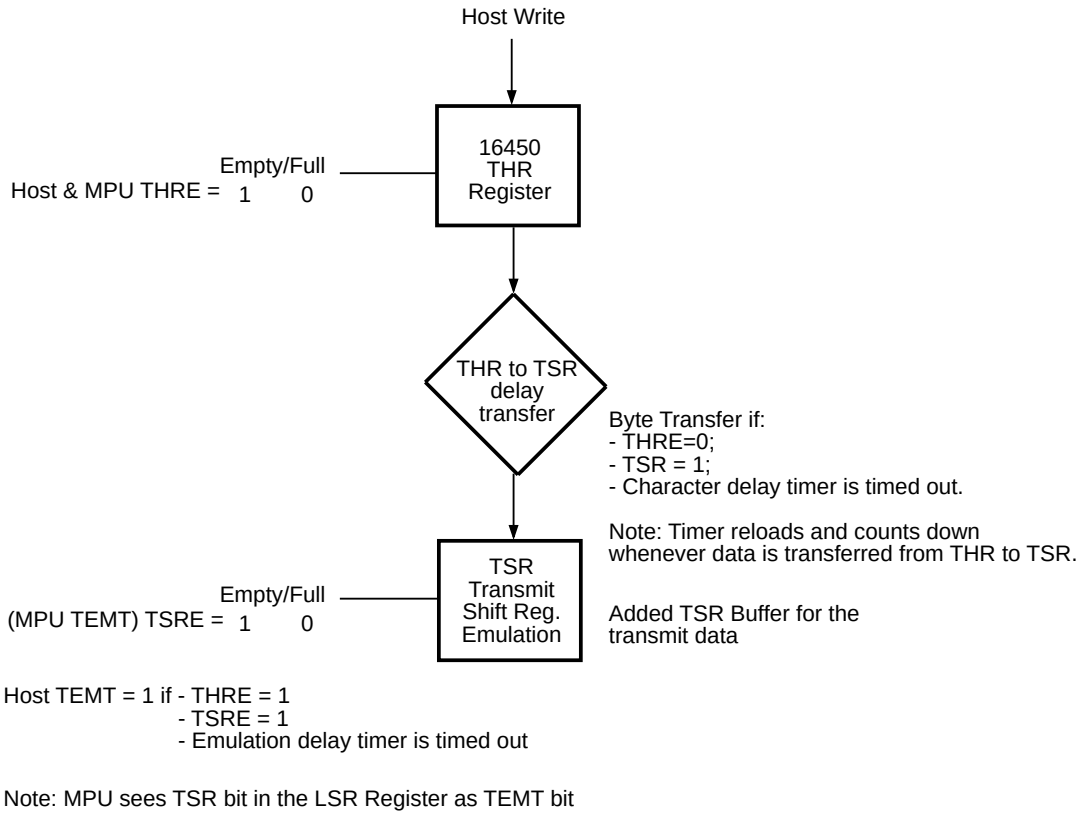


Figure 9. TEMT Emulation Logic Implementation

Z182 MPU CONTROL REGISTERS

Figures 10 through 50 refer to the Z80182/Z8L182 MPU Control registers. For additional information, refer to the Z8S180 Product Specification and Technical Manual.

ASCI CHANNELS CONTROL REGISTERS

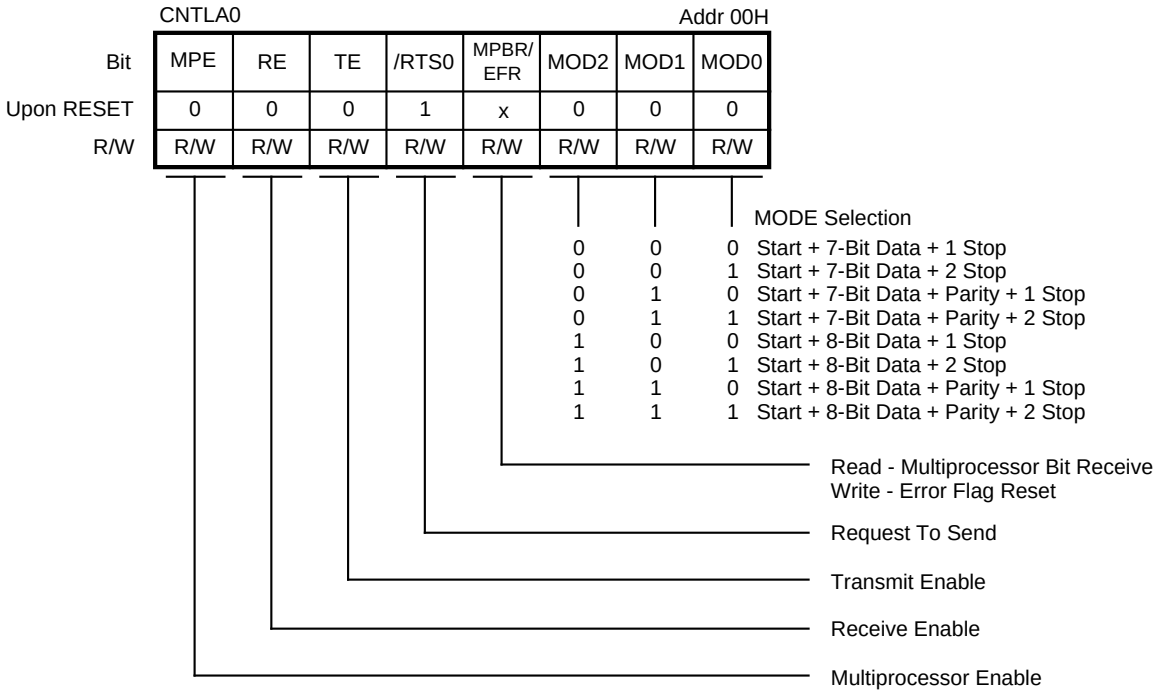


Figure 10a. ASCI Control Register A (Ch. 0)

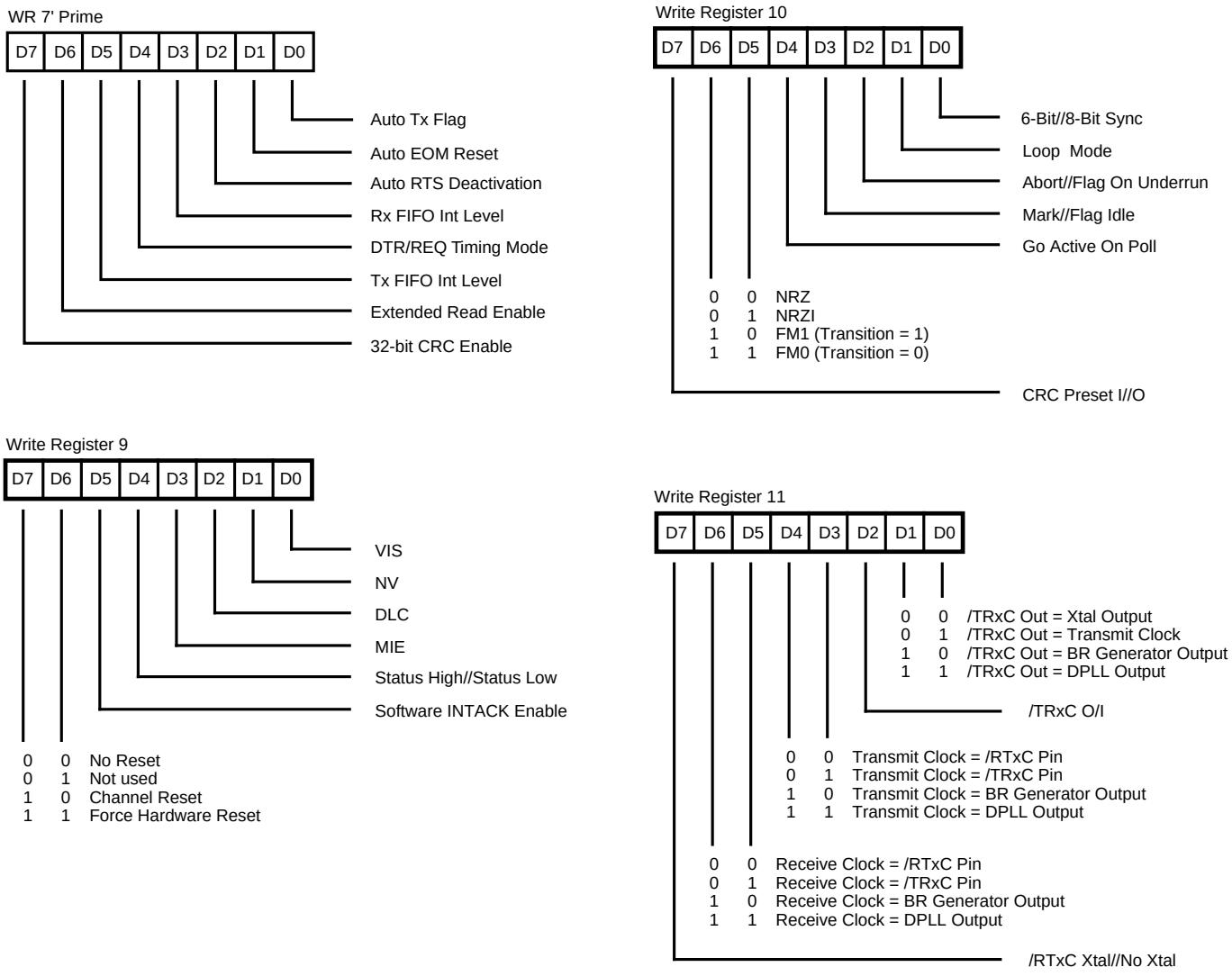


Figure 52. Write Register Bit Functions (Continued)

CONTROL REGISTERS (Continued)

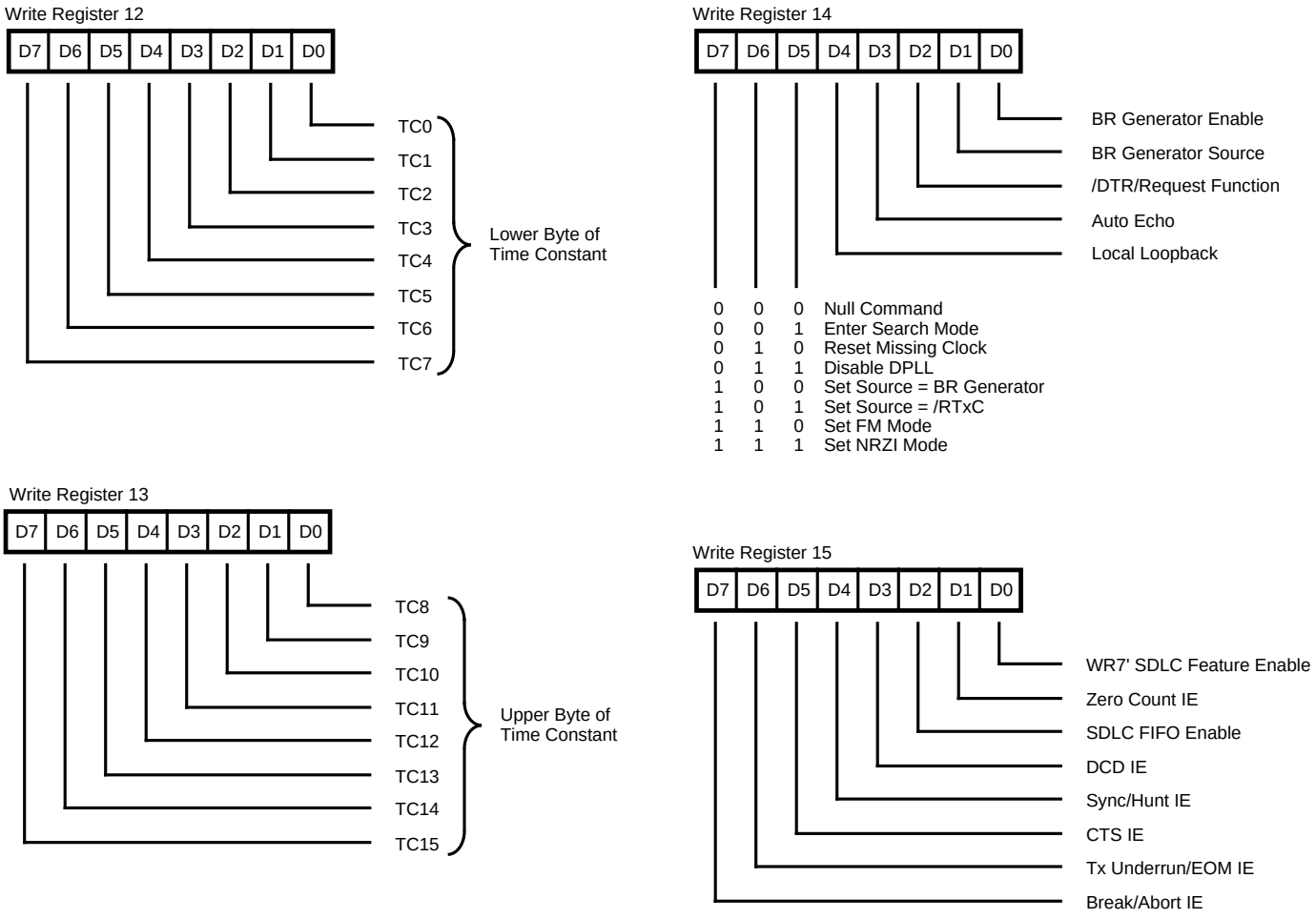
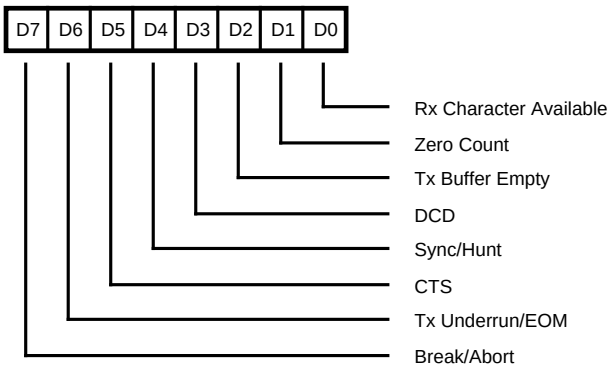
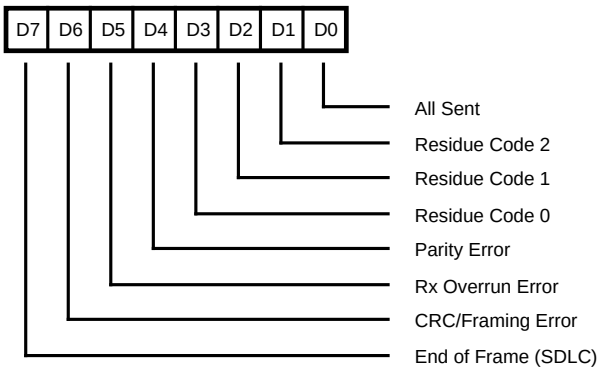


Figure 52. Write Register Bit Functions (Continued)

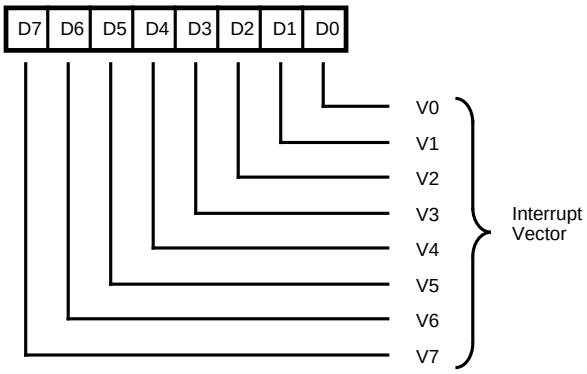
Read Register 0



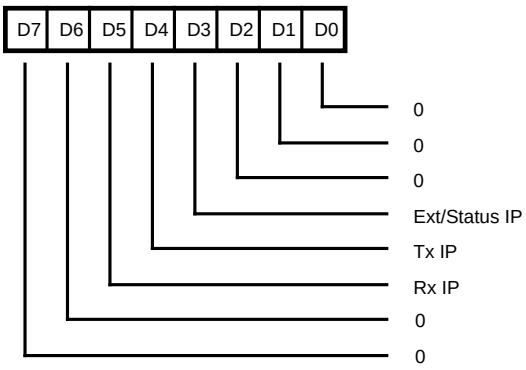
Read Register 1



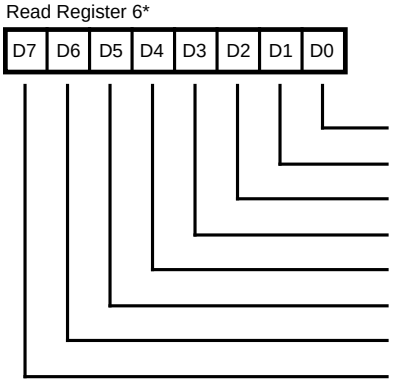
Read Register 2



Read Register 3



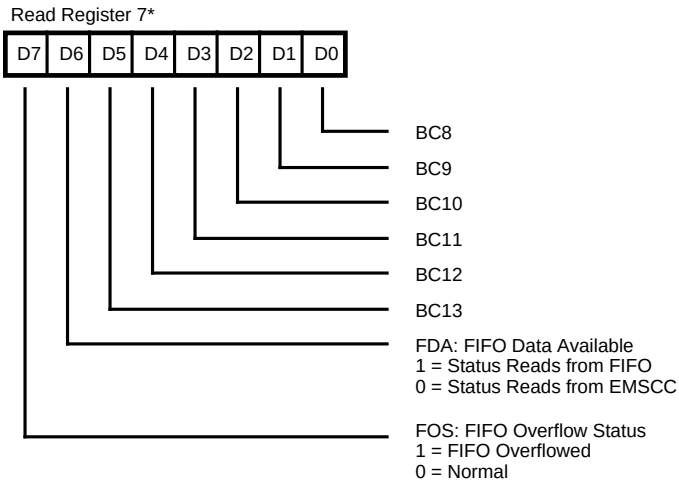
Read Register 6*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Read Register 7*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Figure 52. Write Register Bit Functions (Continued)

INTERRUPT EDGE/PIN MUX REGISTER

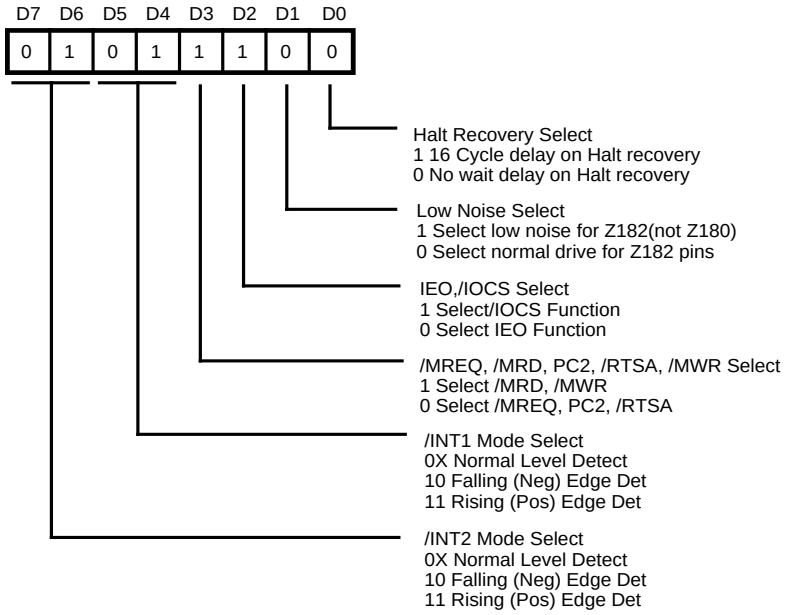


Figure 59. Interrupt Edge/Pin MUX Register
(Z180 MPU Read/Write, Address xxDFH)

Bits 7-6. These bits control the interrupt capture logic for the external /INT2 PIN. When programmed as '0X', the /INT2 pin performs as the normal level detecting interrupt pin. When programmed as 10 the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT2 of the Z180. This interrupt must be cleared by writing a 1 to bit 7 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge.

Bits 5-4. These bits control the interrupt capture logic for the external /INT1 PIN. When programmed as '0X', the /INT1 pin performs as the normal level detecting interrupt pin. When programmed as 10, the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT1 of the Z180. This interrupt must be cleared by writing a 1 to bit 6 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge. Edge detect logic cannot be used in Emulation Adaptor EV mode 1.

Bit 3. Programming this bit to 1 selects the /MRD and the /MWR functions. The default for power up and /RESET conditions is 1, i.e., the /MRD and /MWR. By programming this bit to 0 the /MREQ Z180 function is enabled, as well as the PC2//RTSA function on the PC2//RTSA//MWR pin. If the /MREQ Z180 function is enabled, any external bus master must be prevented from asserting Z182's IRD signal unless accessing Z182's IO.

Bit 2. This bit selects the /IOCS function which is the default for power up and /RESET conditions. By programming this bit to 0 the IEO function is enabled for this multiplexed pin.

Bit 1. This bit selects the low noise or normal drive feature for the Z182 pins . The default at power up is normal drive for Z182 pins. By programming this bit to 1, low noise for the Z182 pins is chosen and the output drive capability of the following pins is reduced to 25% of the original drive capability:

- CKS
- CKA1/TEND0
- CKA0/DREQ0
- RxS/CTS1
- TxA1
- TxA0
- TxS

Programming this bit to 0 selects normal drive for the Z182 pins. Refer to the Z8S180 Product Specification for Low noise control of Z180 pins.

IUS/IP Register

The IUS/IP Register is used by the Z180™ MPU to determine the source of the interrupt. This register will have the appropriate bit set when an interrupt occurs.

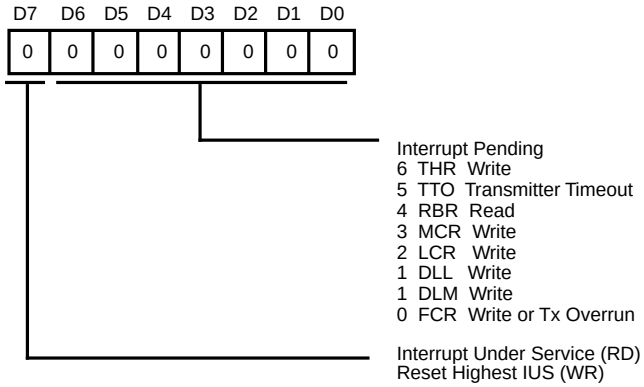


Figure 61. IUS/IP Register
(Z180 MPU, Address xxFEH)

Bit 7 Interrupt Under Service (Read/Write)
This bit represents a logical OR of each individual IUS bit for the internal MIMIC interrupt daisy chain. An IUS bit is set when an interrupt is registered (IP set) and enabled (IE set), the incoming IEI daisy chain is active (chain enabled) and an interrupt acknowledge cycle is entered. By writing a 1 to this bit the highest priority IUS bit that is set will be reset. Writing a 0 to this bit has no effect.

This should be done at the end of every MIMIC Interrupt Service routine.

Bit 6 Transmit Holding Register Written (Read Only)
This bit is set when the PC/XT/AT writes to the Transmit Holding Register. It is reset when the Z180 MPU reads the Transmit Holding Register. In FIFO mode, this bit is set when the trigger level is reached (4,8,14 bytes available). **Note:** The THR bit is set (interrupts) when the transmitter FIFO reaches the data available trigger level set in the MPU FCR control register. The bit and interrupt source is cleared when the number of data bytes falls below the set trigger level.

Bit 5 Transmitter Timeout with Data in FIFO (Read Only)
This bit is set when the transmitter FIFO has been idle (no read or write and timer decrements to zero) with data bytes below the trigger level. It is cleared when the FIFO is read or written.

Bit 4 Receive Buffer Read (Read Only)
This bit is set when the PC/XT/AT reads the Receive Buffer Register. It is reset when the Z180 MPU writes to the Receive Buffer Register. In FIFO mode, this bit is set upon the PC reading all the data in the receive FIFO. **Note:** RBR is set and interrupts when the receive FIFO has been emptied by the PC. This bit and interrupt are cleared when one or more bytes are written into the receive FIFO by the MPU.

Bit 3 Modem Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the Modem Control Register. It is reset when the Z180™ MPU reads the Modem Control Register.

Bit 2 Line Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the Line Control Register. It is reset when the Z180 MPU reads the Line Control Register.

Bit 1 Divisor Latch LS/MS Write (Read Only)
This bit is set when the PC/XT/AT writes to the Divisor Latch Least Significant or Most Significant bytes. It is reset when the PC reads the LS/MS register(s). To determine which byte(s) have been written, the Z180 must read either LS or MS locations and then repoll this bit. If only one location is interrupting, the interrupt is cleared when that location is read by the Z180.

Bit 0 FIFO Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the FCR. This bit is also set when Transmit occurs. It is reset when the Z180 MPU reads this register.

The data direction register determines which are inputs and outputs in the PC Data Register. When a bit is set to 1 the corresponding bit in the PC Data Register is an input. If the bit is 0, then the corresponding bit is an output.

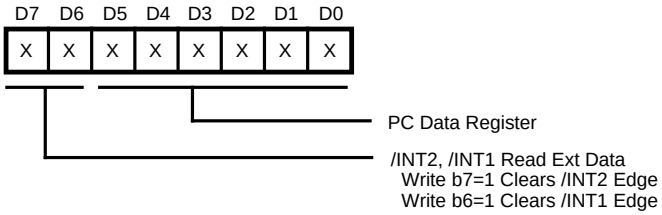


Figure 88. PC, Port C, Data Register
(Z180 MPU Read/Write, Address xxDEH)

When the Z180 MPU writes to the PC Data Register, the data is stored in the internal buffer. The values of Port C data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PC Data Register, the data on the external pins is returned.

Bits 6 and 7 serve the special function of reading the value of the external /INT2 and /INT1 lines. When operating either /INT2 or /INT1 in edge detection mode, the edge detect latch is reset by writing a 1 to bit 6 or 7 respectively. Writing a 0 has no effect. ***These latches should be reset at the end of an /INT1 or /INT2 interrupt service routine when using edge-triggered interrupt modes.***

16550 MIMIC INTERFACE DMA

The 16550 MIMIC is also able to do direct DMA with the PC/XT/AT. DMA is enabled by setting bits 3, 4 and 5 of the Master Control Register. DMA is accomplished by using the two DMA pins and the Transmitter Holding and Receive Data Registers.

If bit 5 is 1, the /HTxRDY pin is equal to the complement of the Transmit Holding Register Empty bit. If bit 5 is 1 and bit 3 is 0 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement of the Transmit Holding Register Empty Shadow bit. If bit 5 is 1 and bit 3 is 1 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Transmit Holding Register Empty Shadow bit.

If bit 4 is 1, then the /HRxRDY pin is equal to the complement of the Data Ready bit. If bit 4 is 1 and bit 3 is 0 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Data Ready Shadow bit. If bit 4 is 1 and bit 3 is 1 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement or the Data Ready Shadow bit.

DC CHARACTERISTICS

Z80182/Z8L182

(V_{CC} = 5V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL, NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL, NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL, NMI	–0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL, NMI	–0.3		0.8	V	
V_{OH1}	Output H Voltage	2.4			V	I_{OH} = –200 µA
	All outputs	V_{CC} –1.2				I_{OH} = –200 µA
V_{OH2}	Output H PHI	V_{CC} –0.6			V	I_{OH}= –200 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.2 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{TL}	Tri-state Leakage Current			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{CC}*	Power Dissipation*		60	120	mA	f = 20 MHz
	(Normal Operation)		100	200	mA	f = 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(SLEEP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(I/O STOP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		5	10	mA	f = 20 MHz
	(SYSTEM STOP mode)		9	17	mA	f = 33 MHz
	IDLE Mode		TBD	TBD	mA	f = 20 MHz
			TBD	TBD	mA	f = 33 MHz
	STANDBY Mode		50		µA	f = 0 MHz †
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

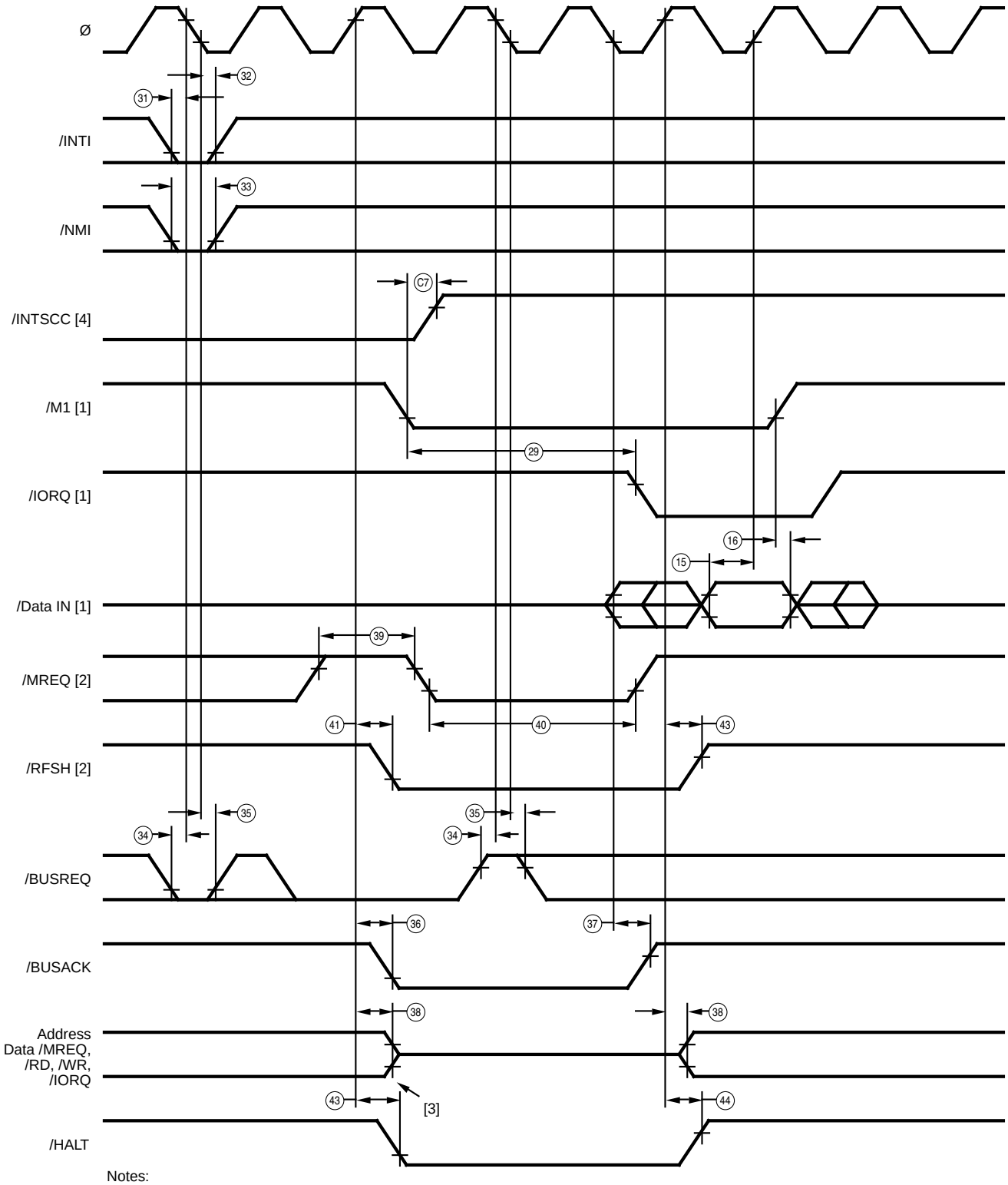
Notes:

These I_{CC} values are preliminary and subject to change without notice.

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
V_{CC} = 5.0V; (I_{OH} Low EMI) = -50 µA, I_{OL} (Low EMI) = 500 µA

† Device may take up to two seconds before stabilizing to steady state standby current.

TIMING DIAGRAMS (Continued)



Notes:
[1] During /INT0 acknowledge cycle
[2] During refresh cycle
[3] Output buffer is off at this point
[4] Refer to Table C, parameter 7

Figure 91. CPU Timing
(/INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode
HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

16550 MIMIC TIMING (Continued)

Table K. Interrupt Timing RCVR FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
14	tSINT	Delay from Stop to Set Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles
15	tRINT	Delay from /HRD (RD RBR or RD LSR) to Reset Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles

Note:
These AC parameter values are preliminary and are subject to change without notice.

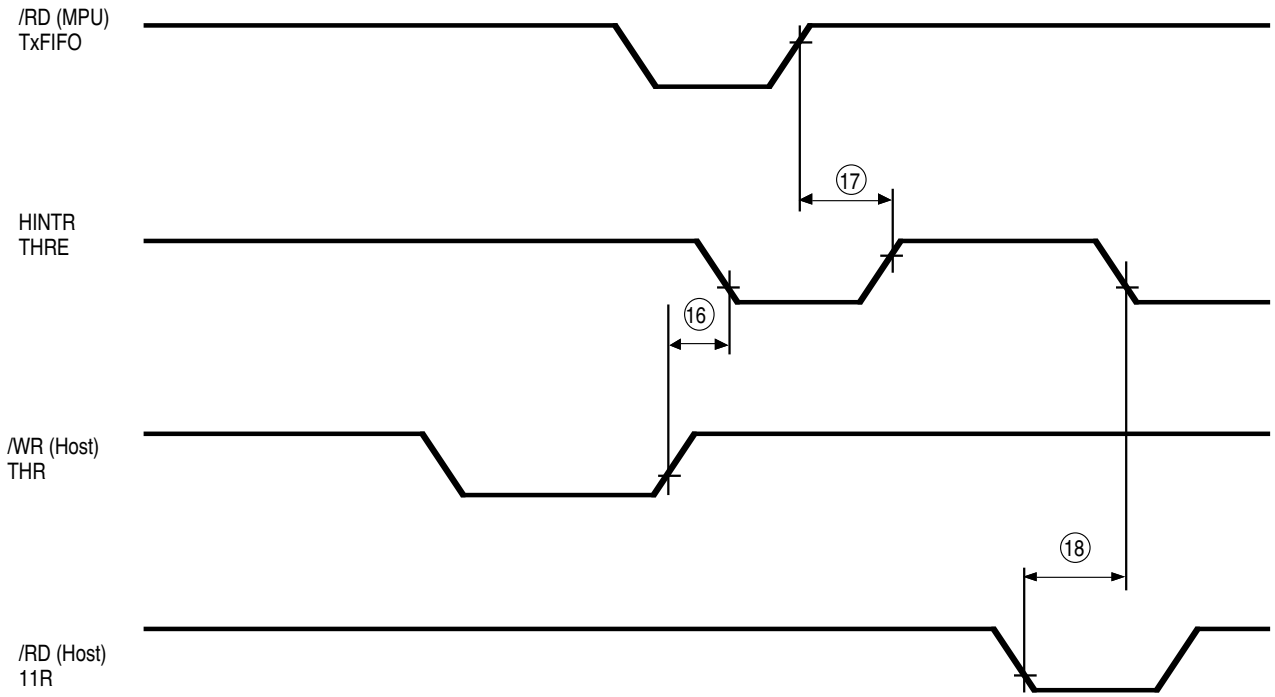


Figure 115. Interrupt Timing Transmitter FIFO

16550 MIMIC TIMING (Continued)

Table M. RCVR FIFO Bytes Other Than First

No	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
19	tRXi	Delay from /HRD RBR to /HRxRDY Inactive		290		290	ns
20	TWxi	Delay from Write to /HTxRDY Inactive		125		125	
21	tSXa	Delay From Start to /HTxRDY Active		3 MPU Clock Cycles		3 MPU Clock Cycles	

Note:
These AC parameter values are preliminary and are subject to change without notice.

Clock Generator

The Z80182/Z8L182 ZIP™ uses the Z182 MPUs on-chip clock generator to supply system clock. The required clock is easily generated by connection a crystal to the external terminals (XTAL,EXTAL). The clock output runs at half the crystal frequency for X2 mode.

Recommended characteristics of the crystal and the values for the capacitor are as follows (the values will change with crystal frequency).

Type of crystal:
Fundamental, parallel type crystal (AT cut is recommended).

Frequency tolerance:
Application dependent.

CL, Load capacitance:
Approximately 22 pF (acceptable range is 20-30 pF).

RS, equivalent-series resistance:
≤ 60 Ohms
C_{IN}=C_{OUT}=15~22 pF.

For PHI > 15 MHz (X2 Mode), it is recommended that an oscillator be used as input to EXTAL.

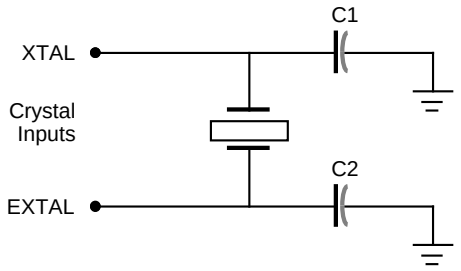


Figure 117. Circuit Configuration For Crystal