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Understanding Embedded - Microprocessors

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018216fsc1838

Z180 CPU SIGNALS

A19-A0. *Address Bus (input/output, active High, tri-state).* A19-A0 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges up to 1 Mbyte, and I/O data bus exchanges up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states. This bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset).

D7-D0. *Data Bus (bi-directional, active High, tri-state).* D7-D0 constitute an 8-bit bi-directional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

/RD. *Read (input/output, active Low, tri-state).* /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

/WR. *Write (input/output, active Low, tri-state).* /WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

/IORQ. *I/O Request (input/output, active Low, tri-state).* /IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. /IORQ is also generated, along with /M1, during the acknowledgment of the /INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

/M1. *Machine Cycle 1 (input/output, active Low).* Together with /MREQ, /M1 indicates that the current cycle is the opcode fetch cycle of an instruction execution; unless /M1E bit in the OMCR is cleared to 0. Together with /IORQ, /M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the /HALT and ST signals to decode status of the CPU machine cycle. This signal is analogous to the /LIR signal of the Z64180.

/MREQ. *Memory Request (input/output, active Low, tri-state).* /MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the /ME signal of the Z64180. /MREQ is multiplexed with /MRD on the /MRD//MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if the /MREQ function is selected; and is inactive High if /MRD function is selected.

/MRD. *Memory Read (input/output, active Low, tri-state).* /MRD is active when both the internal /MREQ and /RD are active. /MRD is multiplexed with /MREQ on the /MRD //MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if /MREQ function is selected; and is inactive High if /MRD function is selected. The default function on power up is /MRD and may be changed by programming bit 3 of the Interrupt Edge/Pin MUX Register (xxDFH).

/MWR. *Memory Write (input/output, active Low, tri-state).* /MWR is active when both the internal /MREQ and /WR are active. This /RTSA or PC2 combination is pin multiplexed with /MWR on the /MWR/PC2//RTSA pin. The default function of this pin on power up is /MWR, which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/WAIT. *(input/output active Low).* /WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The /WAIT input is sampled on the falling edge of T2 (and subsequent wait states). If the input is sampled Low, then additional wait states are inserted until the /WAIT input is sampled High, at which time execution will continue.

/HALT. *Halt/Sleep Status (input/output, active Low).* This output is asserted after the CPU has executed either the HALT or SLEEP instruction, and is waiting for either non-maskable or maskable interrupts before operation can resume. It is also used with the /M1 and ST signals to decode status of the CPU machine cycle. On exit of HALT/SLEEP mode, the first instruction fetch can be delayed by 16 clock cycles after the /HALT pin goes High, if HALT 16 feature is selected.

/BUSACK. *Bus Acknowledge (input/output, active Low).* /BUSACK indicates to the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

/BUSREQ. *Bus Request (input, active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address/data buses and other control signals, into the high impedance state.

/W//REQB. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

16550 MIMIC INTERFACE SIGNALS

HD7-HD0. *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

/HDDIS. *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

HA2-HA0. *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

/HCS. *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

/HWR. *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

/HRD. *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

HINTR. *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

/HTxRDY. *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

/HRxRDY. *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

PARALLEL PORTS

PA7-PA0. *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

PC7-PC0. *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 4.

Table 4. Multiplexed Port Pins

Port Mode Function	ASCI/ESCC Mode Function
PB7	RxS,/CTS1
PB6 Select with bit 6=1	RxA1
PB5 System Config Reg.	TxA1
PB4	RxA0
PB3	TxA0
PB2 Select with bit 5=1	/DCD0
PB1 System Config Reg.	/CTS0 (Note 1)
PB0	/RTS0
PC7	Always Reads /INT2 Ext. Status
PC6	Always Reads /INT1 Ext. Status
PC5	/W//REQA
PC4	/SYNCA
PC3 Select with bit 7=1	/DTR//REQA
PC2 System Config Reg.	/RTSA (Note 2)
PC1	/CTSA
PC0	/DCDA

Note 1:
When the Port function (PB1) is selected, the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

Note 2:
Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functions.

16550 MIMIC INTERFACE FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has a 16550 MIMIC interface that allows it to mimic the 16550 device. It has all the interface pins necessary to connect to the PC/XT/AT bus. It contains the complete register set of the part with the same interrupt structure. The data path allows parallel transfer of data to and from the register set by the internal Z80180 of the Z80182/Z8L182. There is no shift register associated with the mimic of the 16550 UART. This interface saves the application from doing a serial transfer before performing data compression or error correction on the data.

Control of the register set is maintained by six priority encoded interrupts to the Z80182/Z8L182. When the PC/XT/AT writes to THR, MCR, LCR, DLL, DLM, FCR or reads the RBR, an interrupt to the Z80182/Z8L182 is generated. Each interrupt can be individually masked off or all interrupts can be disabled by writing a single bit. Both mode 0 and mode 2 interrupts are supported by the 16550 MIMIC interface.

Two eight-bit timers are also available to control the data transfer rate of the 16550 MIMIC interface. Their input is tied to the ESCC channel B divide clock, so a down count of 24 bits is possible. An additional two eight bit timers are available for programming the FIFO timeout feature (Four Character Time Emulation) for both Receive and Transmit FIFO's.

The 16550 MIMIC interface supports the PC/XT/AT interrupt structure as well as an additional mode that allows for a wired Logic AND interrupt structure.

The 16550 MIMIC interface is also capable of high speed parallel DMA transfers by using two control lines and the transmit and receive registers of the 16550 MIMIC interface.

All registers of the 16550 MIMIC interface are accessible in any page of I/O space since only the lowest eight address lines are decoded. See Figure 6 for a block diagram of the 16550 MIMIC interface.

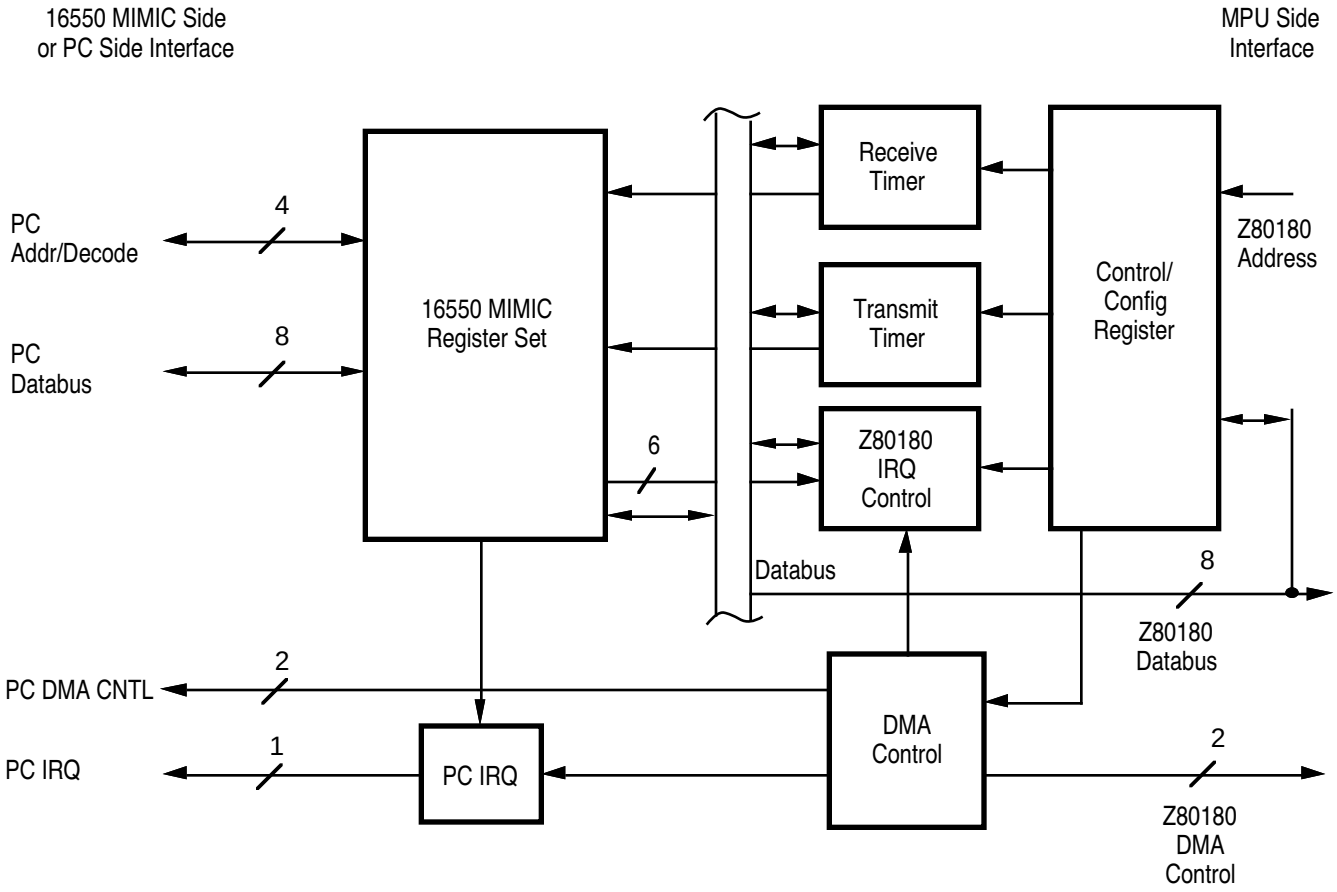


Figure 6. 16550 MIMIC Block Diagram

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only). The Ports are controlled through two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

PROGRAMMING

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for Z182 peripheral access. The full sixteen address lines are decoded for on-chip Z180 MPU access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers through the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated through the System Configuration Register and the Interrupt Edge/Pin MUX Register.

Table 7. Z80182/Z8L182 MPU Registers

Register Name	MPU Addr	PC Addr
Z80182/Z8L182 MPU Control Registers	0000H to 00x3FH (Relocatable to 0040H to 007FH or 0080H to 00BFH)	None

Note:
"x" indicates don't care condition

Table 8. Z80182/Z8L182 MIMIC Register MAP

Register Name	MPU Addr/Access		PC Addr/Access	
MMC MIMIC Master Control Register	xxFFH	R/W	None	
IUS/IP Interrupt Pending	xxFEH	R/Wb7	None	
IE Interrupt Enable	xxFDH	R/W	None	
IVEC Interrupt Vector	xxFCH	R/W	None	
TTCR Transmit Time Constant	xxFAH	R/W	None	
RTCR Receive Time Constant	xxFBH	R/W	None	
FSCR FIFO Status and Control	xxECH	R/W7-4	None	
RTTC Receive Timeout Time Constant	xxEAH	R/W	None	
TTTC Transmit Timeout Time Constant	xxEBH	R/W	None	
RBR Receive Buffer Register	xxF0H	W only	00H	DLAB=0 R only
THR Transmit Holding Register	xxF0H	R only	00H	DLAB=0 W only
IER Interrupt Enable Register	xxF1H	R only	01H	DLAB=0 R/W
IIR Interrupt Identification	None		02H	R only
FCR FIFO Control Register	xxE9H	R only	02H	W only
MM REGISTER	XXE9H	W only	None	
LCR Line Control Register	xxF3H	R only	03H	R/W
MCR Modem Control Register	xxF4H	R only	04H	R/W
LSR Line Status Register	xxF5H	R/Wb6432	05H	R only
MSR Modem Status Register	xxF6H	R/Wb7-4	06H	R only
SCR Scratch Register	xxF7H	R only	07H	R/W
DLL Divisor Latch (LSByte)	xxF8H	R only	00H	DLAB=1 R/W
DLM Divisor Latch (MSByte)	xxF9H	R only	01H	DLAB=1 R/W

Z182 MPU CONTROL REGISTERS

Figures 10 through 50 refer to the Z80182/Z8L182 MPU Control registers. For additional information, refer to the Z8S180 Product Specification and Technical Manual.

ASCI CHANNELS CONTROL REGISTERS

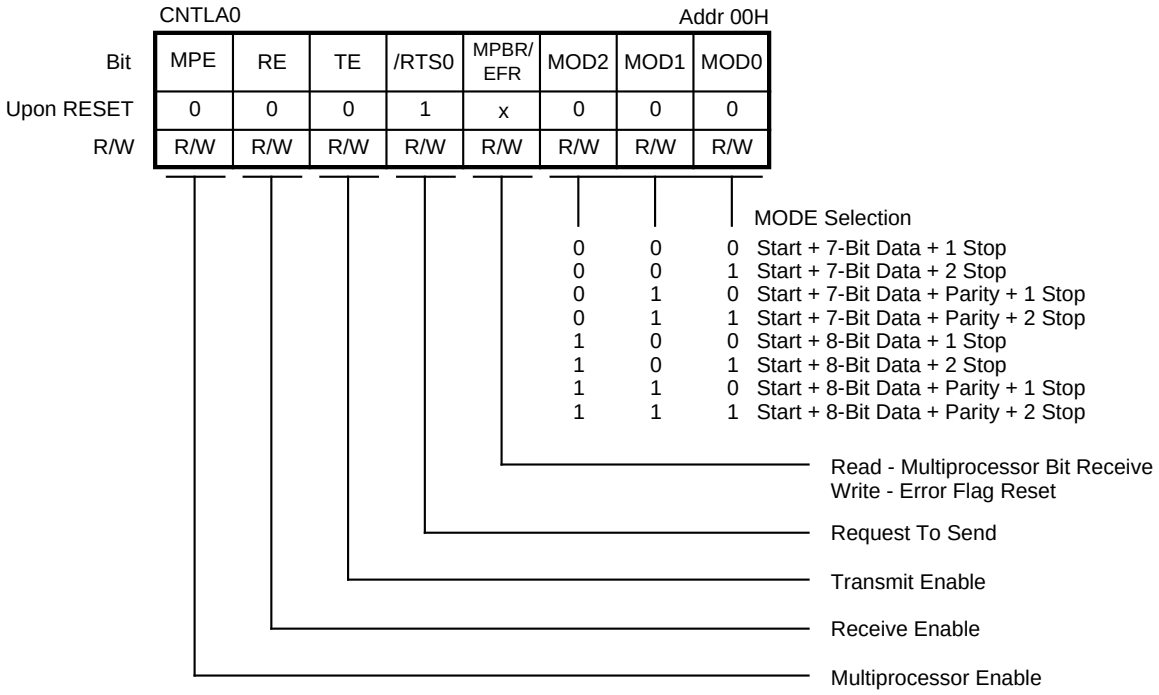
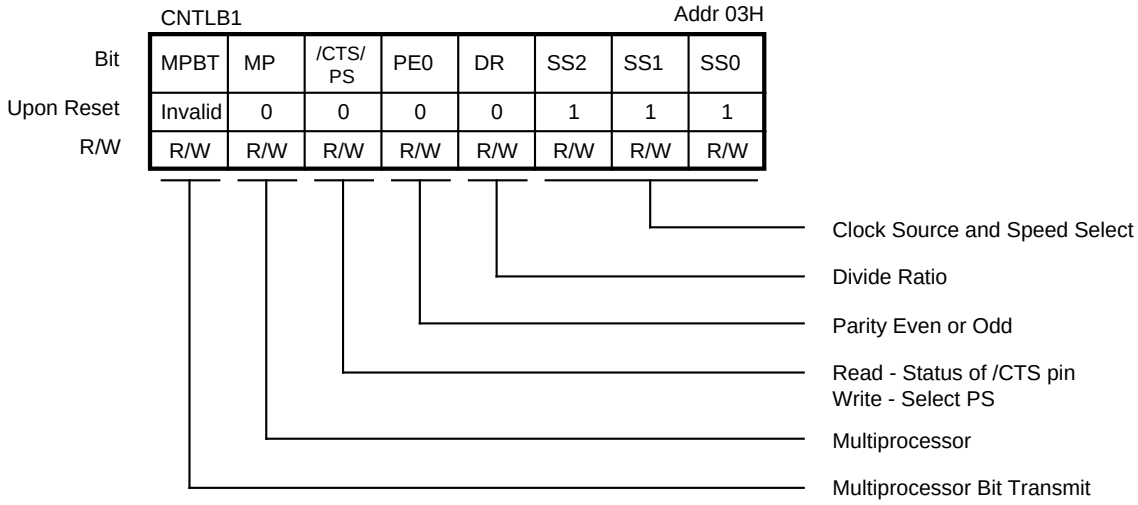


Figure 10a. ASCI Control Register A (Ch. 0)

ASCI CHANNELS CONTROL REGISTERS (Continued)



General Divide Ratio SS, 2, 1, 0	PS = 0 (Divide Ratio = 10) DR = 0 (x16)	DR = 1 (x64)	PS = 1 (Divide Ratio = 30) DR = 0 (x16)	DR = 1 (x64)
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
*111	External Clock (Frequency < Ø ÷ 40)			

Note:
* Baud rate is external clock rate ÷ 16; therefore, Ø ÷ (40 x 16) is maximum baud rate using external clocking.

Figure 12. ASCI Control Register B (Ch. 1)

TIMER DATA REGISTERS

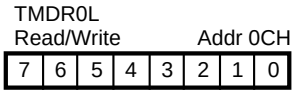


Figure 23. Timer 0 Data Register L

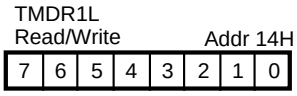
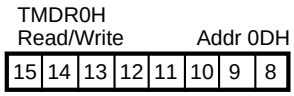
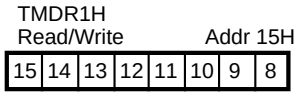


Figure 24. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 25. Timer 0 Data Register H



When Read, read Data Register L before reading Data Register H.

Figure 26. Timer 1 Data Register H

TIMER RELOAD REGISTERS

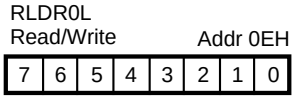


Figure 27. Timer 0 Reload Register L

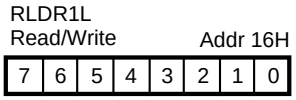


Figure 28. Timer 1 Reload Register L

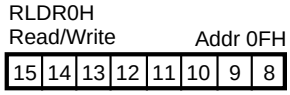


Figure 29. Timer 0 Reload Register H

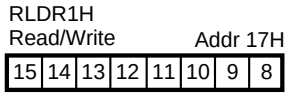


Figure 30. Timer 1 Reload Register H

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Figures 54 through 65 describe miscellaneous registers that control the Z182 configuration, RAM/ROM chip select, interrupt and various status and timers.

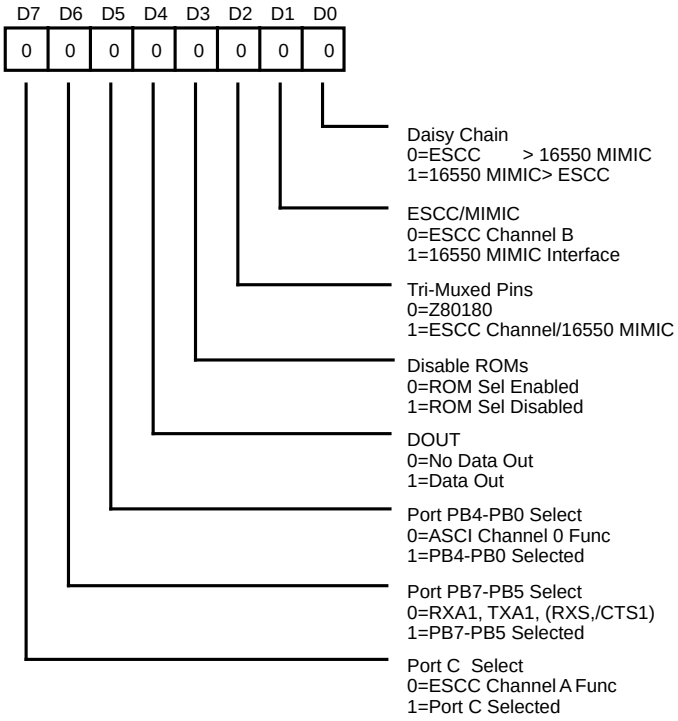


Figure 54. System Configuration Register
(Z180 MPU Read/Write, Address xxEFH)

System Configuration Register

Bit 7 Port C Select
When this bit is set to 1, bit 8 parallel Port C is selected on the multiplexed pins. When this bit is reset to 0 then these multiplexed pins take ESCC™ Channel A functions.

Bit 6 PB7-PB5 Select
When this bit is set to 1, parallel Port B bits 7 through 5 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins become RxA1, TxA1 and RxS/CTS1.

Bit 5 PB4-PB0 Select
When this bit is set to 1, parallel Port B bits 4 through 0 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins take ASCI channel 0 functions.

Bit 4 DD_{OUT} ROM Emulator Mode Enable
When this bit is set to 1, the Z182 is in "ROM emulator mode". In this mode, bus direction for certain transaction periods are set to the opposite direction to export internal bus transactions outside the Z80182/Z8L182. This allows the use of ROM emulators/logic analyzers for application development (see Tables 12a and 12b).

Note: The word "Out" means that the Z182 data bus direction is in output mode, "In" means input mode, and "Z" means high impedance. DD_{OUT} stands for Data Direction Out and is the status of the D4 bit in the System Configuration Register (SCR).

Table 12a. Data Bus Direction (Z182 Bus Master)

I/O And Memory Transactions

	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 /Z8L182 Idle Mode
Z80182 /Z8L182 Data Bus (DD_{OUT} =0)	Out	Z	Out	In	Out	In	Z	Z
Z80182 /Z8L182 Data Bus (DD_{OUT} =1)	Out	Out	Out	In	Out	In	Z	Z

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Table 12b. Data Bus Direction (Z182 Bus Master)

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral (IEI=1)	Intack For Off-Chip Peripheral (IEI=0)
Z80182/Z8L182 Data Bus (DD_{OUT}=0)	Z	In
Z80182/Z8L182 Data Bus (DD_{OUT}=1)	Out	In

Table 13a. Data Bus Direction (Z80182/Z8L182 ***is not*** Bus Master)

I/O And Memory Transactions

	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 Idle Mode
Z80182 /Z8L182 Data Bus DD_{OUT}=0)	In	Out	Z	Z	Z	In	Z	Z
Z80182 /Z8L182 Data Bus (DD_{OUT}=1)	In	Out	Z	Z	Z	In	Z	Z

Table 13b. Data Bus Direction (Z80182/Z8L182 ***is not*** Bus Master)

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral	Intack For Off-Chip Peripheral
Z80182/Z8L182 Data Bus (DD_{OUT}=0)	Out	In
Z80182/Z8L182 Data Bus (DD_{OUT}=1)	Out	In

INTERRUPT EDGE/PIN MUX REGISTER

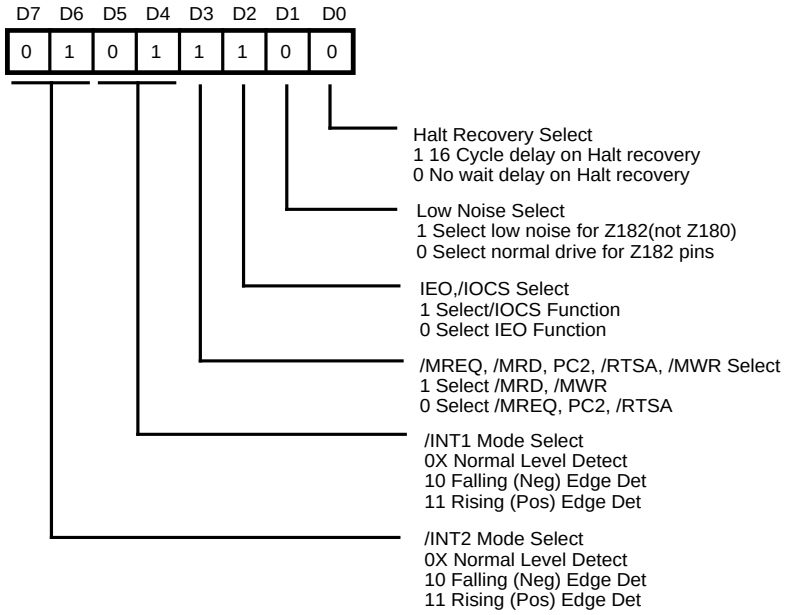


Figure 59. Interrupt Edge/Pin MUX Register
(Z180 MPU Read/Write, Address xxDFH)

Bits 7-6. These bits control the interrupt capture logic for the external /INT2 PIN. When programmed as '0X', the /INT2 pin performs as the normal level detecting interrupt pin. When programmed as 10 the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT2 of the Z180. This interrupt must be cleared by writing a 1 to bit 7 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge.

Bits 5-4. These bits control the interrupt capture logic for the external /INT1 PIN. When programmed as '0X', the /INT1 pin performs as the normal level detecting interrupt pin. When programmed as 10, the negative edge detection is enabled. Any falling edge latches an active Low on the internal /INT1 of the Z180. This interrupt must be cleared by writing a 1 to bit 6 of the Port C Data Register. Programming these control bits to 11 enables rising edge interrupts to be latched. The latch is cleared in the same fashion as the falling edge. Edge detect logic cannot be used in Emulation Adaptor EV mode 1.

Bit 3. Programming this bit to 1 selects the /MRD and the /MWR functions. The default for power up and /RESET conditions is 1, i.e., the /MRD and /MWR. By programming this bit to 0 the /MREQ Z180 function is enabled, as well as the PC2//RTSA function on the PC2//RTSA//MWR pin. If the /MREQ Z180 function is enabled, any external bus master must be prevented from asserting Z182's IRD signal unless accessing Z182's IO.

Bit 2. This bit selects the /IOCS function which is the default for power up and /RESET conditions. By programming this bit to 0 the IEO function is enabled for this multiplexed pin.

Bit 1. This bit selects the low noise or normal drive feature for the Z182 pins . The default at power up is normal drive for Z182 pins. By programming this bit to 1, low noise for the Z182 pins is chosen and the output drive capability of the following pins is reduced to 25% of the original drive capability:

- CKS
- CKA1/TEND0
- CKA0/DREQ0
- RxS/CTS1
- TxA1
- TxA0
- TxS

Programming this bit to 0 selects normal drive for the Z182 pins. Refer to the Z8S180 Product Specification for Low noise control of Z180 pins.

16550 MIMIC REGISTERS

The Z80182/Z8L182 contains the following set of registers for interfacing with the PC/XT/AT.

- Receive Buffer Register
- Transmit Holding Register
- Interrupt Enable Register
- Interrupt Identification Register
- FIFO Control Register
- Line Control Register
- Modem Control Register
- Line Status Register
- Modem Status Register
- Scratch Register
- Divisor Latch Least/Most Significant Bytes
- FIFO Control Register

These registers emulate the 16550 UART and enable the PC/XT/AT to interface with them as with an actual 16550 UART. This allows the Z80182/Z8L182 to be software compatible with existing modem software.

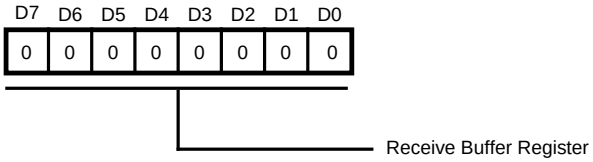


Figure 69. Receive Buffer Register
(PC Read Only, Address 00H, DLAB=0, R/W=Read)
(Z180™ MPU Write Only, Address XXF0H)

Receive Buffer Register

When the Z180 has assembled a byte of data to pass to the PC/XT/AT, it places it in the Receive Buffer Register. If the Received Data Available interrupt is enabled then an interrupt is generated for the PC/XT/AT and the Data Ready bit is set (if the Receive Timer is enabled, the interrupt and setting of the Data Ready bit is delayed until after the timer times out). Also the shadowed bits of the Line Status Register are transferred to their respective bits when the Z180 MPU writes to the Receive Buffer Register (See Line Status Register Bits 1, 2, 3 and 4). This allows a simultaneous setting of error bits when the data is written to the Receive Buffer Register. In FIFO, mode this address is used to read (PC) and write (Z180) the Receive FIFO.

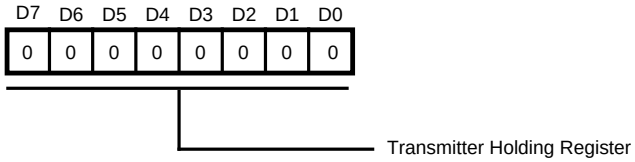


Figure 70. Transmit Holding Register
(PC Write Only, Address 00H, DLAB=0, R/W=Write)
(Z180 MPU Read Only, Address xxF0H)

Transmit Holding Register

When the PC/XT/AT writes to the Transmit Holding Register, the Z80182/Z8L182 responds by setting the appropriate bit in the IP register and by generating an interrupt to the Z180 MPU if it is enabled. When the Z180 MPU reads this register the Transmit Holding Register empty flag is set (if the transmitter timer is enabled , this bit is set after the timer times out). In FIFO mode of operation, this address is used to read (Z180) and write (PC) the Transmitter FIFO.

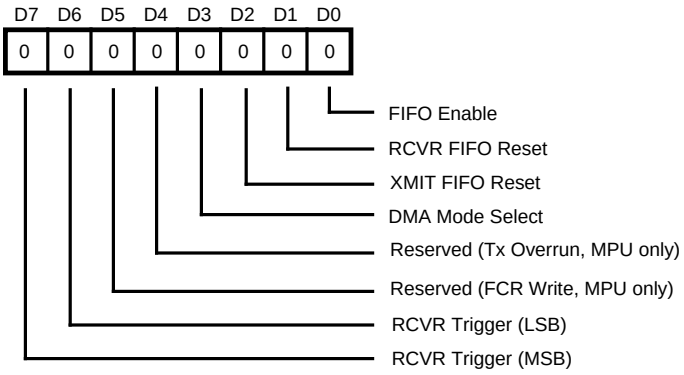


Figure 71. FIFO Control Register
(PC Write Only, Address 02H)
(Z180 MPU Read Only, Address xxE9H)

Z80182/Z8L182 MIMIC DMA CONSIDERATIONS

For the PC Interface, the 16550 device has two modes of operation that need to be supported by the MIMIC. In single transfer mode, the DMA request line for the receiver goes active whenever there is at least one character in the RCVR FIFO. For the transmitter, the DMA request line is active on an empty XMIT FIFO and inactive on non-empty.

In multi-transfer mode, the RCVR DMA goes active at the trigger level and inactive on RCVR FIFO empty. The XMIT DMA is active on non-full XMIT FIFO and inactive on a full XMIT FIFO.

Bit 3 in the FCR controls the DMA mode for the PC interface. If a 1 is programmed into this bit, multi-byte DMA is enabled. A 0 in this bit (default) enables single byte DMA.

As specified, the 16550 does not have any means of handling the error status bits in the FIFO in this multi-transfer mode. Such DMA transfers would require blocks with some checksum or other error checking scheme.

For the MPU interface, the DMA is controlled by a non-empty transmit FIFO and by a non-full receive FIFO conditions (THRE and the DR bits in the LSR). If the delay timers are enabled, the respective shadow bits are used for DMA control. The effect of the DMA logic is to request DMA service when at least one byte of data is available to be read or written to the FIFO's by the Z180. The Z180's DMA channel can be programmed to trigger on edge or on level.

EMULATION MODES

The Z80182/Z8L182 provides four modes of operation. The modes are selected by the EV1 and EV2 pins. These four modes allow the system development and commercial production to be done with the same device. The four emulation modes are shown in Table 20.

Table 20. EV2 and EV1, Emulation Mode Control

	EV2	EV1	EV Description
Mode 0	0	0	Normal Mode, on-chip Z180 bus master
Mode 1	0	1	Emulation Adapter Mode
Mode 2	1	0	Emulator Probe Mode
Mode 3	1	1	RESERVED, for Test Use Only

Mode 0 Normal Mode

This is the normal operating mode for the Z80182/Z8L182.

Mode 1 Emulation Adapter Mode

The Emulation Adaptor Mode enables system development for the Z182 with a readily available Z180 emulator. The Emulator provides the Z180™ MPU and Z180 peripheral functions to the target system, with their signals passing through the emulation adapter. In Emulation Adaptor Mode the Z182s, Z180 MPU and Z180 peripheral signals are tri-state or physically disconnected. The Z182 continues to provide its ESCC, MIMIC, chip select, and Port functions and signals to the target system. The Mode 1 effects on the Z182 are shown in Table 21. Note that INT1-2 Edge Detect Logic cannot be used in Emulation Adaptor EV Mode 2.

EMULATION MODES (Continued)

Table 21. Emulation Mode 1

Signal	Normal Mode 0	Emulation Adaptor Mode 1
PHI	Output	Input
/M1	Output	Input
/MREQ,/MRD	Output	Input
/IORQ	Output	Input
/RD	Output	Input
/WR	Output	Input
/RFSH	Output	Input
/HALT	Output	Input
ST	Output	Input
E	Output	Tri-state
/BUSACK	Output	Input
/WAIT	Input	Output
A19,A18/T_{OUT}	Output	Input
A17-A0	Output	Input
D7-D0	Input/Output	Input/Output
TxA0	Output	Tri-state
/RTS0	Output	Tri-state
TxA1	Output	Tri-state
/INT0	Input	Output, Open-Drain

Mode 2 Emulation Probe Mode
In the Emulator Probe Mode all of the Z182 output signals are tri-state. This scheme allows a Z182 emulator probe to grab on to the Z182 package leads on the target system.

Mode 3 RESERVED (for test purposes only)
This mode is reserved for test purpose only, do not use.

Notes:
Z182 has two branches of reset. /RESET controls the Z182 overall configuration, RAM and ROM boundaries, plus the ESCC, Port and the 16550 MIMIC interface. In Normal Mode, a "one shot" circuit samples the input of the /RESET pin to assert the internal reset to its proper duration. In Adapter Mode, this "one shot" circuit is bypassed. Note also that the Z180's crystal oscillator is disabled in Mode 1 and Mode 2.

In Mode 1 the emulator must provide /MREQ on the (/MREQ,/MRD) Z80182/Z8L182 pin (not /MRD); and A18 (not T_{OUT}) on the A18/T_{OUT} pin.

SLEEP, HALT EFFECT ON MIMIC AND 182 SIGNALS

The following Z80182/Z8L182 signals are driven High when Z180™ MPU enters a SLEEP or HALT state:

- /MRD when selected in the Interrupt Edge/Pin MUX Register.
- /MWR when selected in the Interrupt Edge/Pin MUX Register.
- /ROMCS,/RAMCS always High in SLEEP or HALT.

The following signals are High-Z during SLEEP and HALT:

- /IOCS when so selected in the Interrupt Edge/Pin MUX Register.
- /RD and /WR.

A0-A19 (A18 if selected) always High-Z in power down.

D0-D7 always High-Z in power down modes.

The MIMIC logic of the 182 is disabled during power down modes of the Z180.

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS} ..... –0.3V to +7.0V
Voltages on all inputs
with respect to V_{SS} ..... –0.3V to V_{CC} +0.3V
Operating Ambient Temperature ..... 0 to +70°C
Storage Temperature .....–55°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Figure 89).

Available operating temperature range is:
S = 0°C to +70°C

Voltage Supply Range:
+4.50V ≤ V_{CC} ≤ + 5.50V Z80182
+3.0V ≤ V_{CC} ≤ + 3.60V Z8L182

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

Note: The ESCC™ Core is only guaranteed to operate at 20 MHz 5.0 volts or 10 MHz 3.3 volts. Upon reset, the Z182 system clock is "divided by one" before clocking the ESCC. When Z182 is operated above 20 MHz 5.0 volts or 10 MHz 3.3 volts, the ESCC should be programmed to "divide-by-two" mode.

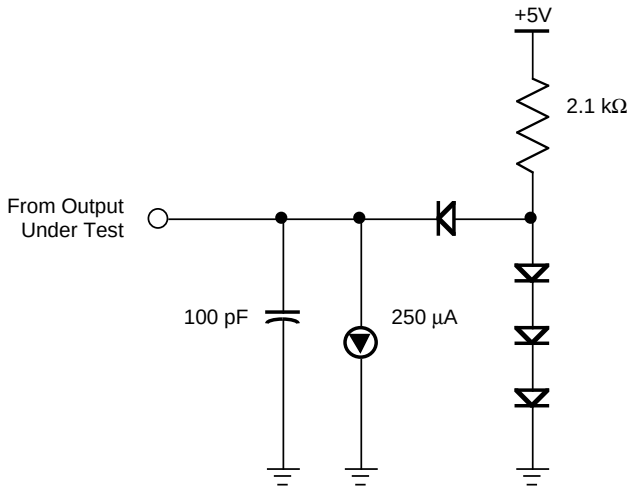


Figure 89. Test Load Diagram

TIMING DIAGRAMS (Continued)

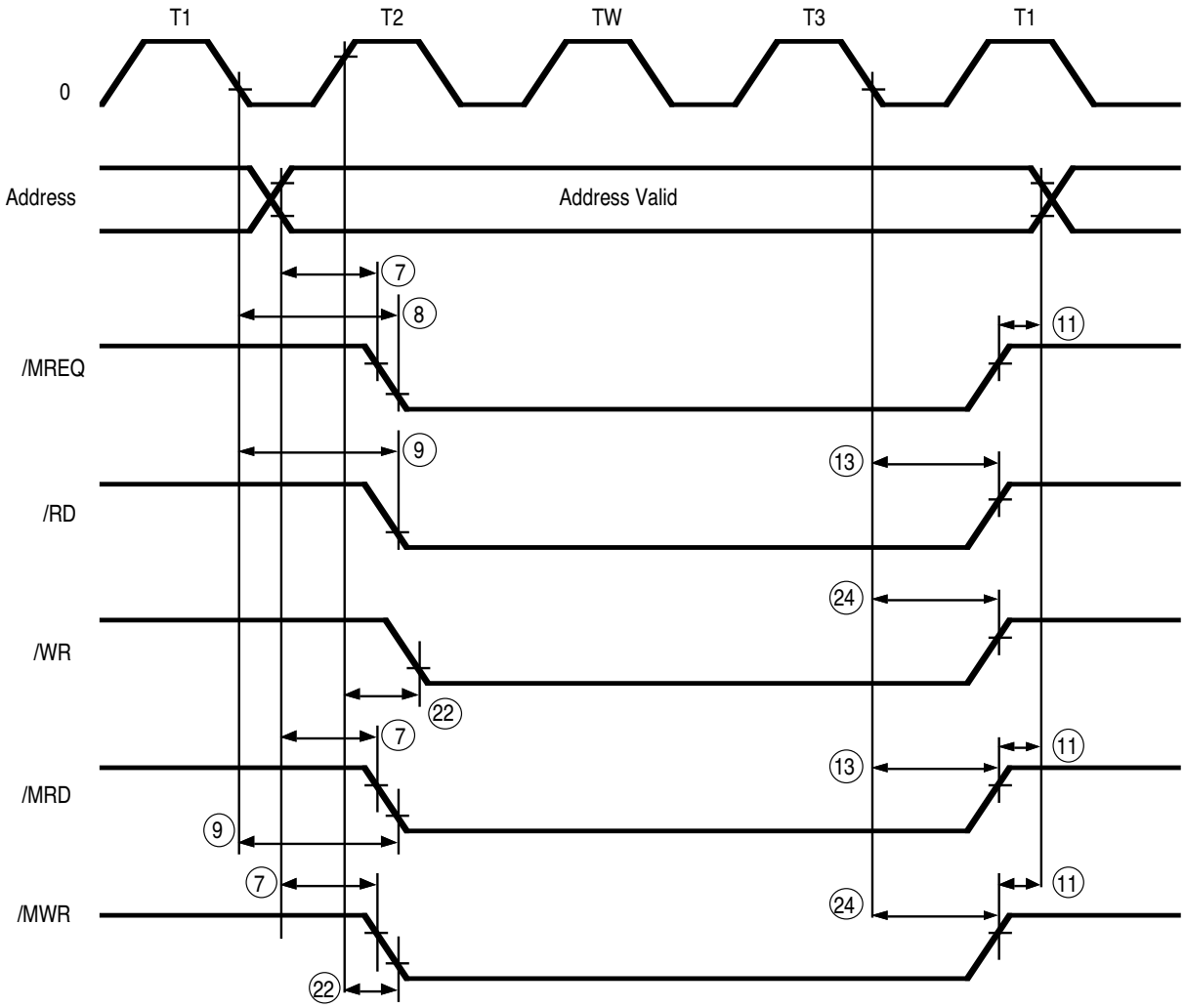


Figure 101. /MWR and /MRD Timing

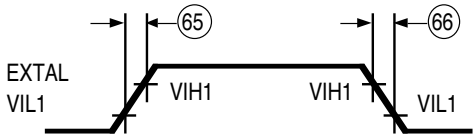


Figure 102. External Clock Rise Time and Fall Time

Figure 103. Input Rise and Fall Time
(Except EXTAL, /RESET)

Z8S180 AC CHARACTERISTICS (Continued)

No.	Sym	Parameter	Z8L180 20 MHz Min	Z8L180 20 MHz Max	Z8S180 33 MHz Min	Z8S180 33 MHz Max	Unit	Note
41	tRFD1	Clock Rise to /RFSH Fall Delay		20		15	ns	
42	tRFD2	Clock Rise to /RFSH Rise Delay		20		15	ns	
43	tHAD1	Clock Rise to /HALT Fall Delay		15		15	ns	
44	tHAD2	Clock Rise to /HALT Rise Delay		15		15	ns	
45	tDRQS	/DREQi Setup Time to Clock Rise	20		15		ns	
46	tDRQH	/DREQi Hold Time from Clock Rise	20		15		ns	
47	tTED1	Clock Fall to /TENDi Fall Delay		25		15	ns	
48	tTED2	Clock Fall to /TENDi Rise Delay		25		15	ns	
49	tED1	Clock Rise to E Rise Delay		30		15	ns	
50	tED2	Clock Edge to E Fall Delay		30		15	ns	
51	PWEH	E Pulse Width (High)	25		20		ns	
52	PWEL	E Pulse Width (Low)	50		40		ns	
53	tEr	Enable Rise Time		10		10	ns	
54	tEf	Enable Fall Time		10		10	ns	
55	tTOD	Clock Fall to Timer Output Delay		75		50	ns	
56	tSTDI	CSI/O Tx Data Delay Time (Internal Clock Operation)		75		60	ns	
57	tSTDE	CSI/O Tx Data Delay Time (External Clock Operation)		7.5 tcyc+100		7.5 tcyc+100	ns	
58	tSRSI	CSI/O Rx Data Setup Time (Internal Clock Operation)		1	1		tcyc	
59	tSRHI	CSI/O Rx Data Hold Time (Internal Clock Operation)		1	1		tcyc	
60	tSRSE	CSI/O Rx Data Setup Time (External Clock Operation)		1	1		tcyc	
61	tSRHE	CSI/O Rx Data Hold Time (External Clock Operation)		1	1		tcyc	
62	tRES	/RESET Setup time to Clock Fall	40		25		ns	
63	tREH	/RESET Hold time from Clock Fall	25		15		ns	
64	tOSC	Oscillator Stabilization Time		20		20	ms	
65	tEXr	External Clock Rise Time (EXTAL)		10		5	ns	
66	tEXf	External Clock Fall Time (EXTAL)		10		5	ns	
67	tRr	/RESET Rise Time		50		50	ms	[2]
68	tRf	/RESET Fall Time		50		50	ms	[2]
69	tIr	Input Rise Time (Except EXTAL, /RESET)		50		50	ns	[2]
70	tIf	Input Fall Time (Except EXTAL, /RESET)		50		50	ns	[2]
71	TdCS	/MREQ Valid to /ROMCS, /RAMCS Valid Delay		15		10	ns	
72	TdIOCS	/IORQ Valid to /IOCS Valid Delay		15		10	ns	

Notes:
These AC parameters values are preliminary and subject to change without notice.
[1] All specifications reflect 100% output drive (disabled slew rate limiting feature).
[2] Specification 1 through 5 refer to PHI clock output.
[3] Exceeds characterization (data propagation delay needs to be analyzed).

16550 MIMIC TIMING

Refer to Figures 106 thru 112 for MIMIC AC Timing.

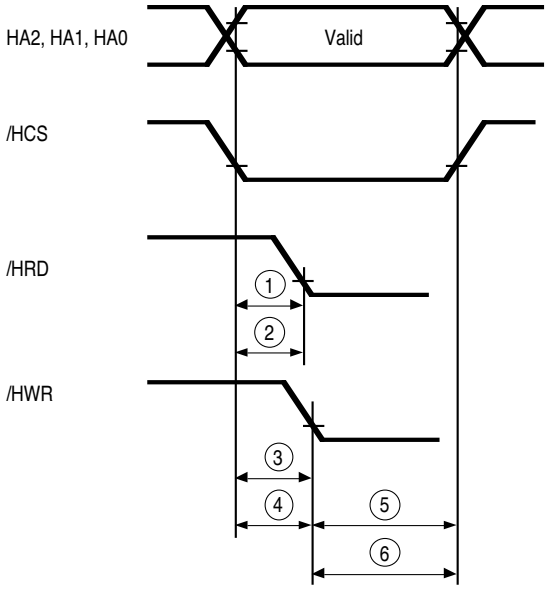


Figure 110. PC Host /RD /WR Timing

Table H. PC Host /RD /WR Timing

No	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
1	tAR	/HRD Delay from Address	30		30		ns
2	tCSR	/HRD Delay from /HCS	30		30		ns
3	tAW	/HWR Delay from Address	30		30		ns
4	tCSW	/HWR Delay from /HCS	30		30		ns
5	tAh	Address Hold Time	20		20		ns
6	tCSh	/HCS Hold Time	20		20		ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

16550 MIMIC TIMING (Continued)

Table K. Interrupt Timing RCVR FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
14	tSINT	Delay from Stop to Set Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles
15	tRINT	Delay from /HRD (RD RBR or RD LSR) to Reset Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles

Note:
These AC parameter values are preliminary and are subject to change without notice.

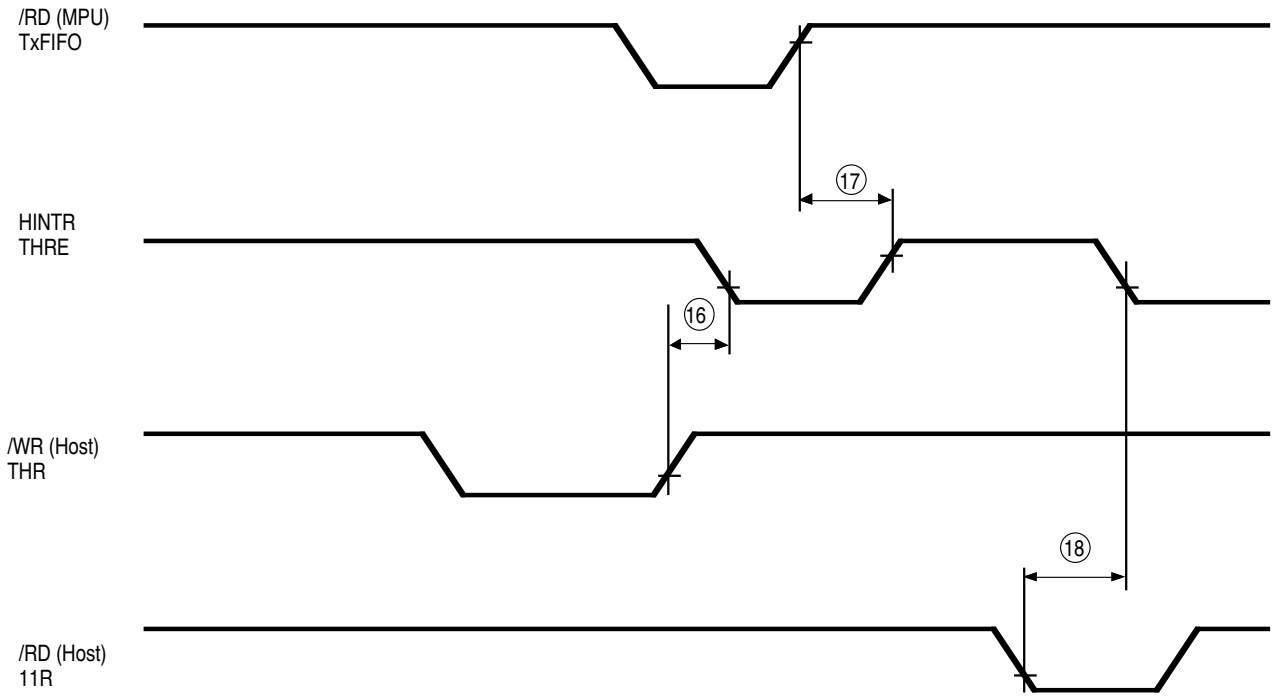


Figure 115. Interrupt Timing Transmitter FIFO