Zilog - Z8018216FSC1838TR Datasheet

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Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	16MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018216fsc1838tr

GENERAL DESCRIPTION (Continued)

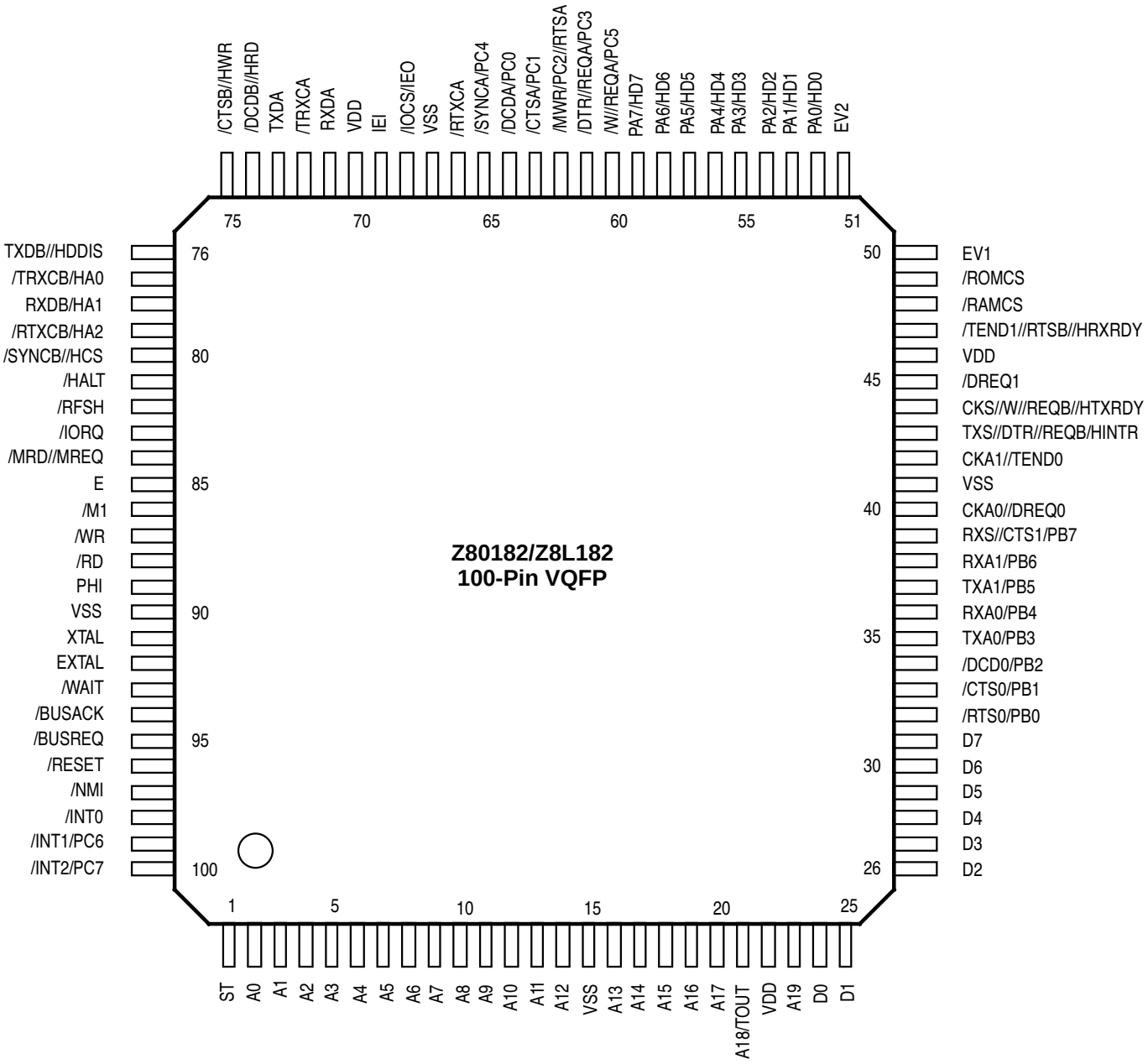


Figure 3. Z80182/Z8L182 100-Pin VQFP Pin Configuration

Z180 CPU SIGNALS

A19-A0. *Address Bus (input/output, active High, tri-state).* A19-A0 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges up to 1 Mbyte, and I/O data bus exchanges up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states. This bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset).

D7-D0. *Data Bus (bi-directional, active High, tri-state).* D7-D0 constitute an 8-bit bi-directional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

/RD. *Read (input/output, active Low, tri-state).* /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

/WR. *Write (input/output, active Low, tri-state).* /WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

/IORQ. *I/O Request (input/output, active Low, tri-state).* /IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. /IORQ is also generated, along with /M1, during the acknowledgment of the /INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

/M1. *Machine Cycle 1 (input/output, active Low).* Together with /MREQ, /M1 indicates that the current cycle is the opcode fetch cycle of an instruction execution; unless /M1E bit in the OMCR is cleared to 0. Together with /IORQ, /M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the /HALT and ST signals to decode status of the CPU machine cycle. This signal is analogous to the /LIR signal of the Z64180.

/MREQ. *Memory Request (input/output, active Low, tri-state).* /MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the /ME signal of the Z64180. /MREQ is multiplexed with /MRD on the /MRD//MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if the /MREQ function is selected; and is inactive High if /MRD function is selected.

/MRD. *Memory Read (input/output, active Low, tri-state).* /MRD is active when both the internal /MREQ and /RD are active. /MRD is multiplexed with /MREQ on the /MRD //MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if /MREQ function is selected; and is inactive High if /MRD function is selected. The default function on power up is /MRD and may be changed by programming bit 3 of the Interrupt Edge/Pin MUX Register (xxDFH).

/MWR. *Memory Write (input/output, active Low, tri-state).* /MWR is active when both the internal /MREQ and /WR are active. This /RTSA or PC2 combination is pin multiplexed with /MWR on the /MWR/PC2//RTSA pin. The default function of this pin on power up is /MWR, which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/WAIT. *(input/output active Low).* /WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The /WAIT input is sampled on the falling edge of T2 (and subsequent wait states). If the input is sampled Low, then additional wait states are inserted until the /WAIT input is sampled High, at which time execution will continue.

/HALT. *Halt/Sleep Status (input/output, active Low).* This output is asserted after the CPU has executed either the HALT or SLEEP instruction, and is waiting for either non-maskable or maskable interrupts before operation can resume. It is also used with the /M1 and ST signals to decode status of the CPU machine cycle. On exit of HALT/SLEEP mode, the first instruction fetch can be delayed by 16 clock cycles after the /HALT pin goes High, if HALT 16 feature is selected.

/BUSACK. *Bus Acknowledge (input/output, active Low).* /BUSACK indicates to the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

/BUSREQ. *Bus Request (input, active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address/data buses and other control signals, into the high impedance state.

Z85230 ESCC SIGNALS (Continued)

/SYNCA, /SYNCB. *Synchronization (inputs/outputs, active Low).* These pins can act as either inputs, outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to /CTS and /DCD. In this mode, transitions on these lines affect the state of the Sync /Hunt status bits in Read Register 0, but have no other function. /SYNCA is also multiplexed with PC4 (parallel Port C, bit 4) on the /SYNCA/PC4 pin.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode /SYNC must be driven Low two receive clock cycles after the last bit in the sync character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.

In the Internal Synchronization mode, (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync character is recognized (regardless of the character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. In Z80182/Z8L182 mode 1 the /SYNCB signal is multiplexed with the 16550 MIMIC interface /HCS input on the /SYNCB //HCS pin.

/CTSA. *Clear To Send (input, active Low).* If this pin is programmed as auto enable, a Low on this input enables the channel A transmitter. If not programmed as auto enable, it may be used as a general-purpose input. The input is Schmitt-trigger buffered to accommodate slow rise-time input. The ESCC™ detects transitions on this input and can interrupt the Z180™ MPU on either logic level transitions. /CTSA is multiplexed with PC1 (parallel Port C, bit 1) on the /CTSA/PC1 pin.

/CTSB. *Clear To Send (input, active Low).* This pin is similar to /CTSA's functionality but is applicable to the channel B transmitter. In Z80182/Z8L182 mode, the /CTSB signal is multiplexed with the 16550 MIMIC interface /HWR input on the /CTSB //HWR pin.

/DCDA. *Data Carrier Detect (input, active Low).* This pin functions as receiver enables if it is programmed as an auto enable bit; otherwise, it may be used as a general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects transitions on this pin and can interrupt the Z180 MPU on either logic level transitions. /DCDA is also multiplexed with PC0 (parallel Port C, bit 0) on the /DCDA/PC0 pin.

/DCDB. *Data Carrier Detect (input, active Low).* This pin's functionality is similar to /DCDA but applicable to the channel B receiver. In Z80182/Z8L182 mode 1, /DCDB is multiplexed with the 16550 MIMIC interface /HRD input on the /DCDB//HRD pin.

/RTSA. *Request to Send (output, active Low).* When the Request to Send (RTS) bit in Write Register 5 channel A is set, the /RTSA signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with auto enables off, the /RTSA pin strictly follows the state of the RTS bit. The pin can be used as general-purpose output. /RTSA is multiplexed with PC2 (parallel Port C bit 2). This /RTSA or PC2 combination is pin multiplexed with /MWR (active when both the internal /MREQ and /WR are active) on the /MWR/PC2//RTSA pin. The default function of this pin on power-up is /MWR which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/RTSB. *Request to Send (output, active Low).* This pin is similar in functionality as /RTSA but is applicable on channel B. The /RTSB signal is multiplexed with the Z180 MPU /TEND1 signal and the 16550 MIMIC interface /HRxRDY signal on the /TEND1//RTSB//HRxRDY pin.

/DTR//REQA. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. /DTR//REQA is also multiplexed with PC3 (parallel Port C, bit 3) on the /DTR//REQA /PC3 pin.

/DTR//REQB. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. The /DTR//REQB signal is multiplexed with the Z180 MPU TxS signal and the 16550 MIMIC interface HINTR signal on the /TxS//DTR//REQB //HINTR pin.

/W//REQA. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This dual-purpose output can be programmed as Request (receive) lines for a DMA controller or as Wait lines to synchronize the Z180 MPU to the ESCC data rate. The reset state is Wait. The ESCC allows full duplex DMA transfers. /W//REQA is also multiplexed with PC5 (parallel Port C, bit 5) on the /W//REQA/PC5 pin.

MULTIPLEXED PIN DESCRIPTIONS

A18/$T_{OUT.}$ During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, The T_{OUT} function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/T_{OUT}. Therefore, the selection of T_{OUT} will not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

CKA0//DREQ0. During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, /DREQ0 function is always selected.

CKA1//TEND0. During Reset, this pin is initialized as CKA1 pin. If CKA1D bit in the ASCI control register Ch1(CNTLA1) is set to 1, /TEND0 function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

RxS//CTS1. During Reset, this pin is initialized as the RxS pin. If CTS1E bit in the ASCI status register Ch1 (STAT1) is set to 1, /CTS1 function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 2 specifies. On Reset, both bits 1 and 2 are 0, so /TEND1,TxS,CKS are selected.

Table 2. Triple Multiplexed Pins

Bit 1	Bit 2	Master Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/RTSB,/DTR//REQB,/W//REQB
1	0	/TEND1,TxS,CKS
1	1	/HRxRDY,//HTxRDY,HINTR

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is 0, then the Z80182/Z8L182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is 1, then Z80182/Z8L182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182/Z8L182 Mode 0 is always selected as shown in Table 3.

Table 3. Mode 0 and Mode 1 Multiplexed Pins

Z80182/Z8L182 Mode 0	Z80182/Z8L182 Mode 1
TxDB	/HDDIS
RxDB	HA1
/TRxCB	HA0
/RTxCB	HA2
/SYNCB	/HCS
/CTSB	/HWR
/DCDB	/HRD
PA7-PA0	HD7-HD0

Z182 CPU

The Z182 CPU is 100% software compatible with the Z80® CPU and has the following additional features:

Faster Execution Speed. The Z182 CPU is "fine tuned," making execution speed, on average, 10% to 20% faster than the Z80 CPU.

Enhanced DRAM Refresh Circuit. Z182 CPU's DRAM refresh circuit does periodic refresh and generates an 8-bit refresh address. It can be disabled or the refresh period adjusted, through software control.

Enhanced Instruction Set. The Z182 CPU has seven additional instructions to those of the Z80 CPU, which include the MLT (Multiply) instruction.

HALT and Low Power Modes of Operation. The Z182 CPU has HALT and Low Power modes of operation, which are ideal for the applications requiring low power consumption like battery operated portable terminals.

System Stop Mode. When the Z182 is in System Stop mode, it is only the Z180 MPU that is in STOP mode.

Standby and Idle Mode. Please refer to the Z8S180 Product Specification for additional information on these two additional Low Power modes.

Instruction Set. The instruction set of the Z182 CPU is identical to the Z180. For more details about each transaction, please refer to the Product Specification/ Technical Manual for the Z180/Z80 CPU.

Z182 CPU Basic Operation

Z182 CPU's basic operation consists of the following events. These are identical to the Z180 MPU. For more details about each operation, please refer to the Product Specification/Technical Manual for the Z180.

- Operation Code Fetch Cycle
- Memory Read/Write Operation
- Input/Output Operation
- Bus Request/Acknowledge Operation
- Maskable Interrupt Request Operation
- Trap and Non-Maskable Interrupt Request Operation
- HALT and Low Power Modes of Operation
- Reset Operation

Memory Management Unit (MMU)

The Memory Management Unit (MMU) allows the user to map the memory used by the CPU (64 Kbytes of logical addressing space) into 1 Mbyte of physical addressing space. The organization of the MMU allows object code compatibility with the Z80 CPU while offering access to an extended memory space. This is accomplished by using an effective common area-banked area scheme.

DMA Controller

The Z182 MPU has two DMA controllers. Each DMA controller provides high-speed data transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory-to/from-I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. The DMA can access the full 1 Mbytes addressing range with a block length up to 64 Kbytes and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI)

This unit provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels also support a multiprocessor communication format.

Programmable Reload Timer (PRT)

The Z182 MPU has two separate Programmable Reload Timers, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is system clock divided by 20. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSI/O)

The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another CPU or MPU.

Programmable Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z182 MPU unit has a programmable wait state generator. By programming the DMA/WAIT Control Register (DCNTL), up to three wait states are automatically inserted in memory and I/O cycles. This unit also inserts wait states during on-chip DMA transactions. When using RAMCS and ROMCS wait state generators, the wait state controller with the most programmed wait states will determine the number of wait states inserted.

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source
  - Up to 5 Mbits/sec at 20 MHz PCLK (ESCC).
- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit
- NRZ, NRZI or FM encoding/decoding. Manchester Code Decoding (Encoding with External Logic).
- Baud Rate Generator in each Channel
- Digital Phase-Locked Loop (DPLL) for Clock Recovery
- Crystal Oscillator

The following features are implemented in the ESCC™ for the Z80182/Z8L182 only:

- New 32-bit CRC-32 (Ethernet Polynomial)
- ESCC Programmable Clock
  - programmed to be equal to system clock divided by one or two
  - programmed by Z80182 Enhancement Register

Note: The ESCC™ programmable clock must be programmed to divide-by-two mode when operating above the following conditions:

– PHI > 20 MHz at 5.0V

– PHI > 10 MHz at 3.0V

Z80182 MIMIC DOUBLE BUFFERING FOR THE TRANSMITTER

The Z80182 Rev DA implements double buffering for the transmitter in 16450 mode and sets the TEMT bit in the LSR Register automatically.

When this feature is enabled and character delay emulation is being used (see Figure 9):

1. The PC THRE bit in the LSR Register is set when the THR Register is empty;
2. PC Host writes to the 16450 THR Register;
3. Whenever the Z80182 TSR buffer is empty and one character delay timer is in a timed-out state, the byte from the THR Register is transferred to the TSR buffer; the timer is in timed-out state after FIFO Reset or after Host TEMT is set. This allows a dual write to THR when Host TEMT is set.
4. Restart character delay timer (timer reloads and counts down) with byte transfer from THR Register to the TSR buffer;
5. Whenever the TSR buffer is full, the TEMT bit in MPU LSR Register is reset with no delay;
6. MPU reads TSR buffer;
7. TEMT bit in LSR Register for MPU is set with no delay whenever the TSR buffer is empty;
8. When the TSR buffer is read by MPU and THR Register is empty and one character delay timer reaches zero, the TEMT bit in the LSR Register for Host is set from 0 to 1.

The PC THRE bit in the LSR Register is reset whenever the THR Register is full and set whenever THR Register is empty.

MPU IREQ and DMA Request for the transmit data is trigger whenever TSR buffer is full and cleared whenever TSR buffer is empty.

If character delay emulation is not used the TEMT bit in the LSR Register is set whenever both the THR Register and the TSR buffer are both empty. The Host TEMT bit is clear if there is data in either the TSR buffer of THR Register.

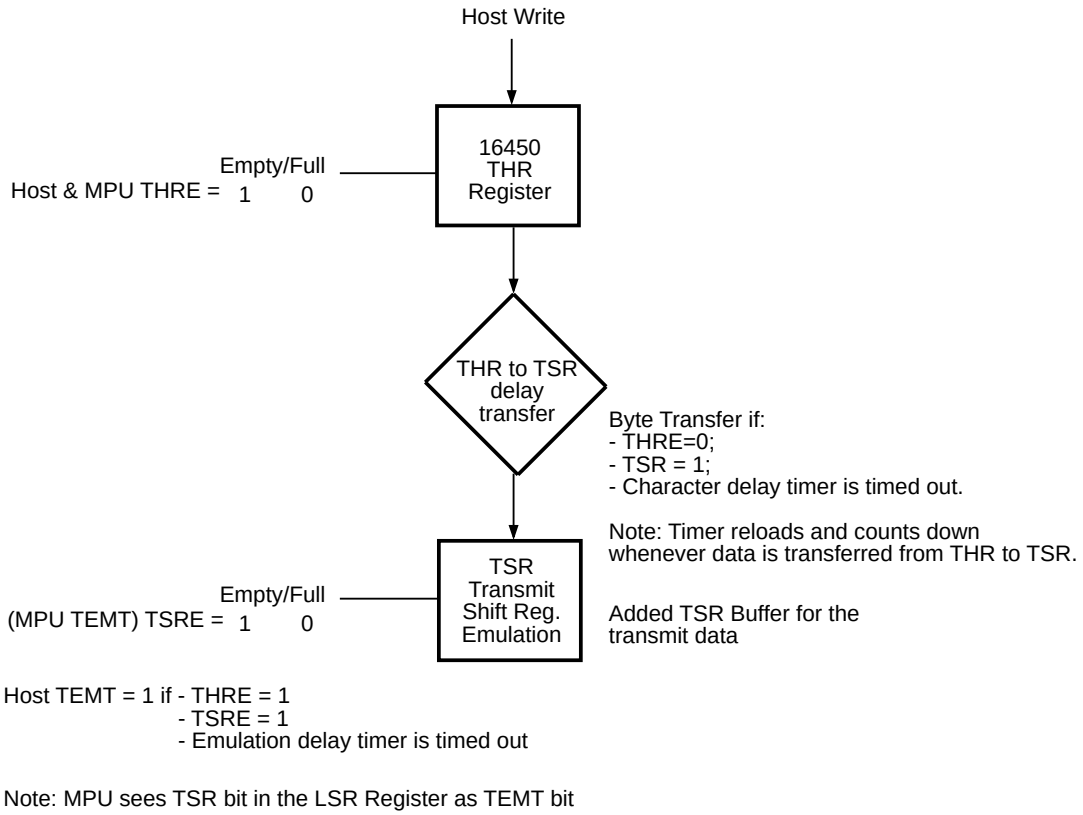
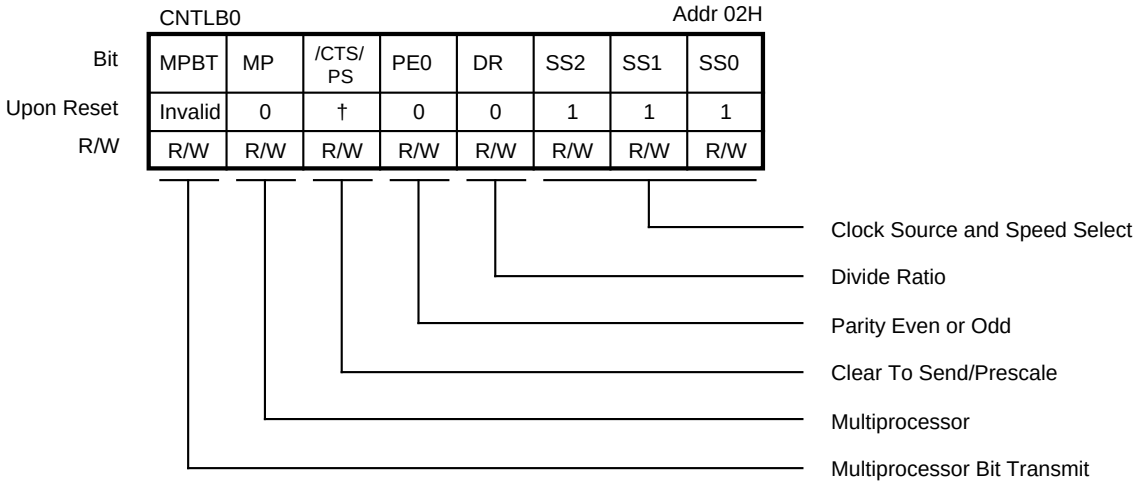


Figure 9. TEMT Emulation Logic Implementation



† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

General Divide Ratio	PS = 0 (Divide Ratio = 10)		PS = 1 (Divide Ratio = 30)	
SS, 2, 1, 0	**DR = 0 (x16)**	**DR = 1 (x64)**	**DR = 0 (x16)**	**DR = 1 (x64)**
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

Figure 11. ASCI Control Register B (Ch. 0)

DMA REGISTERS (Continued)

DSTAT — Addr 30H

Bit	DE1	DE0	/DWE1	/DWE0	DIE1	DIE0	-	DIME
Upon Reset	0	0	1	1	0	0	1	0
R/W	R/W	R/W	W	W	R/W	R/W		R

- DIME: DMA Master Enable
- DIE1, DIE0: DMA Interrupt Enable 1, 0
- /DWE1, /DWE0: DMA Enable Bit Write Enable 1, 0
- DE1, DE0: DMA Enable Ch 1, 0

Figure 40. DMA Status Register

DMODE — Addr 31H

Bit	-	-	DM1	DM0	SM1	SM0	MMOD	-
Upon Reset	1	1	0	0	0	0	0	1
R/W			R/W	R/W	R/W	R/W	R/W	

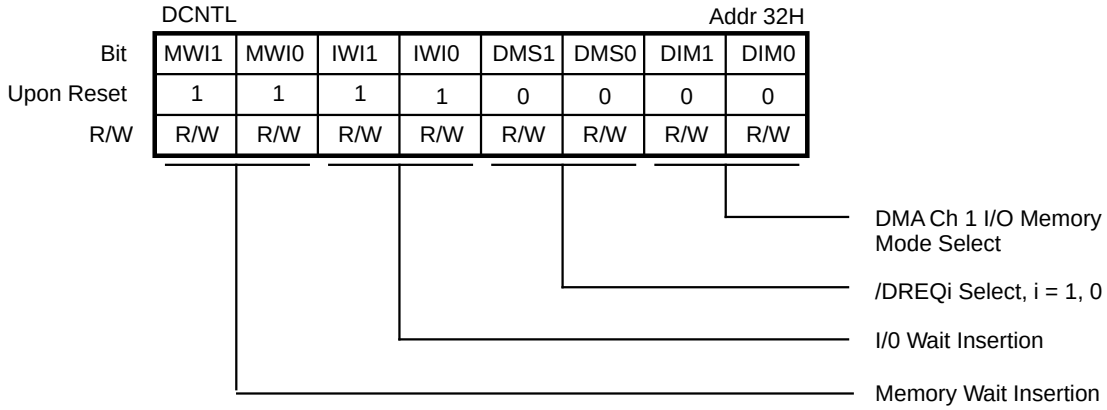
- MMOD: Memory MODE Select
- SM1, SM0: Ch 0 Source Mode 1, 0
- DM1, DM0: Ch 0 Destination Mode 1, 0

DM1, 0	Destination	Address
00	M	DAR0+1
01	M	DAR0-1
10	M	DAR0 Fixed
11	I/O	DAR0 Fixed

SM1, 0	Source	Address
00	M	SAR0+1
01	M	SAR0-1
10	M	SAR0 Fixed
11	I/O	SAR0 Fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

Figure 41. DMA Mode Registers



*

MWI1, 0	No. of Wait States
00	0
01	1
10	2
11	3

IWI1, 0	No. of Wait States
00	1
01	2
10	3
11	4

DMSi	Sense
1	Edge Sense
0	Level Sense

DM1, 0	Transfer Mode	Address Increment/Decrement	
00	M - I/O	MAR1+1	IAR1 Fixed
01	M - I/O	MAR1-1	IAR1 Fixed
10	I/O - M	IAR1 Fixed	MAR1+1
11	I/O - M	IAR1 Fixed	MAR1-1

Note:
* If using ROM/RAM Chip Select wait state generators, the Z180 wait state generator should be set to 0.

Figure 42. DMA/WAIT Control Register

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is stopped completely. IDLE mode is exited in a similar way as STANDBY mode, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS, except that the 2^{17} bit wake-up timer is bypassed; all control signals are asserted eight clock cycles after the exit conditions are gathered.

STANDBY-QUICK RECOVERY Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from 2^{17} clock cycles (6.5 ms at 20 MHz) to 2^{6} clock cycles (3.2 µs at 20 MHz). This feature can only be used when providing an oscillator as clock source.

To enter STANDBY-QUICK RECOVERY mode:

1. Set D6 and D3 to 1 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS; the clock and other control signals are recovered sooner than the STANDBY mode.

Note: If STANDBY-QUICK RECOVERY is enabled, the user must make sure stable oscillation is obtained within 64 clock cycles.

CPU Control Register

The Z8S180 has an additional register which allows the programmer to select options that directly affect the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU Control Register (CCR) allows the programmer to change the divide-by-two internal clock to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 can reduce the output drivers on selected groups of pins to 25% of normal pad driver capability which minimizes the EMI noise generated by the part.

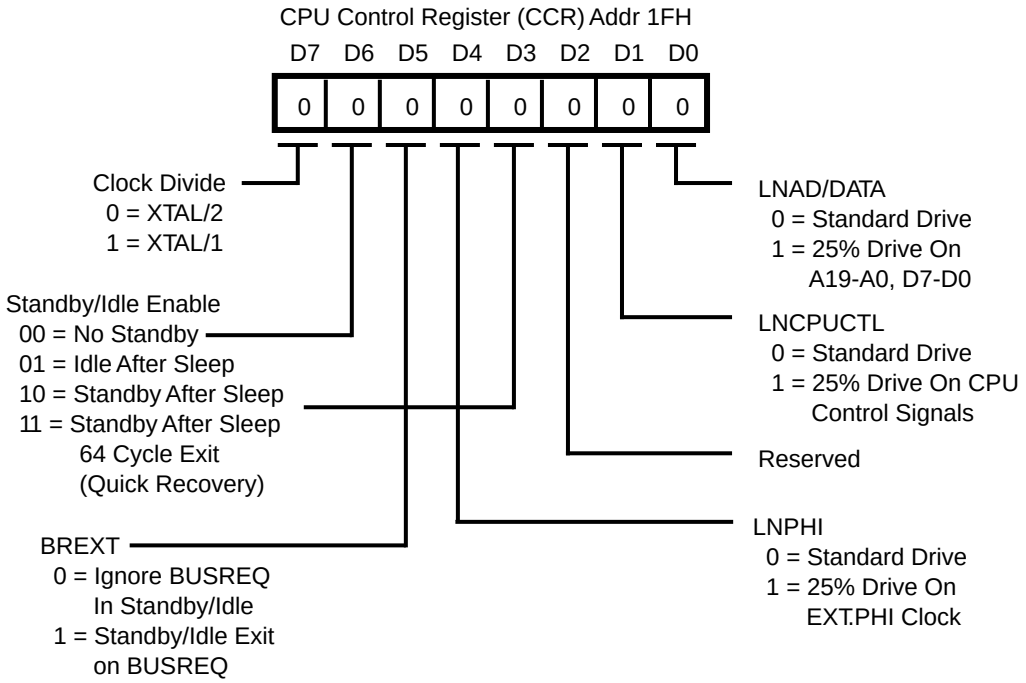


Figure 51. CPU Control Register

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Figures 54 through 65 describe miscellaneous registers that control the Z182 configuration, RAM/ROM chip select, interrupt and various status and timers.

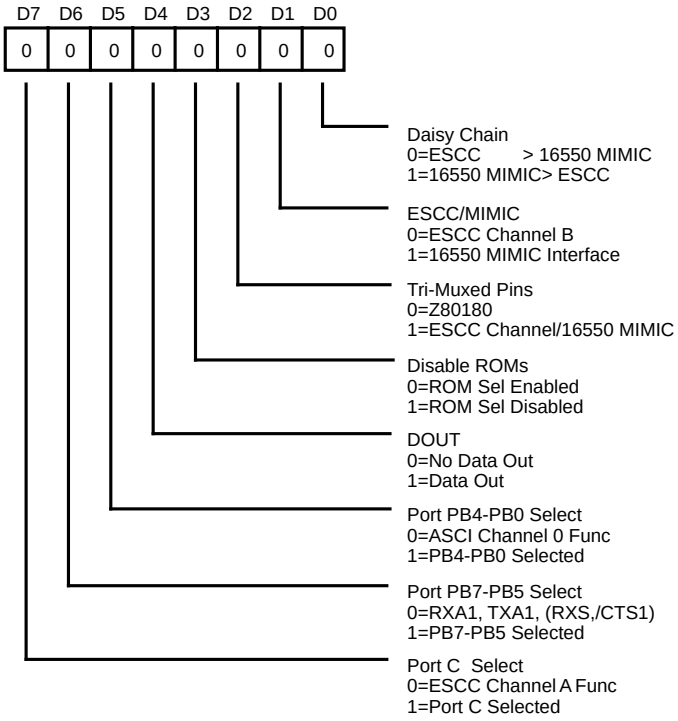


Figure 54. System Configuration Register
(Z180 MPU Read/Write, Address xxEFH)

System Configuration Register

Bit 7 Port C Select
When this bit is set to 1, bit 8 parallel Port C is selected on the multiplexed pins. When this bit is reset to 0 then these multiplexed pins take ESCC™ Channel A functions.

Bit 6 PB7-PB5 Select
When this bit is set to 1, parallel Port B bits 7 through 5 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins become RxA1, TxA1 and RxS/CTS1.

Bit 5 PB4-PB0 Select
When this bit is set to 1, parallel Port B bits 4 through 0 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins take ASCI channel 0 functions.

Bit 4 DD_{OUT} ROM Emulator Mode Enable
When this bit is set to 1, the Z182 is in "ROM emulator mode". In this mode, bus direction for certain transaction periods are set to the opposite direction to export internal bus transactions outside the Z80182/Z8L182. This allows the use of ROM emulators/logic analyzers for application development (see Tables 12a and 12b).

Note: The word "Out" means that the Z182 data bus direction is in output mode, "In" means input mode, and "Z" means high impedance. DD_{OUT} stands for Data Direction Out and is the status of the D4 bit in the System Configuration Register (SCR).

Table 12a. Data Bus Direction (Z182 Bus Master)

I/O And Memory Transactions

	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 /Z8L182 Idle Mode
Z80182 /Z8L182 Data Bus (DD_{OUT} =0)	Out	Z	Out	In	Out	In	Z	Z
Z80182 /Z8L182 Data Bus (DD_{OUT} =1)	Out	Out	Out	In	Out	In	Z	Z

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Bit 3 Disable ROMs
If this bit is 1, it disables the ROMCS pin. If it is 0, addresses below the ROM boundary set by the ROMBR register will cause the ROMCS pin to go Low.

Bit 2 Tri-Muxed Pins Select
The Z80182/Z8L182 has three pins that are triple multiplexed and controlled by bit 2 and bit 1. Table 14 shows the different modes.

Table 14. SCR Control for Triple Multiplexed Pins

Bit 2	Bit 1	System Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/TEND1,TxS,CKS
1	0	/RTSB,(/DTR//REQB),(/W//REQB)
1	1	/HRxRDY,//HTxRDY,HINTR

Bit 1 ESCC™ Channel B/MIMIC
If this bit is 0, Mode 0 is selected.
If this bit is 1, Mode 1 is selected.

Mode 0:
Channel A ESCC Enabled
Channel B ESCC Enabled
PIA Port Enabled
16550 MIMIC Interface Disabled

Mode 1:
Channel A ESCC enabled
Channel B outputs disabled
PIA disabled
16550 MIMIC Interface Enabled

Bit 0 Daisy Chain
This bit is used to set interrupt priority of the ESCC and 16550 MIMIC interface. If it is 0, the ESCC is higher up in the daisy chain than the 16550 MIMIC interface. If it is 1, the 16550 interface is higher up than the ESCC. Note that /INT0 is used for both MIMIC and ESCC Interrupts.

/RAMCS AND /ROMCS REGISTERS

To assist decoding of ROM and RAM blocks of memory, three more registers and two pins have been added to the Z80182/Z8L182. The two pins are /ROMCS and /RAMCS. The three registers are RAMUBR, RAMLBR and ROMBR.

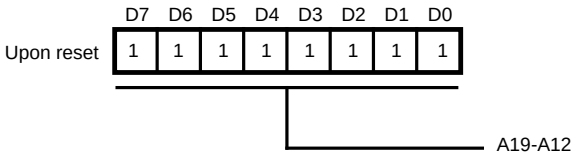


Figure 55. RAMUBR
(Z180 MPU Read/Write, Address xxE6H)

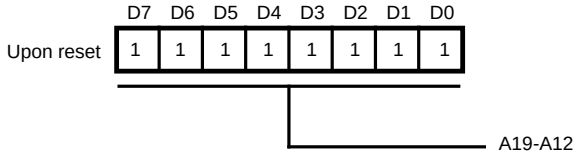


Figure 56. RAMLBR
(Z180 MPU Read/Write, Address xxE7H)

DC CHARACTERISTICS

Z80182/Z8L182

(V_{CC} = 5V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL, NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL, NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL, NMI	–0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL, NMI	–0.3		0.8	V	
V_{OH1}	Output H Voltage	2.4			V	I_{OH} = –200 µA
	All outputs	V_{CC} –1.2				I_{OH} = –200 µA
V_{OH2}	Output H PHI	V_{CC} –0.6			V	I_{OH}= –200 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.2 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{TL}	Tri-state Leakage Current			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{CC}*	Power Dissipation*		60	120	mA	f = 20 MHz
	(Normal Operation)		100	200	mA	f = 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(SLEEP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(I/O STOP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		5	10	mA	f = 20 MHz
	(SYSTEM STOP mode)		9	17	mA	f = 33 MHz
	IDLE Mode		TBD	TBD	mA	f = 20 MHz
			TBD	TBD	mA	f = 33 MHz
	STANDBY Mode		50		µA	f = 0 MHz †
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:

These I_{CC} values are preliminary and subject to change without notice.

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
V_{CC} = 5.0V; (I_{OH} Low EMI) = -50 µA, I_{OL} (Low EMI) = 500 µA

† Device may take up to two seconds before stabilizing to steady state standby current.

DC CHARACTERISTICS

Z80182/Z8L182

(V_{CC} = 3.3V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL, NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL, NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL, NMI	–0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL, NMI	–0.3		0.8	V	
V_{OH1}	Output H Voltage All outputs	2.15			V	I_{OH} = –200 µA
V_{OH2}	Output H PHI	V_{CC} –0.6			V	I_{OH}= –200 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.2 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			10	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{TL}	Tri-state Leakage Current			10	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{CC}*	Power Dissipation* (Normal Operation)		40	80	mA	f = 20 MHz
	Power Dissipation* (SLEEP)		TBD	TBD	mA	f= 20 MHz
	Power Dissipation* (I/O STOP)		TBD	TBD	mA	f= 20 MHz
	Power Dissipation* (SYSTEM STOP mode)		4	8	mA	f = 20 MHz
	IDLE Mode		TBD	TBD	mA	f = 20 MHz
	STANDBY Mode		50		µA	f = 0 MHz †
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:

These I_{CC} values are preliminary and subject to change without notice.

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
V_{CC} = 3.3V

† Device may take up to two seconds before stabilizing to steady state current.

General-Purpose I/O Port Timing

This figure shows the timing for the Ports A, B and C. Parameters referred to in this figure appear in Tables D and E.

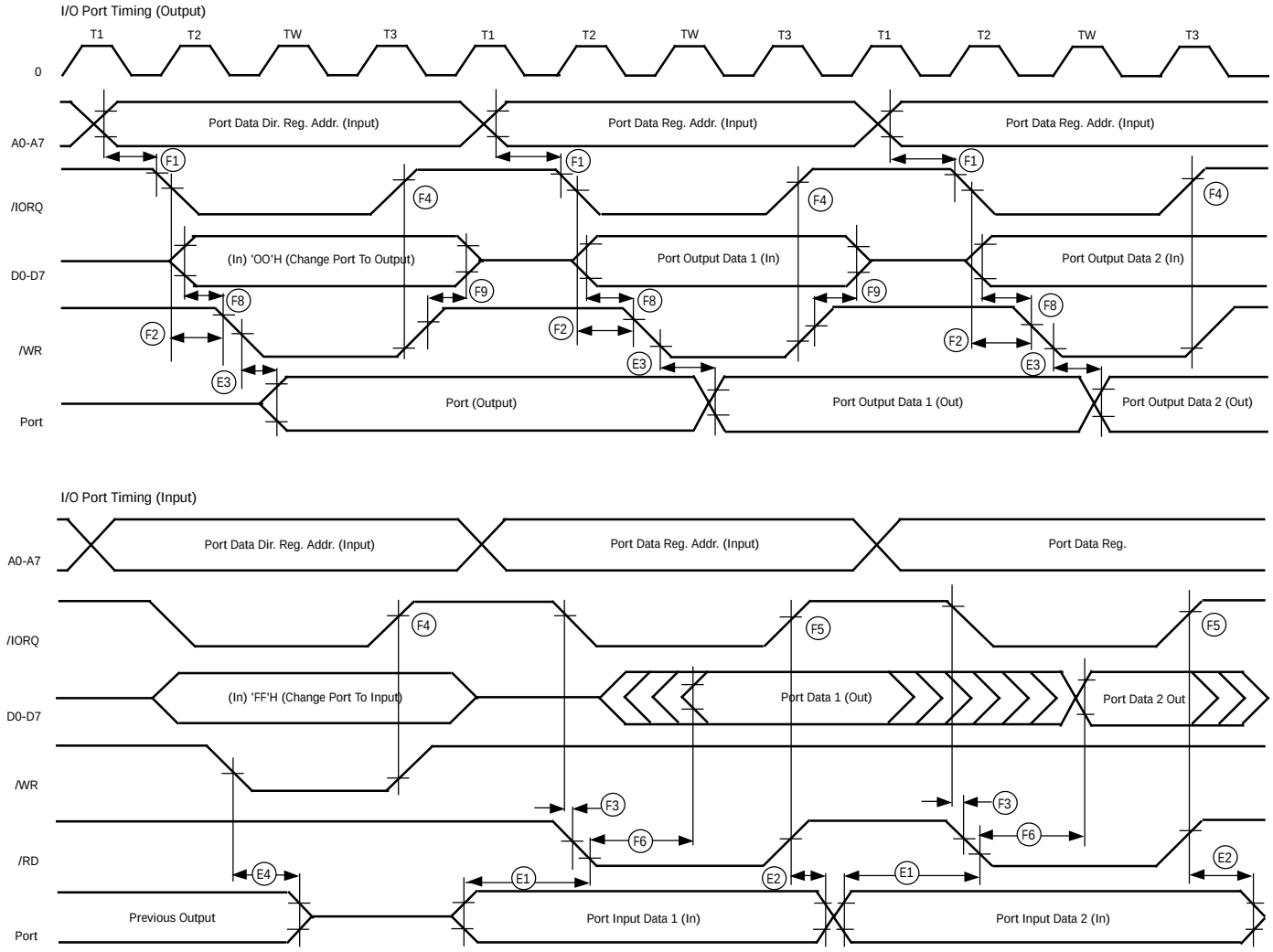


Figure 107. PORT Timing

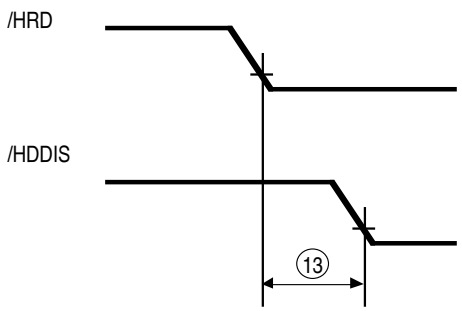


Figure 113. Driver Enable Timing

Table J. Driver Enable Timing

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
13	tRDD	/HRD to Driver Enable/Disable		60		60	ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

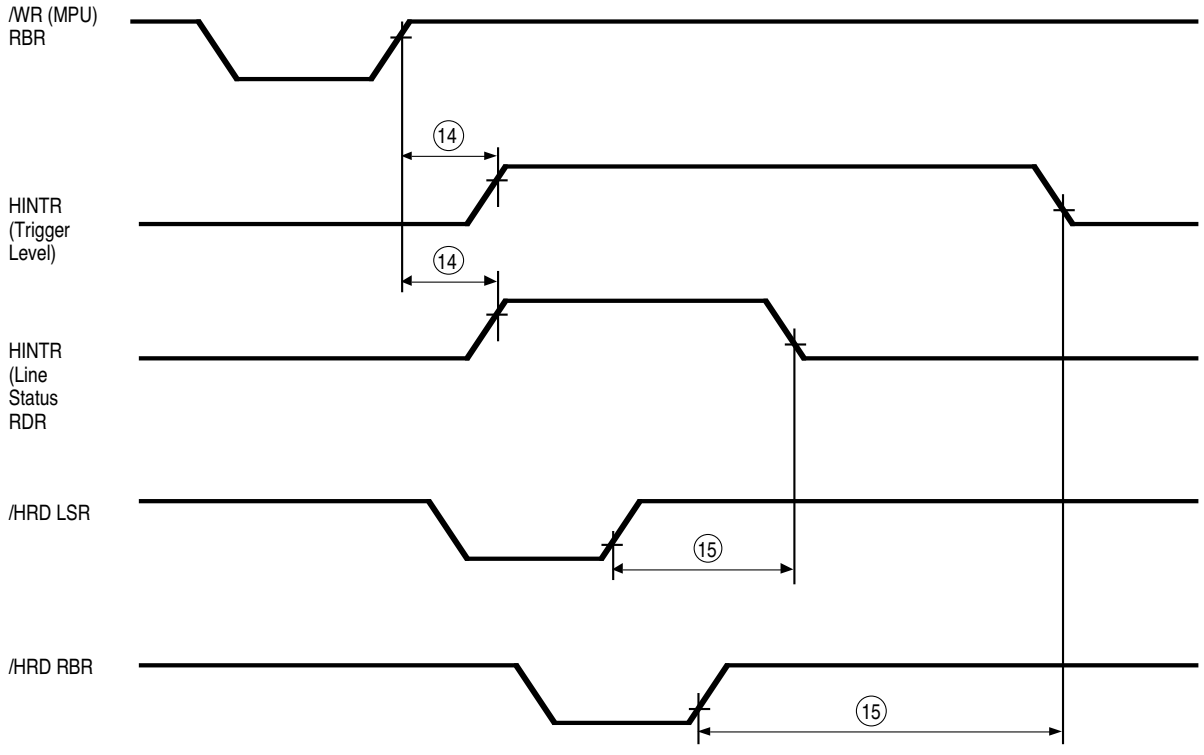


Figure 114. Interrupt Timing RCVR FIFO

16550 MIMIC TIMING (Continued)

Table K. Interrupt Timing RCVR FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
14	tSINT	Delay from Stop to Set Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles
15	tRINT	Delay from /HRD (RD RBR or RD LSR) to Reset Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles

Note:
These AC parameter values are preliminary and are subject to change without notice.

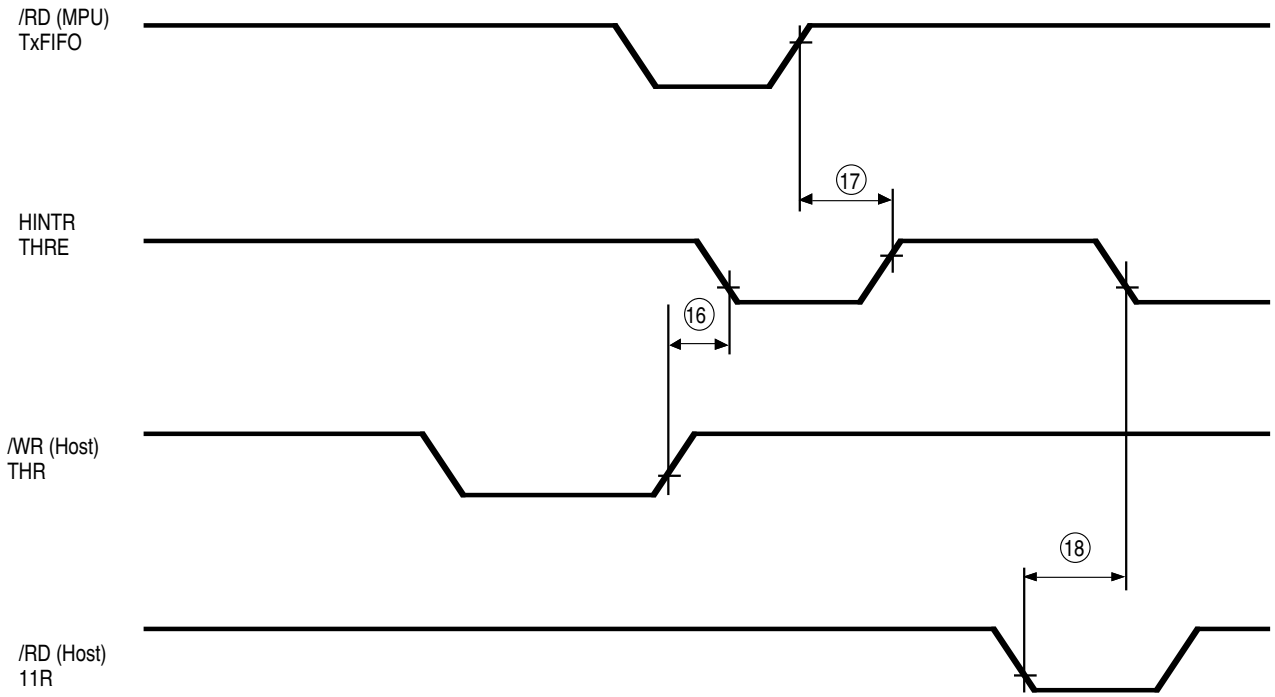


Figure 115. Interrupt Timing Transmitter FIFO

Table L. Interrupt Timing Transmitter FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
16	tHR	Delay from /WR (WR THR) to Reset Interrupt		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles
17	TSTI	Delay from Stop to Interrupt (THRE)	2 MPU Clock Cycles		2 MPU Clock Cycles	
18	TIR	Delay from /RD (RD IIR) to Reset Interrupt (THRIE)		75		75

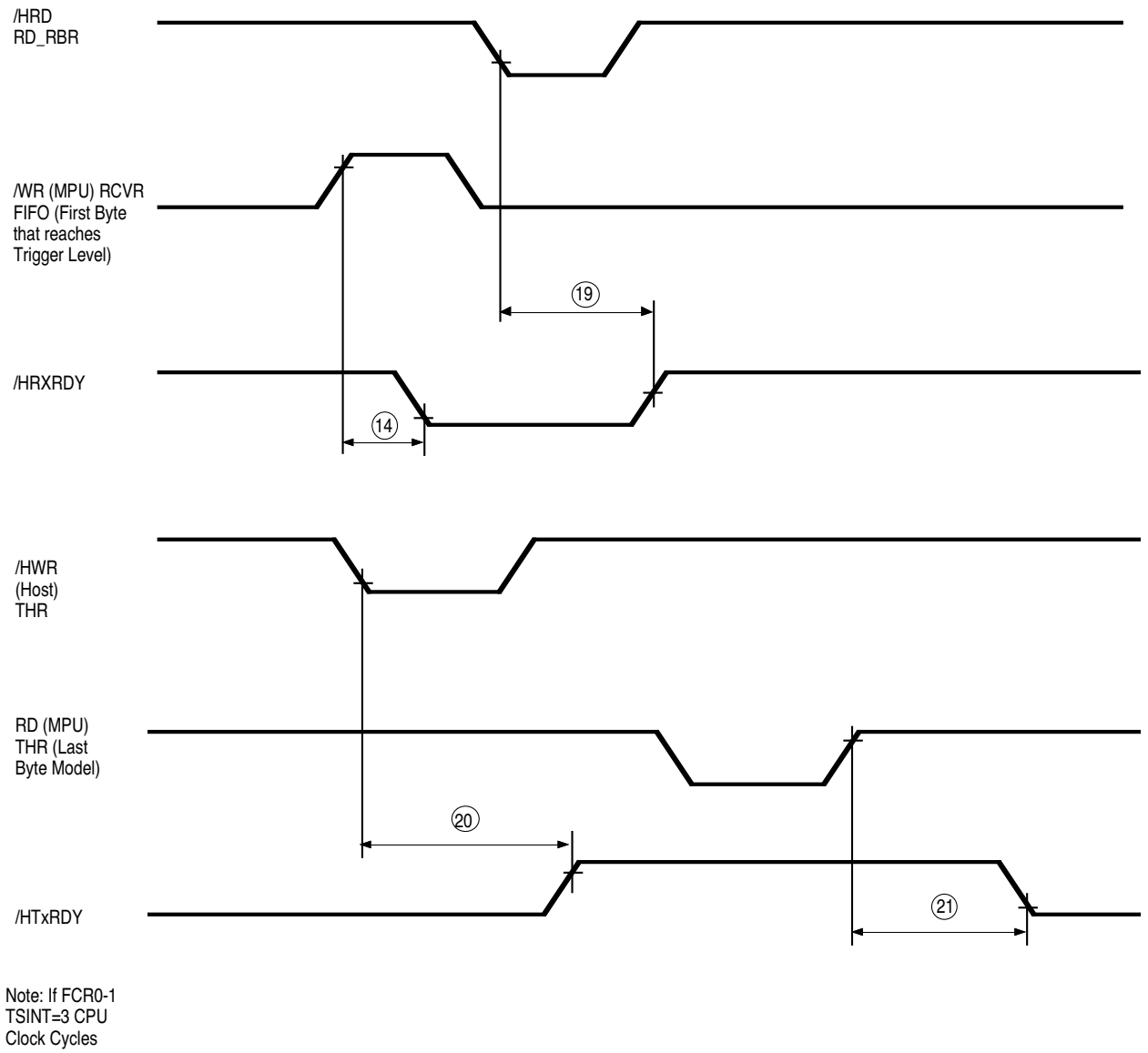


Figure 116 RCVR FIFO Bytes Other Than First