# Zilog - Z8018216FSG Datasheet

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | Z80180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 16MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 100-QFP |
| Supplier Device Package | 100-QFP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8018216fsg |

## MULTIPLEXED PIN DESCRIPTIONS

**A18/$T_{OUT.}$** During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, The $T_{OUT}$ function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/$T_{OUT}$. Therefore, the selection of $T_{OUT}$ will not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

**CKA0//DREQ0.** During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, /DREQ0 function is always selected.

**CKA1//TEND0.** During Reset, this pin is initialized as CKA1 pin. If CKA1D bit in the ASCI control register Ch1(CNTLA1) is set to 1, /TEND0 function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

**RxS//CTS1.** During Reset, this pin is initialized as the RxS pin. If CTS1E bit in the ASCI status register Ch1 (STAT1) is set to 1, /CTS1 function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 2 specifies. On Reset, both bits 1 and 2 are 0, so /TEND1,TxS,CKS are selected.

**Table 2. Triple Multiplexed Pins**

| Bit 1 | Bit 2 | Master Configuration Register |
|---|---|---|
| 0 | 0 | /TEND1,TxS,CKS |
| 0 | 1 | /RTSB,/DTR//REQB,/W//REQB |
| 1 | 0 | /TEND1,TxS,CKS |
| 1 | 1 | /HRxRDY,//HTxRDY,HINTR |

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is 0, then the Z80182/Z8L182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is 1, then Z80182/Z8L182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182/Z8L182 Mode 0 is always selected as shown in Table 3.

**Table 3. Mode 0 and Mode 1 Multiplexed Pins**

| Z80182/Z8L182 Mode 0 | Z80182/Z8L182 Mode 1 |
|---|---|
| TxDB | /HDDIS |
| RxDB | HA1 |
| /TRxCB | HA0 |
| /RTxCB | HA2 |
| /SYNCB | /HCS |
| /CTSB | /HWR |
| /DCDB | /HRD |
| PA7-PA0 | HD7-HD0 |

## Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

## TIMER DATA REGISTERS

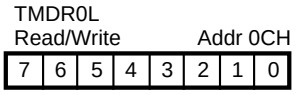



**Figure 23. Timer 0 Data Register L**

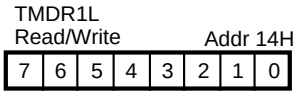
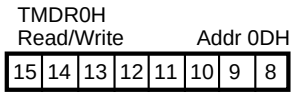
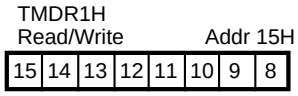



**Figure 24. Timer 1 Data Register L**




When Read, read Data Register L before reading Data Register H.

**Figure 25. Timer 0 Data Register H**




When Read, read Data Register L before reading Data Register H.

**Figure 26. Timer 1 Data Register H**

## TIMER RELOAD REGISTERS

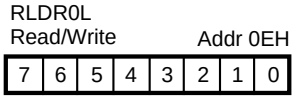



**Figure 27. Timer 0 Reload Register L**

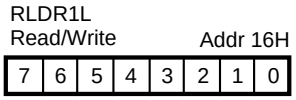



**Figure 28. Timer 1 Reload Register L**

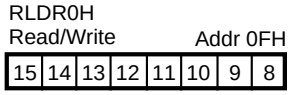



**Figure 29. Timer 0 Reload Register H**

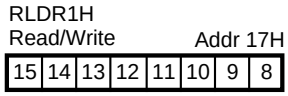
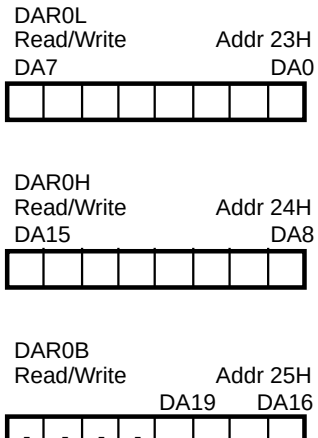



**Figure 30. Timer 1 Reload Register H**

## DMA REGISTERS




Bits 0-2 (3) are used for DAR0B

| A19, | A18, | A17, | A16 | DMA Transfer Request |
|---|---|---|---|---|
| x | x | 0 | 0 | /DREQ0 (external) |
| x | x | 0 | 1 | TDR0 (ASCI0) |
| x | x | 1 | 0 | TDR1 (ASCI1) |
| x | x | 1 | 1 | Not Used |

**Figure 35. DMA 0 Destination Address Registers**

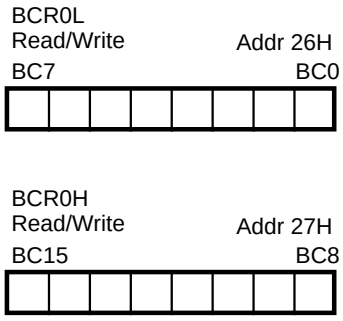



**Figure 36. DMA 0 Byte Counter Registers**

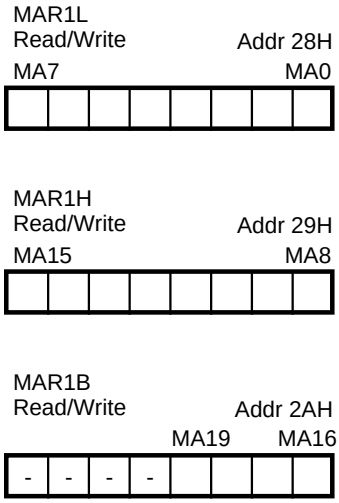



**Figure 37. DMA 1 Memory Address Registers**

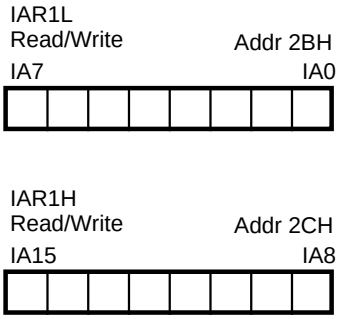



**Figure 38. DMA I/O Address Registers**

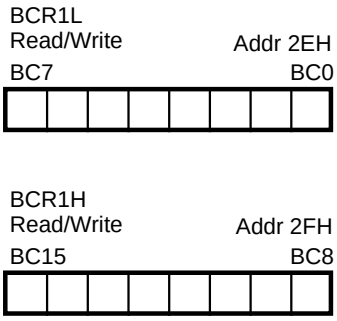



**Figure 39. DMA 1 Byte Count Registers**

## DMA REGISTERS (Continued)

DSTAT — Addr 30H

| Bit | DE1 | DE0 | /DWE1 | /DWE0 | DIE1 | DIE0 | - | DIME |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| R/W | R/W | R/W | W | W | R/W | R/W | | R |

- DIME: DMA Master Enable
- DIE1, DIE0: DMA Interrupt Enable 1, 0
- /DWE1, /DWE0: DMA Enable Bit Write Enable 1, 0
- DE1, DE0: DMA Enable Ch 1, 0

**Figure 40. DMA Status Register**

DMODE — Addr 31H

| Bit | - | - | DM1 | DM0 | SM1 | SM0 | MMOD | - |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| R/W | | | R/W | R/W | R/W | R/W | R/W | |

- MMOD: Memory MODE Select
- SM1, SM0: Ch 0 Source Mode 1, 0
- DM1, DM0: Ch 0 Destination Mode 1, 0

| DM1, 0 | Destination | Address |
|---|---|---|
| 00 | M | DAR0+1 |
| 01 | M | DAR0-1 |
| 10 | M | DAR0 Fixed |
| 11 | I/O | DAR0 Fixed |

| SM1, 0 | Source | Address |
|---|---|---|
| 00 | M | SAR0+1 |
| 01 | M | SAR0-1 |
| 10 | M | SAR0 Fixed |
| 11 | I/O | SAR0 Fixed |

| MMOD | Mode |
|---|---|
| 0 | Cycle Steal Mode |
| 1 | Burst Mode |

**Figure 41. DMA Mode Registers**

## SYSTEM CONTROL REGISTERS

IL — Addr 33H

| Bit | IL7 | IL6 | IL5 | - | - | - | - | - |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | | | | | |

Interrupt Vector Low

**Figure 46. Interrupt Vector Low Register**

ITC — Addr 34H

| Bit | TRAP | UFO | - | - | - | ITE2 | ITE1 | ITE0 |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| R/W | R/W | R | | | | R/W | R/W | R/W |

/INT Enable 2, 1, 0
Undefined Fetch Object
TRAP

**Figure 47. INT/TRAP Control Register**

RCR — Addr 36H

| Bit | REFE | REFW | - | - | - | - | CYC1 | CYC0 |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| R/W | R/W | R/W | | | | | R/W | R/W |

Cycle Select
Refresh Wait State
Refresh Enable

| CYC1, 0 | Interval of Refresh Cycle |
|---|---|
| 00 | 10 states |
| 01 | 20 states |
| 10 | 40 states |
| 11 | 80 states |

**Figure 48. Refresh Control Register**

## CONTROL REGISTERS (Continued)

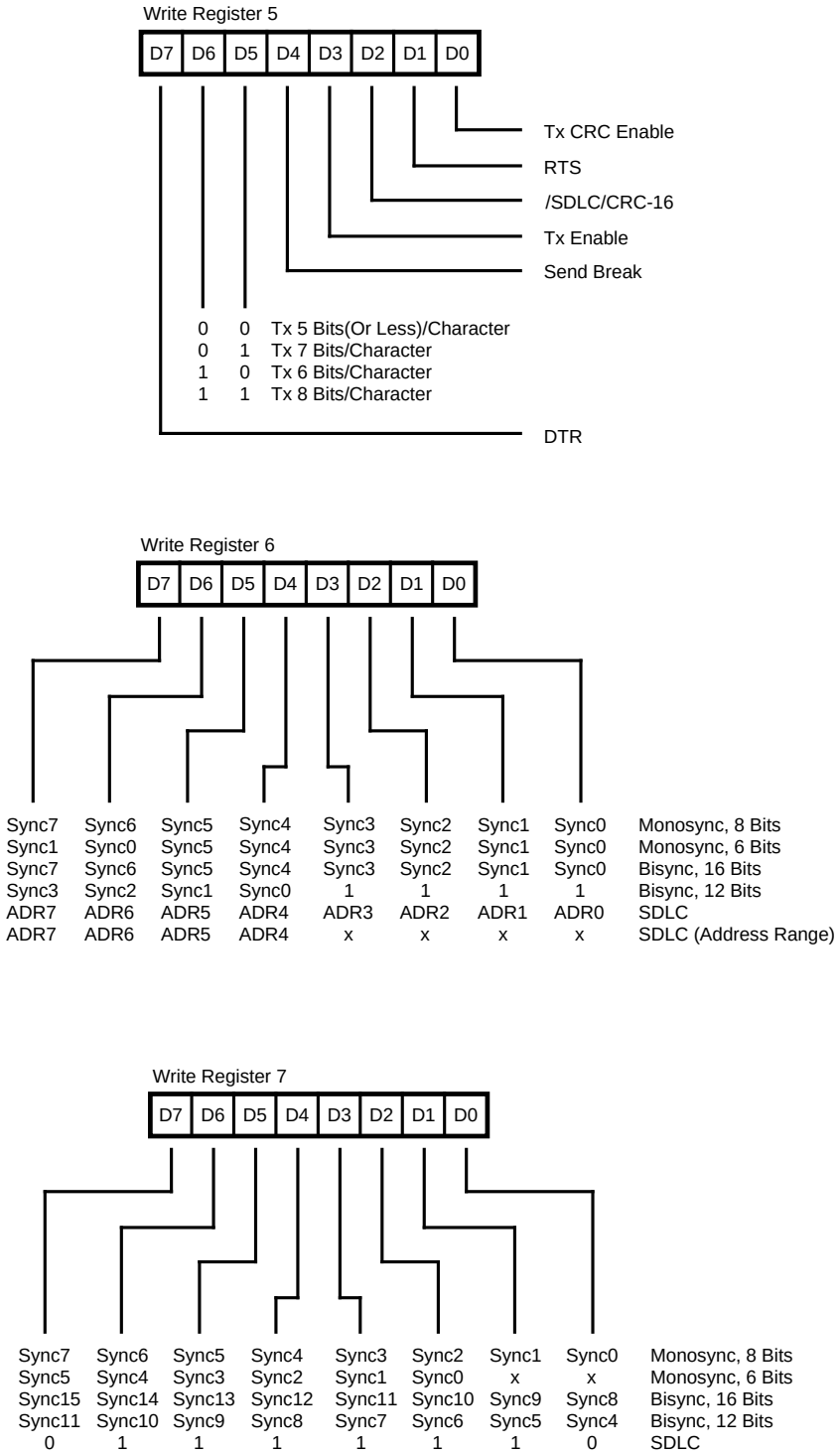



**Figure 52. Write Register Bit Functions** (Continued)

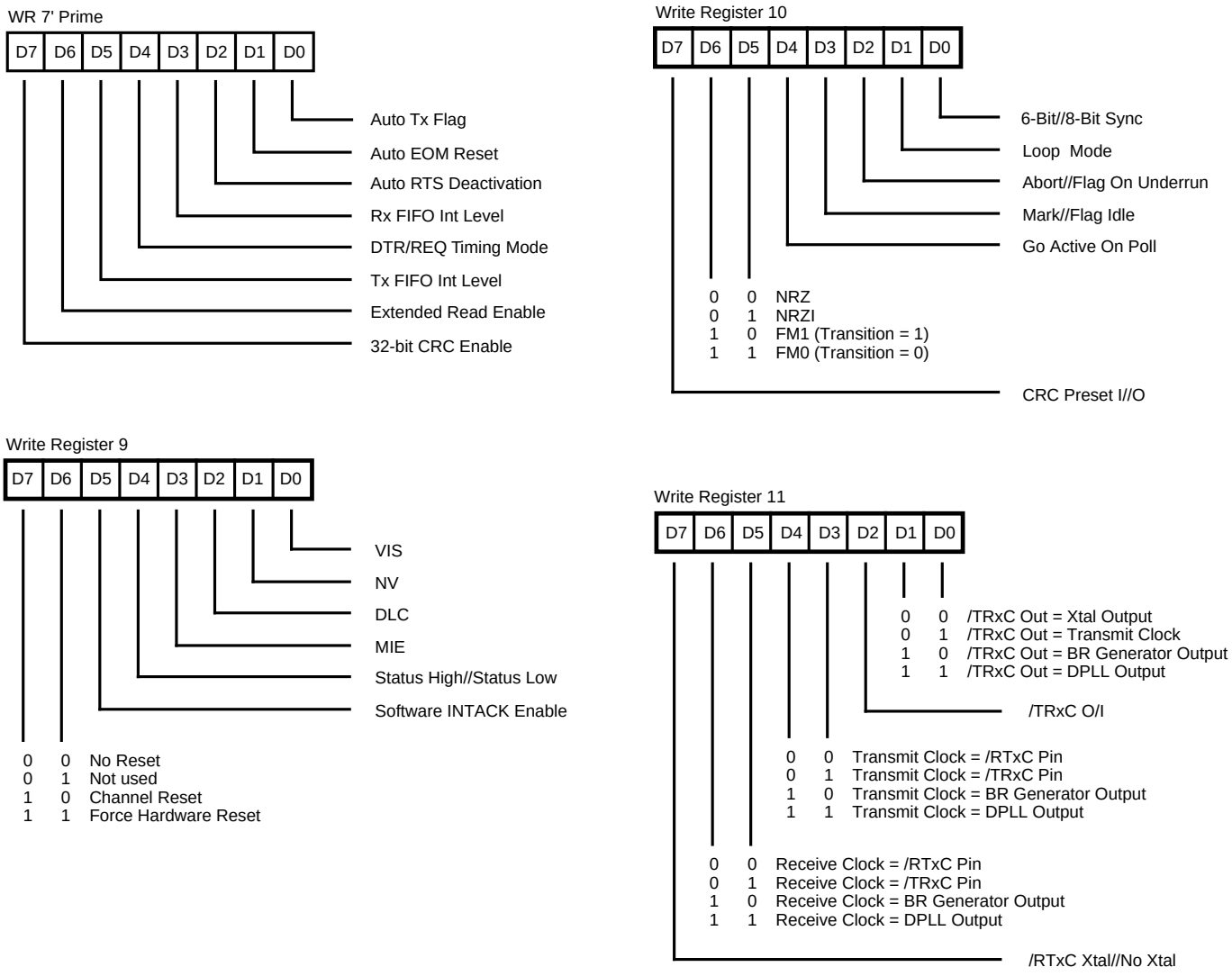



**Figure 52. Write Register Bit Functions** (Continued)

## CONTROL REGISTERS (Continued)

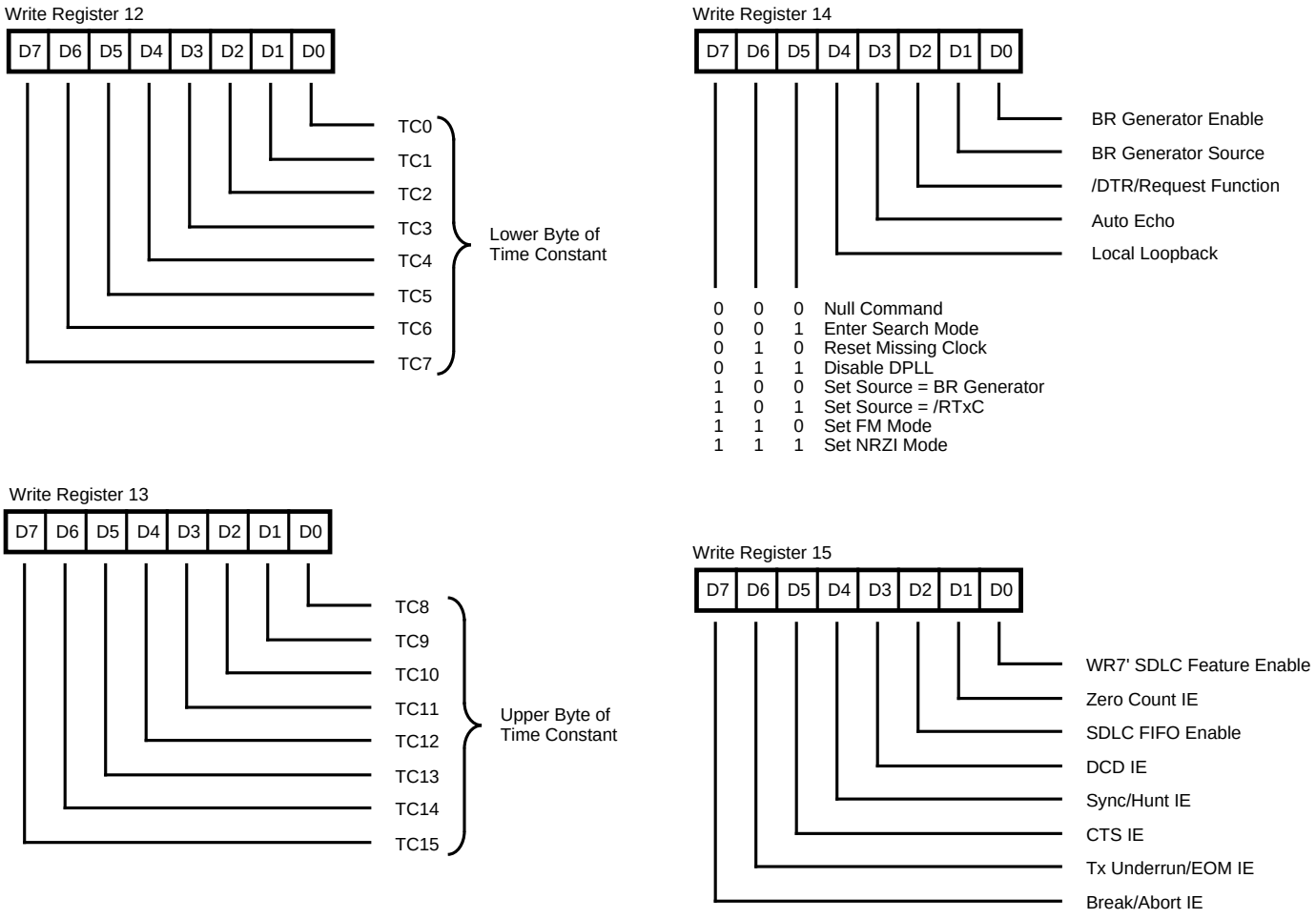



**Figure 52. Write Register Bit Functions** (Continued)

## Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Figures 54 through 65 describe miscellaneous registers that control the Z182 configuration, RAM/ROM chip select, interrupt and various status and timers.

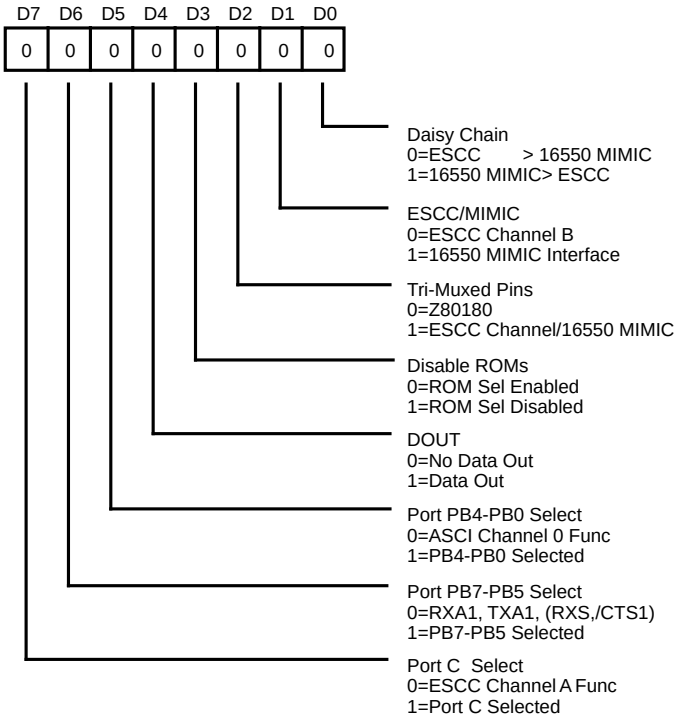



**Figure 54. System Configuration Register**
(Z180 MPU Read/Write, Address xxEFH)

### System Configuration Register

**Bit 7 Port C Select**
When this bit is set to 1, bit 8 parallel Port C is selected on the multiplexed pins. When this bit is reset to 0 then these multiplexed pins take ESCC™ Channel A functions.

**Bit 6 PB7-PB5 Select**
When this bit is set to 1, parallel Port B bits 7 through 5 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins become RxA1, TxA1 and RxS/CTS1.

**Bit 5 PB4-PB0 Select**
When this bit is set to 1, parallel Port B bits 4 through 0 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins take ASCI channel 0 functions.

**Bit 4 $DD_{OUT}$ ROM Emulator Mode Enable**
When this bit is set to 1, the Z182 is in "ROM emulator mode". In this mode, bus direction for certain transaction periods are set to the opposite direction to export internal bus transactions outside the Z80182/Z8L182. This allows the use of ROM emulators/logic analyzers for application development (see Tables 12a and 12b).

**Note:** The word "Out" means that the Z182 data bus direction is in output mode, "In" means input mode, and "Z" means high impedance. $DD_{OUT}$ stands for Data Direction Out and is the status of the D4 bit in the System Configuration Register (SCR).

**Table 12a. Data Bus Direction** (Z182 Bus Master)

**I/O And Memory Transactions**

| | I/O Write to On-Chip Peripherals | I/O Read From On-Chip Peripherals | I/O Write to Off-Chip Peripherals | I/O Read From Off-Chip Peripherals | Write To Memory | Read From Mode | Refresh | Z80182 /Z8L182 Idle Mode |
|---|---|---|---|---|---|---|---|---|
| Z80182 /Z8L182 Data Bus ($DD_{OUT}$ =0) | Out | Z | Out | In | Out | In | Z | Z |
| Z80182 /Z8L182 Data Bus ($DD_{OUT}$ =1) | Out | Out | Out | In | Out | In | Z | Z |

## 16550 MIMIC REGISTERS (Continued)

### FIFO Control Register

**Bit 6 and Bit 7 RCVR trigger LSB and MSB bits**
This 2-bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs (see Table 18).

**Bit 4 and Bit 5**
Reserved for future use (PC side). Note: From the MPU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side will clear a previously set bit 4 or bit 5.

**Bit 3 DMA mode select**
Setting this bit to 1 will cause the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A 1 in this bit enables multi-byte DMA).

**Bit 2 XMIT FIFO Reset**
Setting this bit to 1 will cause the transmitter FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

**Bit 1 RCVR FIFO Reset**
Setting this bit to 1 will cause the receiver FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

**Bit 0 FIFO Enable**
The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be 1 when writing to the other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared. This feature can be forced in a disabled state by the MPU.

**Table 18. Receive Trigger Level**

| b7 | b6 | Trigger Level, Number of Bytes |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 4 |
| 1 | 0 | 8 |
| 1 | 1 | 14 |

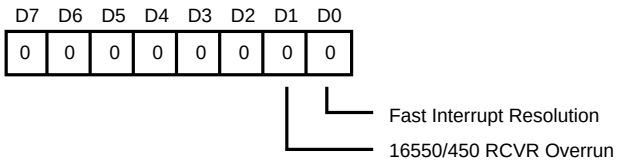



**Figure 72. MIMIC Modification Register**
(Z180 MPU Write only, Address xxE9h)

**Bit 7-2 Reserved.** Program to zero.

**Bit 1 RCVR Overrun Modification**
The actual 16450/16550 device allows the last position in FIFO to be overwritten by DCE during receiver overrun condition. When this bit is enabled (programmed to 1) the last position in FIFO can be overwritten by Z180 during receiver overrun. This feature is disabled by default. When this modification is not enabled, the MIMIC will ignore any write to RBR during an overrun condition.

**Bit 0 Fast MIMIC-ESCC Interrupt Resolution**
When enabling this modification, the internal MIMIC IEO signal into the ESCC IEI input is forced Low when the MIMIC Interrupt line becomes active. This is required to prevent the ESCC from putting it's vector on the databus during an INTACK cycle (given that the MIMIC is programmed to have higher interrupt priority).

When disabled, the internal MIMIC IEO becomes deasserted only after an interrupt acknowledge cycle. In this case, it is possible for the ESCC to force it's interrupt vector onto the data bus even when the MIMIC has a pending interrupt and is higher in priority.

## 16550 MIMIC REGISTERS (Continued)

### Modem Status Register

**Bit 7 Data Carrier Detect**
This bit must be written by the Z180 MPU.

**Bit 6 Ring Indicator**
This bit must be written by the Z180 MPU.

**Bit 5 Data Set Ready**
This bit must be written by the Z180 MPU.

**Bit 4 Clear to Send**
This bit must be written by the Z180™ MPU.

**Bit 3 Delta Data Carrier Detect**
This bit is set to 1 whenever the Data Carrier Detect bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

**Bit 2 Trailing Edge Ring Indicator**
This bit is set to 1 on the falling edge of the Ring Indicator bit. This bit is reset when the PC/XT/AT reads the Modem Status Register.

**Bit 1 Delta Data Set Ready**
This bit is set to 1 whenever the Data Set Ready bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

**Bit 0 Delta Clear To Send**
This bit is set to 1 whenever the Clear To Send bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

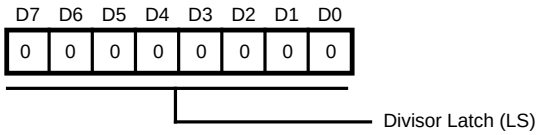



**Figure 79. Scratch Register**
(PC Read/Write, Address 07H)
(Z180 MPU Read Only, Address xxF7H)

### Scratch Register

**Bits 7-0 Scratch Register**
This register is used by the PC/XT/AT programmer for temporary data storage. The Z180 MPU is able to read this register. If the PC/XT/AT writes to this register, no interrupt to the Z180 MPU is generated.

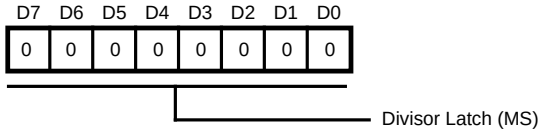



**Figure 80. Divisor Latch (LS)**
(PC Read/Write, Address 00H and DLAB=1)
(Z180 MPU Read Only, Address xxF8H)

### Divisor Latch (LS)

**Bit 7-0 Divisor Latch Most Significant Byte (MS)**
This register contains the Low order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT will generate an interrupt to the Z180 MPU. It can then read the Baud rate divisor and set up the application.

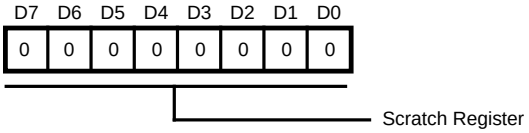



**Figure 81. Divisor Latch (MS)**
(PC Read/Write, Address 01H and DLAB=1)
(Z180 MPU Read Only, Address xxF9H)

### Divisor Latch (MS)

**Bit 7-0 Divisor Latch Most Significant Byte (MS)**
This register contains the High order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT will generate an interrupt to the Z180 MPU. It can then read the Baud rate divisor and set up the application.

## TIMING DIAGRAMS

Z180 MPU Timing

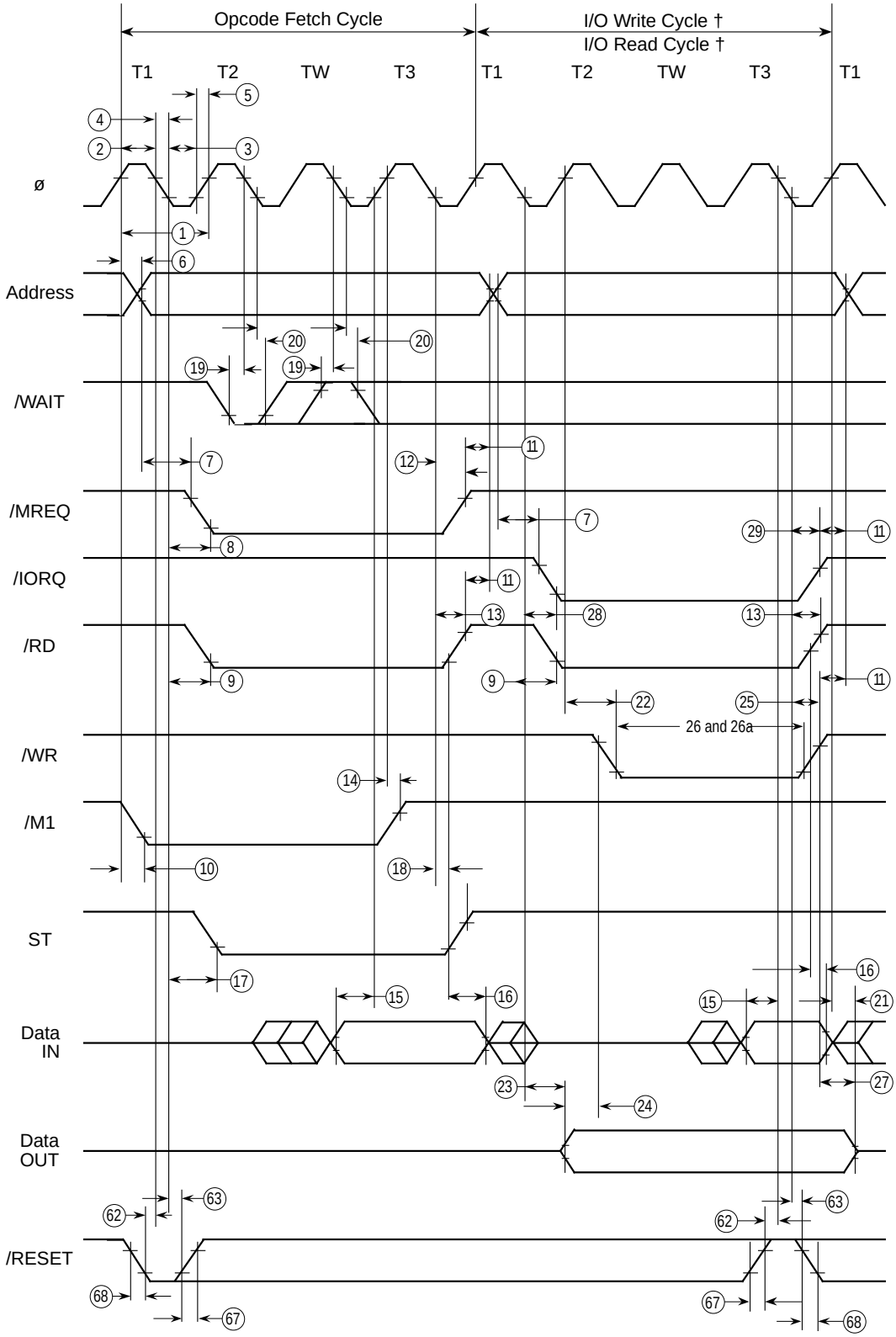



**Figure 90. CPU Timing**
(Opcode Fetch Cycle, Memory Read/Write Cycle
I/O Read/Write Cycle)

## TIMING DIAGRAMS (Continued)

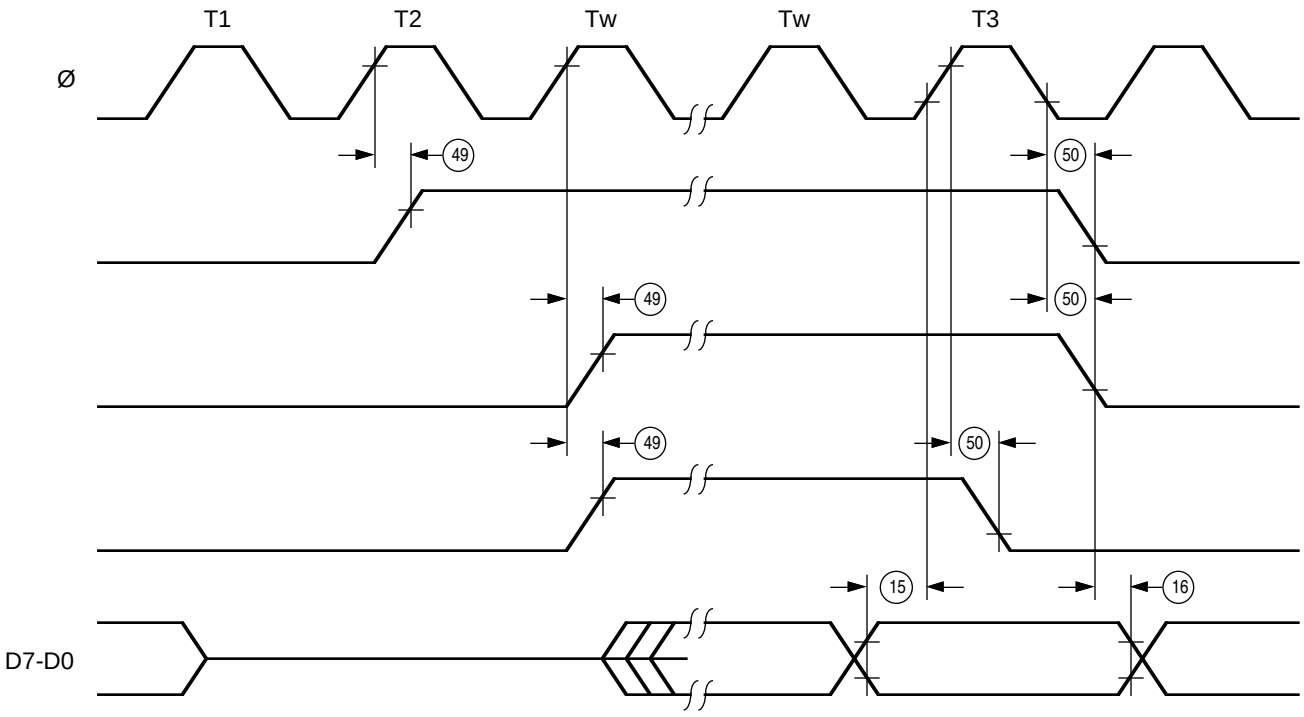



**Figure 94. E Clock Timing**
(Memory Read/Write Cycle
I/O Read/Write Cycle)

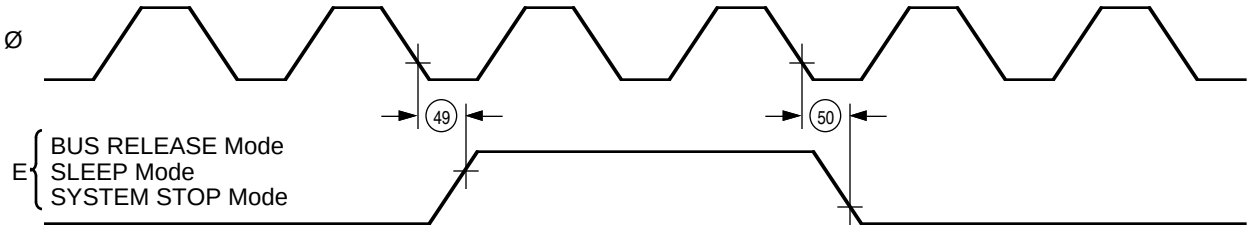



**Figure 95. E Clock Timing**

## ESCC Timing

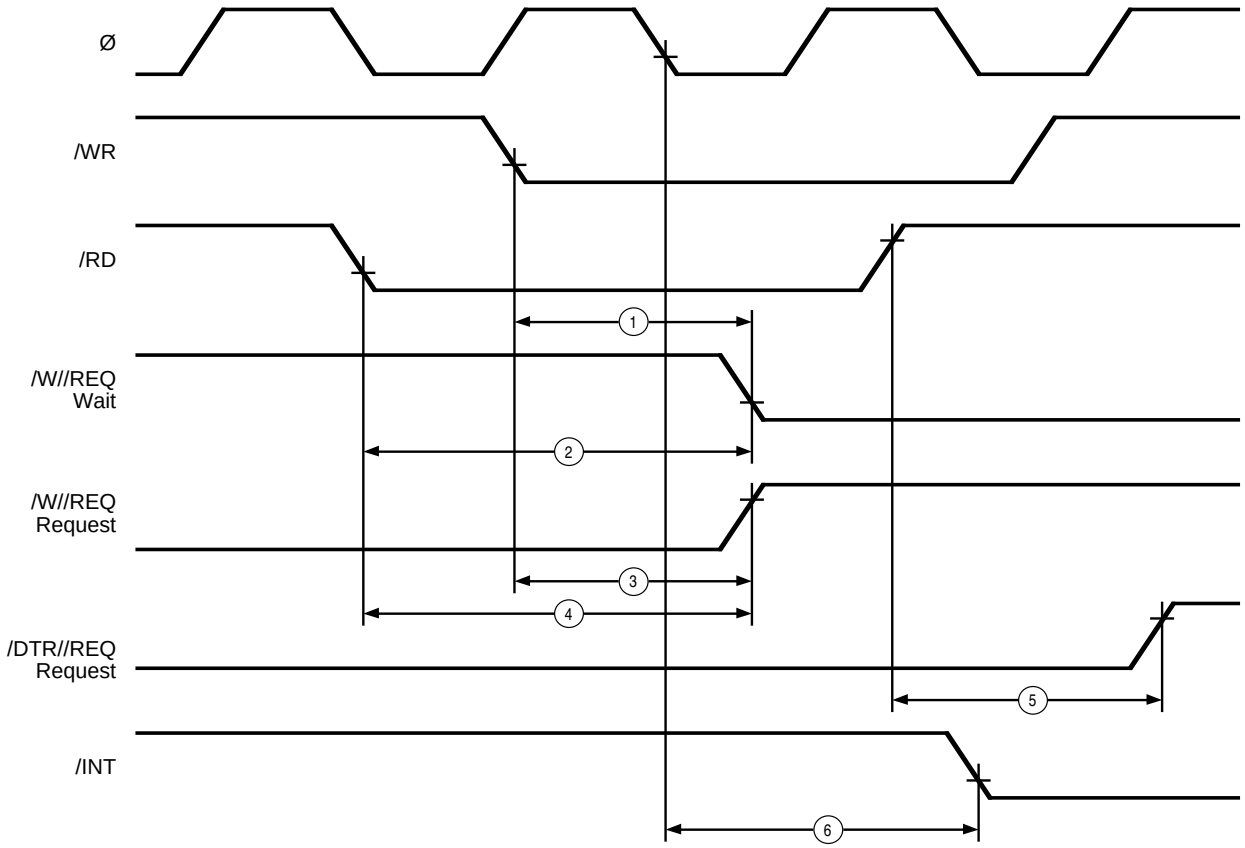



**Figure 104. ESCC AC Parameter**

**Table B. ESCC Timing Parameters**

| No. | Symbol | Parameter | 20 MHz Min | 20 MHz Max | Unit |
|---|---|---|---|---|---|
| 1 | TdWR(W) | /WR Fall to Wait Valid Delay | | 50 | ns |
| 2 | TdRD(W) | /RD Fall to Wait Valid Delay | | 50 | |
| 3 | TdWRf(REQ) | /WR Fall to /W//REQ Not Valid Delay | | 65 | |
| 4 | TdRDf(REQ) | /RD Fall to /W//REQ Not Valid Delay | | 65 | |
| 5 | TdRdr(REQ) | /RD Rise to /DTR//REQ Not Valid Delay | | TBD | |
| 6 | TdPC(INT) | Clock to /INT Valid Delay | | 160 | |

## AC CHARACTERISTICS (Continued)

Z85230 General Timing Diagram

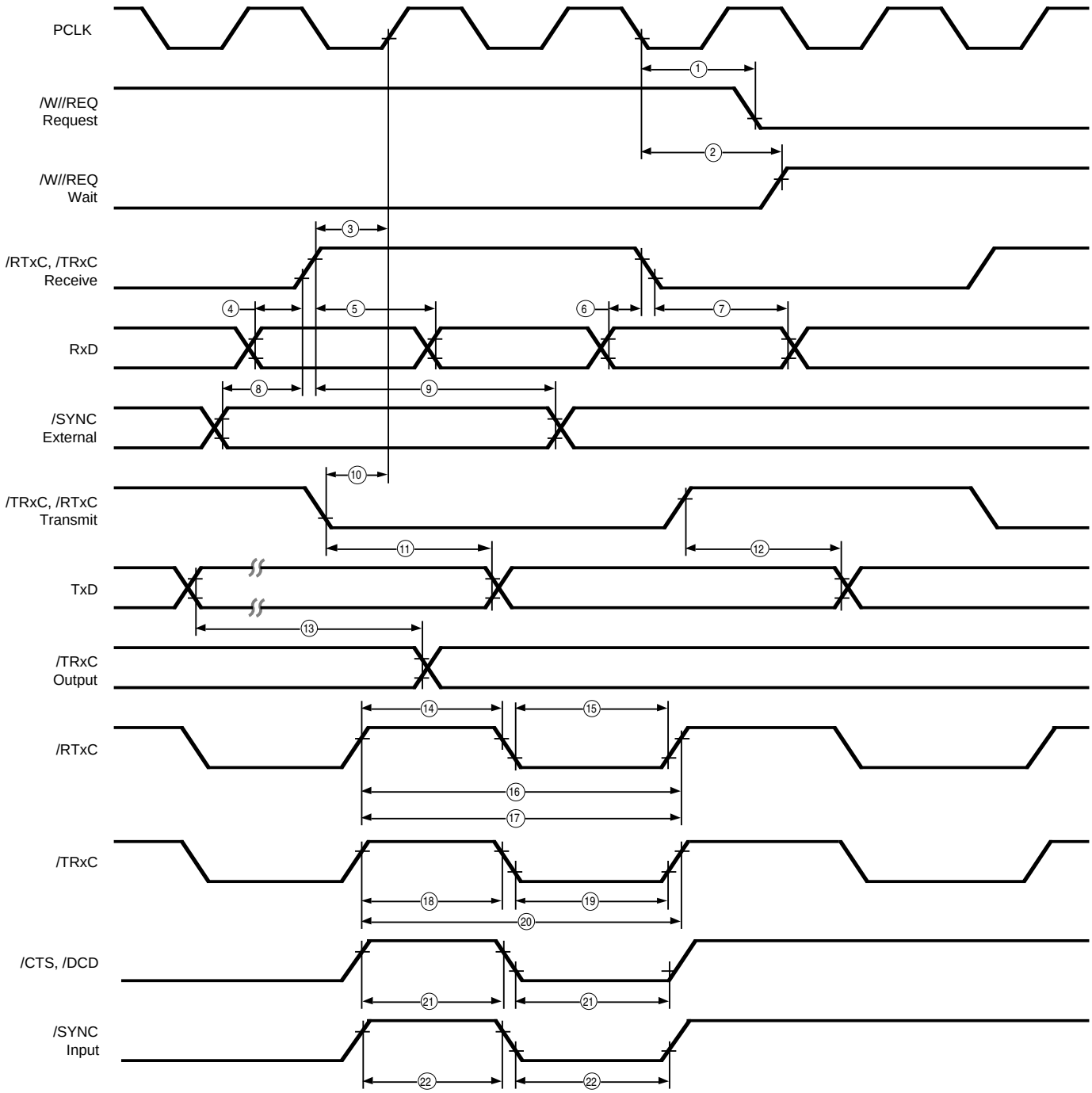



**Figure 105. General Timing Diagram**

## 16550 MIMIC TIMING (Continued)

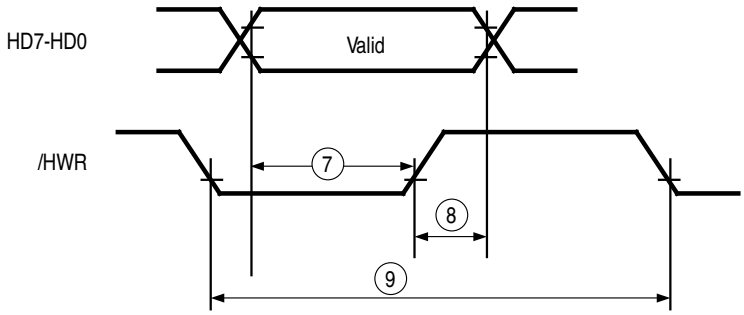



**Figure 111. Data Setup and Hold, Output Delay, Write Cycle**

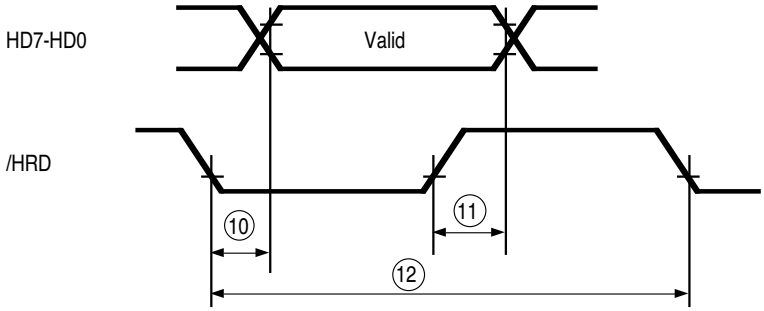



**Figure 112. Data Setup and Hold, Output Delay, Read Cycle**

**Table I. Data Setup and Hold, Output Delay, Read Cycle**

| | | | Z8L182 20 MHz | | Z80182 33 MHz | | |
|---|---|---|---|---|---|---|---|
| **No.** | **Sym** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Units** |
| 7 | tDs | Data Setup Time | 30 | | 30 | | ns |
| 8 | tDh | Data Hold Time | 30 | | 30 | | ns |
| 9 | tWc | Write Cycle Delay | 2.5 MPU Clock Cycles | | 2.5 MPU Clock Cycles | | ns |
| 10 | tRvD | Delay from /HRD to Data | | 125 | | 125 | ns |
| 11 | tHz | /HRD to Floating Delay | | 100 | | 100 | ns |
| 12 | tRc | Read Cycle Delay | 125 | | 125 | | ns |

**Note:**
These AC parameter values are preliminary and are subject to change without notice.

## 16550 MIMIC TIMING (Continued)

**Table K. Interrupt Timing RCVR FIFO**

| No. | Sym | Parameter | Z8L182 20 MHz Min | Z8L182 20 MHz Max | Z80182 33 MHz Min | Z80182 33 MHz Max |
|---|---|---|---|---|---|---|
| 14 | tSINT | Delay from Stop to Set Interrupt | | 2 MPU Clock Cycles | | 2 MPU Clock Cycles |
| 15 | tRINT | Delay from /HRD (RD RBR or RD LSR) to Reset Interrupt | | 2 MPU Clock Cycles | | 2 MPU Clock Cycles |

**Note:**
These AC parameter values are preliminary and are subject to change without notice.

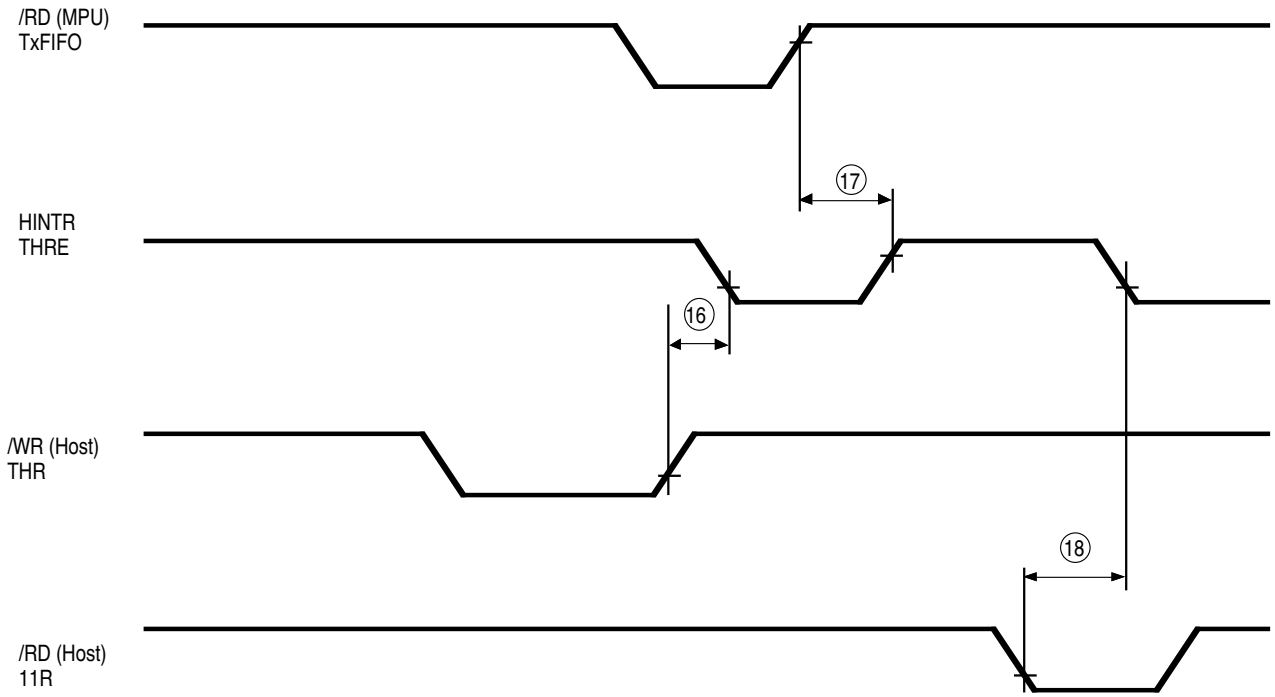
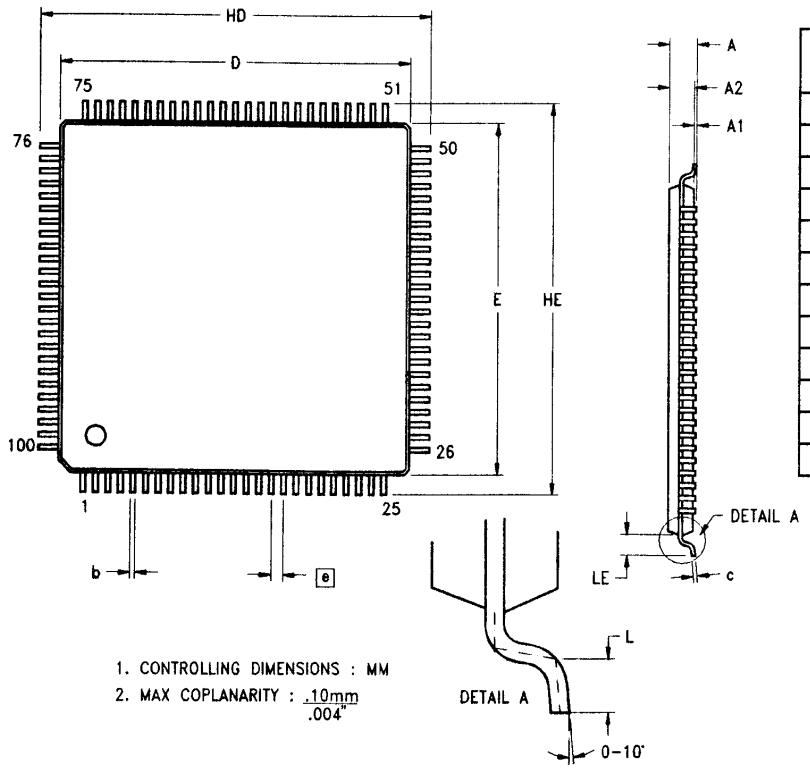



**Figure 115. Interrupt Timing Transmitter FIFO**

## PACKAGE INFORMATION




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.60 | .053 | .063 |
| A1 | 0.05 | 0.20 | .002 | .008 |
| A2 | 1.30 | 1.50 | .051 | .059 |
| b | 0.15 | 0.26 | .C06 | .010 |
| c | 0.10 | 0.20 | .004 | .008 |
| HD | 15.85 | 16.15 | .624 | .636 |
| D | 13.90 | 14.10 | .547 | .555 |
| HE | 15.85 | 16.15 | .624 | .636 |
| E | 13.90 | 14.10 | .547 | .555 |
| e | 0.50 TYP | | .0197 TYP | |
| L | 0.35 | 0.65 | .014 | .026 |
| LE | 0.90 | 1.10 | .035 | .043 |

**100-Pin VQFP Package Diagram**

## ORDERING INFORMATION

| Z8L182 | Z80182 |
|---|---|
| **20 MHz** | **33 MHz** |
| Z8L18220ASC | Z8018233ASC |
| Z8L18220FSC | Z8018233FSC |

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

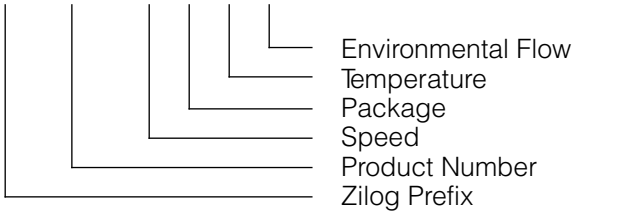
### Preferred Package
A = VQFP (Very Small QFP)
F = Plastic Quad Flatpack

### Preferred Temperature
S = 0°C to +70°C

### Speeds
20 = 20 MHz
33 = 33 MHZ

### Environmental
C = Plastic Standard
D = Plastic Stressed
E = Hermetric Standard

### Example:
**Z 80182 20 F S C** is a Z80182, 20 MHz, QFP, 0°C to +70°C, Plastic Standard Flow



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