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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018233asc

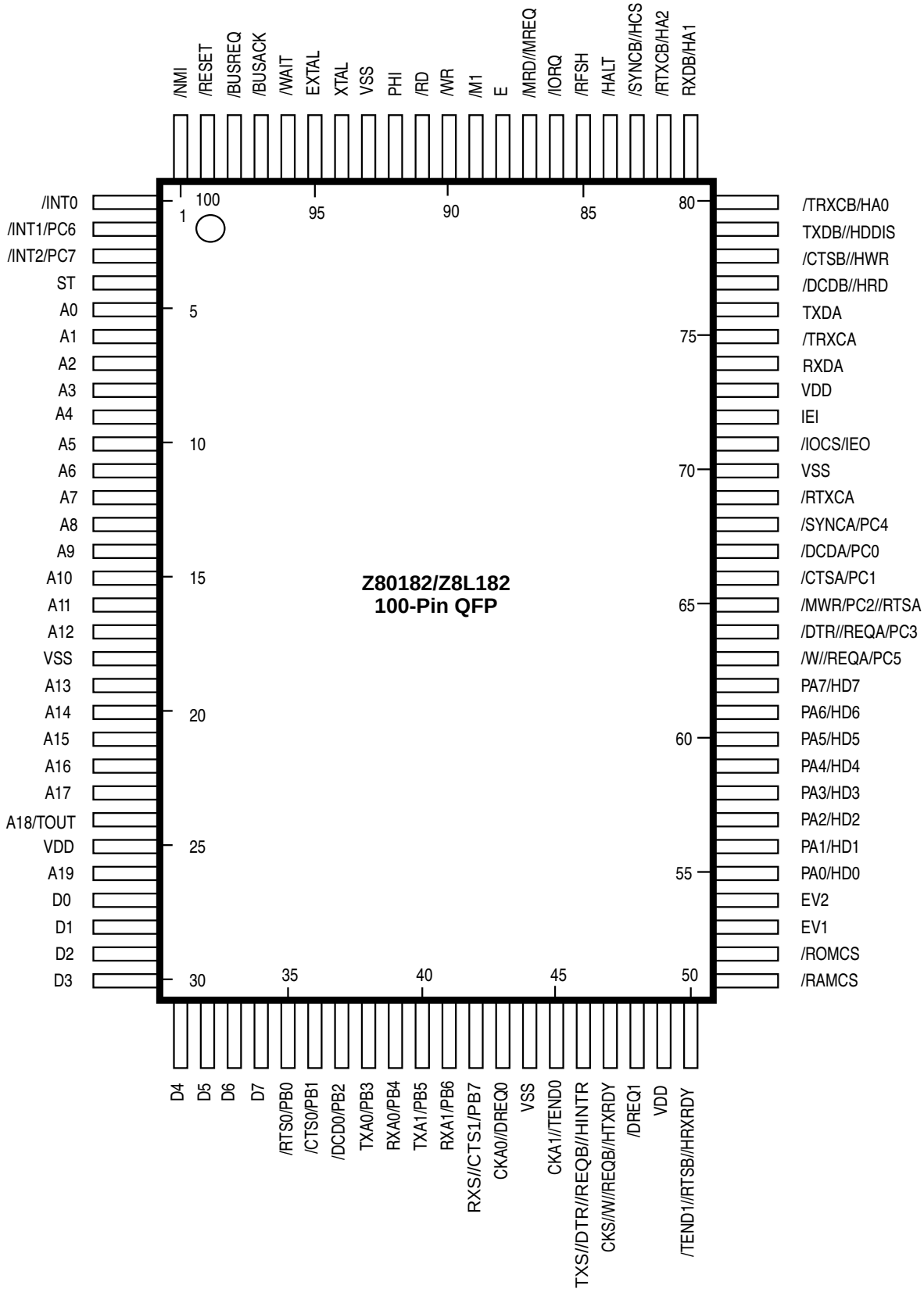


Figure 2. Z80182/Z8L182 100-Pin QFP Pin Configuration

Z180 CPU SIGNALS

A19-A0. *Address Bus (input/output, active High, tri-state).* A19-A0 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges up to 1 Mbyte, and I/O data bus exchanges up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states. This bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset).

D7-D0. *Data Bus (bi-directional, active High, tri-state).* D7-D0 constitute an 8-bit bi-directional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

/RD. *Read (input/output, active Low, tri-state).* /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

/WR. *Write (input/output, active Low, tri-state).* /WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

/IORQ. *I/O Request (input/output, active Low, tri-state).* /IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. /IORQ is also generated, along with /M1, during the acknowledgment of the /INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

/M1. *Machine Cycle 1 (input/output, active Low).* Together with /MREQ, /M1 indicates that the current cycle is the opcode fetch cycle of an instruction execution; unless /M1E bit in the OMCR is cleared to 0. Together with /IORQ, /M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the /HALT and ST signals to decode status of the CPU machine cycle. This signal is analogous to the /LIR signal of the Z64180.

/MREQ. *Memory Request (input/output, active Low, tri-state).* /MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the /ME signal of the Z64180. /MREQ is multiplexed with /MRD on the /MRD//MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if the /MREQ function is selected; and is inactive High if /MRD function is selected.

/MRD. *Memory Read (input/output, active Low, tri-state).* /MRD is active when both the internal /MREQ and /RD are active. /MRD is multiplexed with /MREQ on the /MRD //MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if /MREQ function is selected; and is inactive High if /MRD function is selected. The default function on power up is /MRD and may be changed by programming bit 3 of the Interrupt Edge/Pin MUX Register (xxDFH).

/MWR. *Memory Write (input/output, active Low, tri-state).* /MWR is active when both the internal /MREQ and /WR are active. This /RTSA or PC2 combination is pin multiplexed with /MWR on the /MWR/PC2//RTSA pin. The default function of this pin on power up is /MWR, which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/WAIT. *(input/output active Low).* /WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The /WAIT input is sampled on the falling edge of T2 (and subsequent wait states). If the input is sampled Low, then additional wait states are inserted until the /WAIT input is sampled High, at which time execution will continue.

/HALT. *Halt/Sleep Status (input/output, active Low).* This output is asserted after the CPU has executed either the HALT or SLEEP instruction, and is waiting for either non-maskable or maskable interrupts before operation can resume. It is also used with the /M1 and ST signals to decode status of the CPU machine cycle. On exit of HALT/SLEEP mode, the first instruction fetch can be delayed by 16 clock cycles after the /HALT pin goes High, if HALT 16 feature is selected.

/BUSACK. *Bus Acknowledge (input/output, active Low).* /BUSACK indicates to the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

/BUSREQ. *Bus Request (input, active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address/data buses and other control signals, into the high impedance state.

EMULATION SIGNALS

EV1, EV2. *Emulation Select (input).* These two pins determine the emulation mode of the Z180 MPU (Table 1).

Table 1. Evaluation Modes

Mode	EV2	EV1	Description
0	0	0	Normal mode, on-chip Z180 bus master
1	0	1	Emulation Adapter Mode
2	1	0	Emulator Probe Mode
3	1	1	Reserved for Test

SYSTEM CONTROL SIGNALS

ST. *Status (output, active High).* This signal is used with the /M1 and /HALT output to decode the status of the CPU machine cycle. If unused, this pin should be pulled to V_{DD}.

/RESET. *Reset Signal (input, active Low).* /RESET signal is used for initializing the MPU and other devices in the system. It must be kept in the active state for a period of at least three system clock cycles.

IEI. *Interrupt Enable Signal (input, active High).* IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.

IEO. *Interrupt Enable Output Signal (output, active High).* In the daisy-chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is 1 and the CPU is not servicing an interrupt from the on-chip peripherals. This pin is multiplexed with /IOCS on the /IOCS/IEO pin. The /IOCS function is the default on Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/IOCS. *Auxiliary Chip Select Output Signal (output, active Low).* This pin is multiplexed with /IEO on the /IOCS/IEO pin. /IOCS is an auxiliary chip select that decodes A7, A6, /IORQ, /M1 and effectively decodes the address space xx80H to xxBFH for I/O transactions. A15 through A8 are not decoded so that the chip select is active in all pages of I/O address space. The /IOCS function is the default on the /IOCS/IEO pin after Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/RAMCS. *RAM Chip Select (output, active Low).* Signal used to access RAM based upon the Address and the RAMLBR and RAMUBR registers and /MREQ.

/ROMCS. *ROM Chip Select (output, active Low).* Signal used to access ROM based upon the address and the ROMBR register and /MREQ.

E. *Enable Clock (output, active High).* Synchronous machine cycle clock output during bus transactions.

XTAL. *Crystal (input, active High).* Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

EXTAL. *External Clock/Crystal (input, active High).* Crystal oscillator connections to an external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

PHI. *System Clock (output, active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is reflective of the functional speed of the processor. In clock divide-by-two mode, the pHI frequency is half that of the crystal or input clock. If divide-by-one mode is enabled, the PHI frequency is equivalent to that of crystal or input frequency. The PHI frequency is also fed to the ESCC core. If running over 20 MHz (5V) or 10 MHz (3V) the PHI-ESCC frequency divider should be enabled to divide the PHI clock by two prior to feeding into the ESCC core.

Table 5. Primary, Secondary and Tertiary Pin Functions

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
1	4	ST			
2	5	A0			
3	6	A1			
4	7	A2			
5	8	A3			
6	9	A4			
7	10	A5			
8	11	A6			
9	12	A7			
10	13	A8			
11	14	A9			
12	15	A10			
13	16	A11			
14	17	A12			
15	18	V_{SS}			
16	19	A13			
17	20	A14			
18	21	A15			
19	22	A16			
20	23	A17			
21	24	A18/T_{OUT}			
22	25	V_{DD}			
23	26	A19			
24	27	D0			
25	28	D1			
26	29	D2			
27	30	D3			
28	31	D4			
29	32	D5			
30	33	D6			
31	34	D7			
32	35	/RTS0	PB0		SYS CONF REG Bit 5
33	36	/CTS0	PB1		SYS CONF REG Bit 5
34	37	/DCD0	PB2		SYS CONF REG Bit 5
35	38	TxA0	PB3		SYS CONF REG Bit 5
36	39	RxA0	PB4		SYS CONF REG Bit 5
37	40	TxA1	PB5		SYS CONF REG Bit 6
38	41	RxA1	PB6		SYS CONF REG Bit 6
39	42	RxS//CTS1	PB7		SYS CONF REG Bit 6
40	43	CKA0//DREQ0			

Z182 CPU

The Z182 CPU is 100% software compatible with the Z80® CPU and has the following additional features:

Faster Execution Speed. The Z182 CPU is "fine tuned," making execution speed, on average, 10% to 20% faster than the Z80 CPU.

Enhanced DRAM Refresh Circuit. Z182 CPU's DRAM refresh circuit does periodic refresh and generates an 8-bit refresh address. It can be disabled or the refresh period adjusted, through software control.

Enhanced Instruction Set. The Z182 CPU has seven additional instructions to those of the Z80 CPU, which include the MLT (Multiply) instruction.

HALT and Low Power Modes of Operation. The Z182 CPU has HALT and Low Power modes of operation, which are ideal for the applications requiring low power consumption like battery operated portable terminals.

System Stop Mode. When the Z182 is in System Stop mode, it is only the Z180 MPU that is in STOP mode.

Standby and Idle Mode. Please refer to the Z8S180 Product Specification for additional information on these two additional Low Power modes.

Instruction Set. The instruction set of the Z182 CPU is identical to the Z180. For more details about each transaction, please refer to the Product Specification/ Technical Manual for the Z180/Z80 CPU.

Z182 CPU Basic Operation

Z182 CPU's basic operation consists of the following events. These are identical to the Z180 MPU. For more details about each operation, please refer to the Product Specification/Technical Manual for the Z180.

- Operation Code Fetch Cycle
- Memory Read/Write Operation
- Input/Output Operation
- Bus Request/Acknowledge Operation
- Maskable Interrupt Request Operation
- Trap and Non-Maskable Interrupt Request Operation
- HALT and Low Power Modes of Operation
- Reset Operation

Memory Management Unit (MMU)

The Memory Management Unit (MMU) allows the user to map the memory used by the CPU (64 Kbytes of logical addressing space) into 1 Mbyte of physical addressing space. The organization of the MMU allows object code compatibility with the Z80 CPU while offering access to an extended memory space. This is accomplished by using an effective common area-banked area scheme.

DMA Controller

The Z182 MPU has two DMA controllers. Each DMA controller provides high-speed data transfers between memory and I/O devices. Transfer operations supported are memory-to-memory, memory-to/from-I/O, and I/O-to-I/O. Transfer modes supported are request, burst, and cycle steal. The DMA can access the full 1 Mbytes addressing range with a block length up to 64 Kbytes and can cross over 64K boundaries.

Asynchronous Serial Communication Interface (ASCI)

This unit provides two individual full-duplex UARTs. Each channel includes a programmable baud rate generator and modem control signals. The ASCI channels also support a multiprocessor communication format.

Programmable Reload Timer (PRT)

The Z182 MPU has two separate Programmable Reload Timers, each containing a 16-bit counter (timer) and count reload register. The time base for the counters is system clock divided by 20. PRT channel 1 provides an optional output to allow for waveform generation.

Clocked Serial I/O (CSI/O)

The CSI/O channel provides a half-duplex serial transmitter and receiver. This channel can be used for simple high-speed data connection to another CPU or MPU.

Programmable Wait State Generator

To ease interfacing with slow memory and I/O devices, the Z182 MPU unit has a programmable wait state generator. By programming the DMA/WAIT Control Register (DCNTL), up to three wait states are automatically inserted in memory and I/O cycles. This unit also inserts wait states during on-chip DMA transactions. When using RAMCS and ROMCS wait state generators, the wait state controller with the most programmed wait states will determine the number of wait states inserted.

Z80182 MIMIC DOUBLE BUFFERING FOR THE TRANSMITTER

The Z80182 Rev DA implements double buffering for the transmitter in 16450 mode and sets the TEMT bit in the LSR Register automatically.

When this feature is enabled and character delay emulation is being used (see Figure 9):

1. The PC THRE bit in the LSR Register is set when the THR Register is empty;
2. PC Host writes to the 16450 THR Register;
3. Whenever the Z80182 TSR buffer is empty and one character delay timer is in a timed-out state, the byte from the THR Register is transferred to the TSR buffer; the timer is in timed-out state after FIFO Reset or after Host TEMT is set. This allows a dual write to THR when Host TEMT is set.
4. Restart character delay timer (timer reloads and counts down) with byte transfer from THR Register to the TSR buffer;
5. Whenever the TSR buffer is full, the TEMT bit in MPU LSR Register is reset with no delay;
6. MPU reads TSR buffer;
7. TEMT bit in LSR Register for MPU is set with no delay whenever the TSR buffer is empty;
8. When the TSR buffer is read by MPU and THR Register is empty and one character delay timer reaches zero, the TEMT bit in the LSR Register for Host is set from 0 to 1.

The PC THRE bit in the LSR Register is reset whenever the THR Register is full and set whenever THR Register is empty.

MPU IREQ and DMA Request for the transmit data is trigger whenever TSR buffer is full and cleared whenever TSR buffer is empty.

If character delay emulation is not used the TEMT bit in the LSR Register is set whenever both the THR Register and the TSR buffer are both empty. The Host TEMT bit is clear if there is data in either the TSR buffer of THR Register.

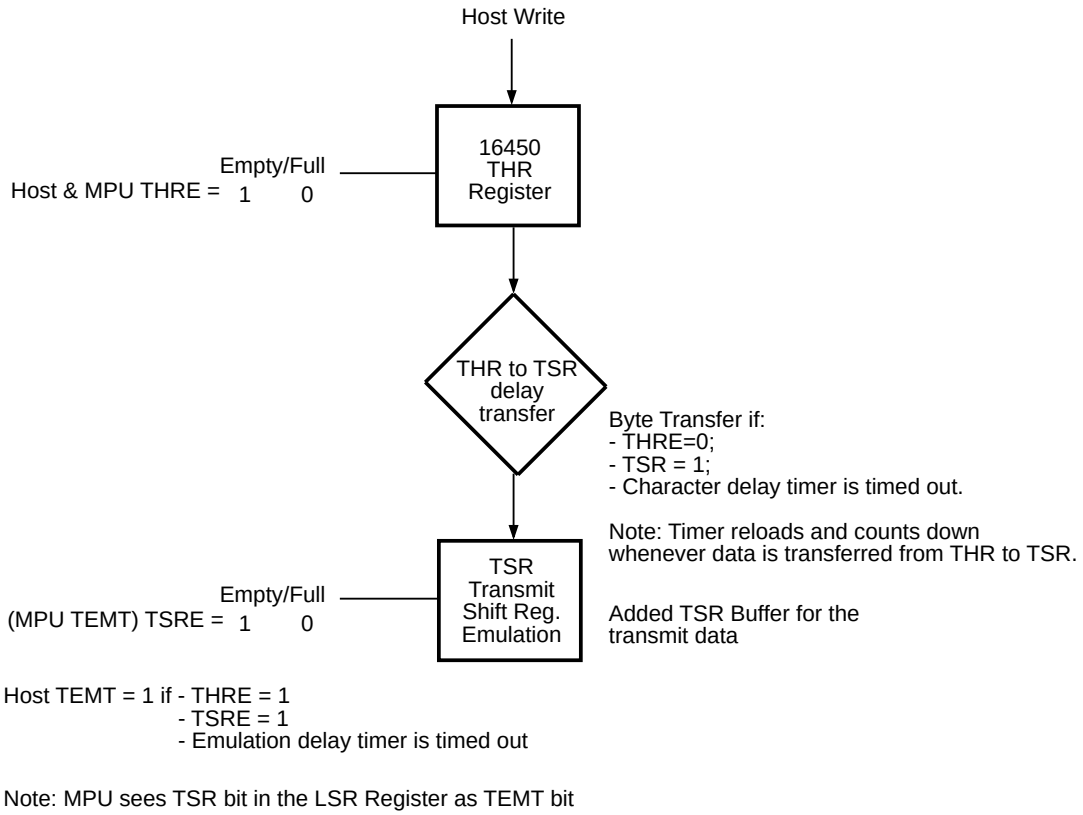


Figure 9. TEMT Emulation Logic Implementation

ASCI CHANNELS CONTROL REGISTERS (Continued)

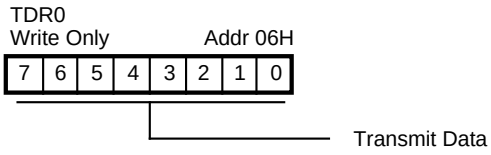


Figure 15. ASCI Transmit Data Register (Ch. 0)

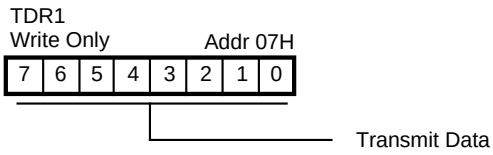


Figure 16. ASCI Transmit Data Register (Ch. 1)

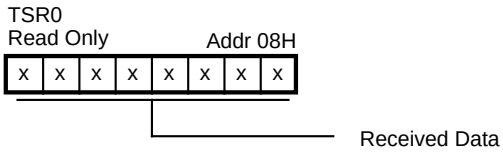


Figure 17. ASCI Receive Data Register (Ch. 0)

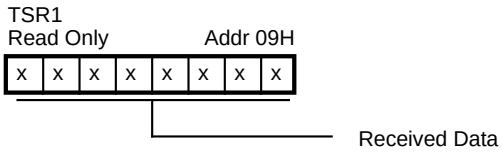


Figure 18. ASCI Receive Data Register (Ch. 1)

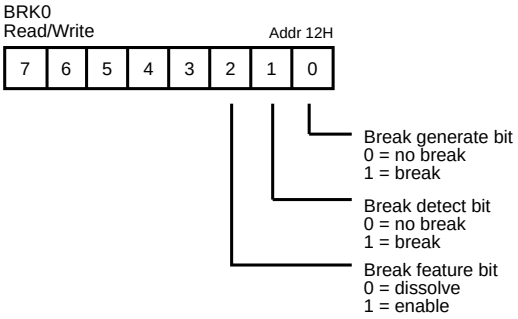


Figure 19. ASCI Break Control Register (Ch. 0)

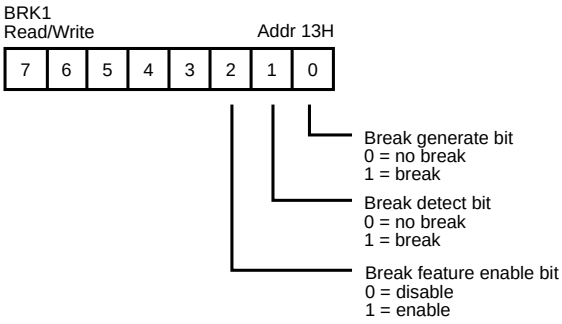


Figure 20. ASCI Break Control Register (Ch. 1)

TIMER DATA REGISTERS

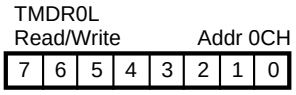


Figure 23. Timer 0 Data Register L

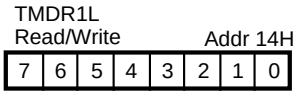
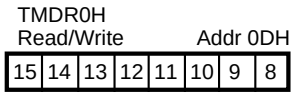
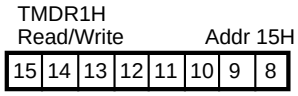


Figure 24. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 25. Timer 0 Data Register H



When Read, read Data Register L before reading Data Register H.

Figure 26. Timer 1 Data Register H

TIMER RELOAD REGISTERS

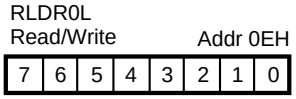


Figure 27. Timer 0 Reload Register L

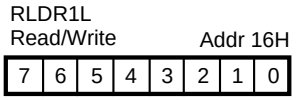


Figure 28. Timer 1 Reload Register L

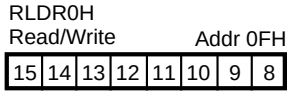


Figure 29. Timer 0 Reload Register H

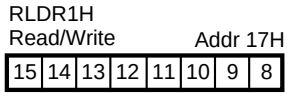
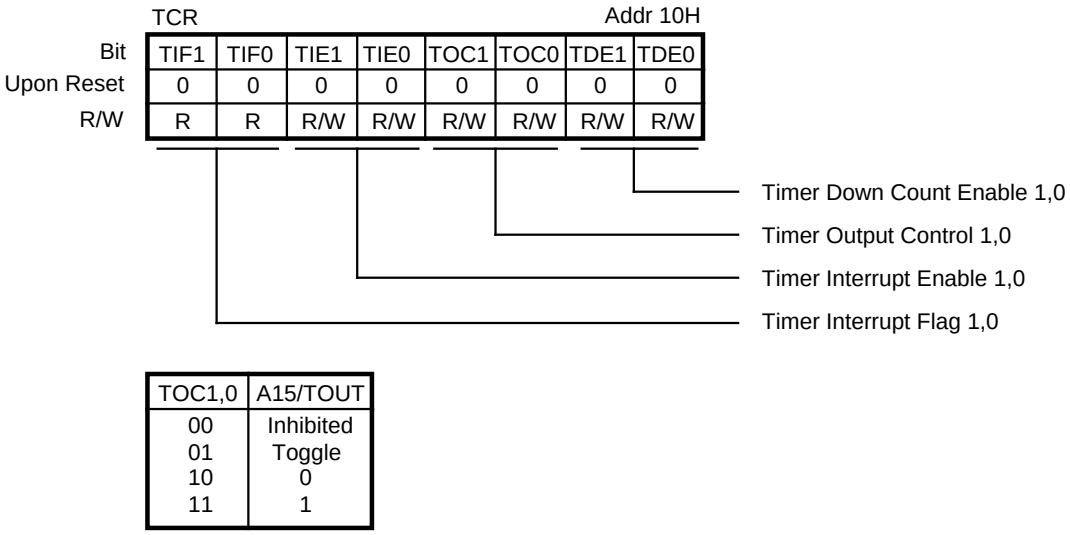


Figure 30. Timer 1 Reload Register H

TIMER CONTROL REGISTER



TOC1,0	A15/TOUT
00	Inhibited
01	Toggle
10	0
11	1

Figure 31. Timer Control Register

STANDBY Mode Exit with BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the Z8S180 exits STANDBY mode when the /BUSREQ input is asserted; the crystal oscillator is then restarted. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the Z8S180 are resumed.

The Z8S180 relinquishes the system bus after the clocking is resumed by:

- Tri-State the address outputs A19 through A0.
- Tri-State the bus control outputs /MREQ, /IORQ, /RD and /WR.
- Asserting /BUSACK

The Z8S180 regains the system bus when /BUSREQ is deactivated. The address outputs and the bus control outputs are then driven High; the STANDBY mode is exited.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the /BUSREQ would not cause the Z8S180 to exit STANDBY mode.

If STANDBY mode is exited due to a reset or an external interrupt, the Z8S180 remains relinquished from the system bus as long as /BUSREQ is active.

STANDBY Mode Exit with External Interrupts

STANDBY mode can be exited by asserting input /NMI. The STANDBY mode may also exit by asserting /INT0, /INT1 or /INT2, depending on the conditions specified in the following paragraphs.

/INT0 wake-up requires assertion throughout duration of clock stabilization time (2^{17} clocks).

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180 are resumed.

1. Exit with Non-Maskable Interrupts

If /NMI is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

2. Exit with External Maskable Interrupts

If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H):

a. If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input would not cause the Z8S180 to exit STANDBY mode. This is true regardless of the state of the Global Interrupt Enable Flag IEF1.

b. If the Global Interrupt Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the Z8S180 to exit STANDBY mode. The CPU performs an interrupt acknowledge sequence appropriate to the input being asserted when clocking is resumed if:

- The interrupt input follows the normal interrupt daisy chain protocol.
- The interrupt source is active until the acknowledge cycle is completed.

c. If the Global Interrupt Flag IEF1 is disabled, i.e., reset to 0, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input will still cause the Z8S180 to exit STANDBY mode. The CPU will proceed to fetch and execute instructions that follow the SLEEP instruction when clocking is resumed.

If the External Maskable Interrupt input is not active until clocking resumes, the Z8S180 will not exit STANDBY mode. If the Non-Maskable Interrupt (/NMI) is not active until clocking resumes, the Z8S180 still exits the STANDBY mode even if the interrupt sources go away before the timer times out, because /NMI is edge-triggered. The condition is latched internally once /NMI is asserted Low.

IDLE Mode

IDLE mode is another power-down mode offered by the Z8S180. To enter IDLE mode:

1. Set D6 and D3 to 0 and 1, respectively.

2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.

3. Execute the SLEEP instruction.

CONTROL REGISTERS (Continued)

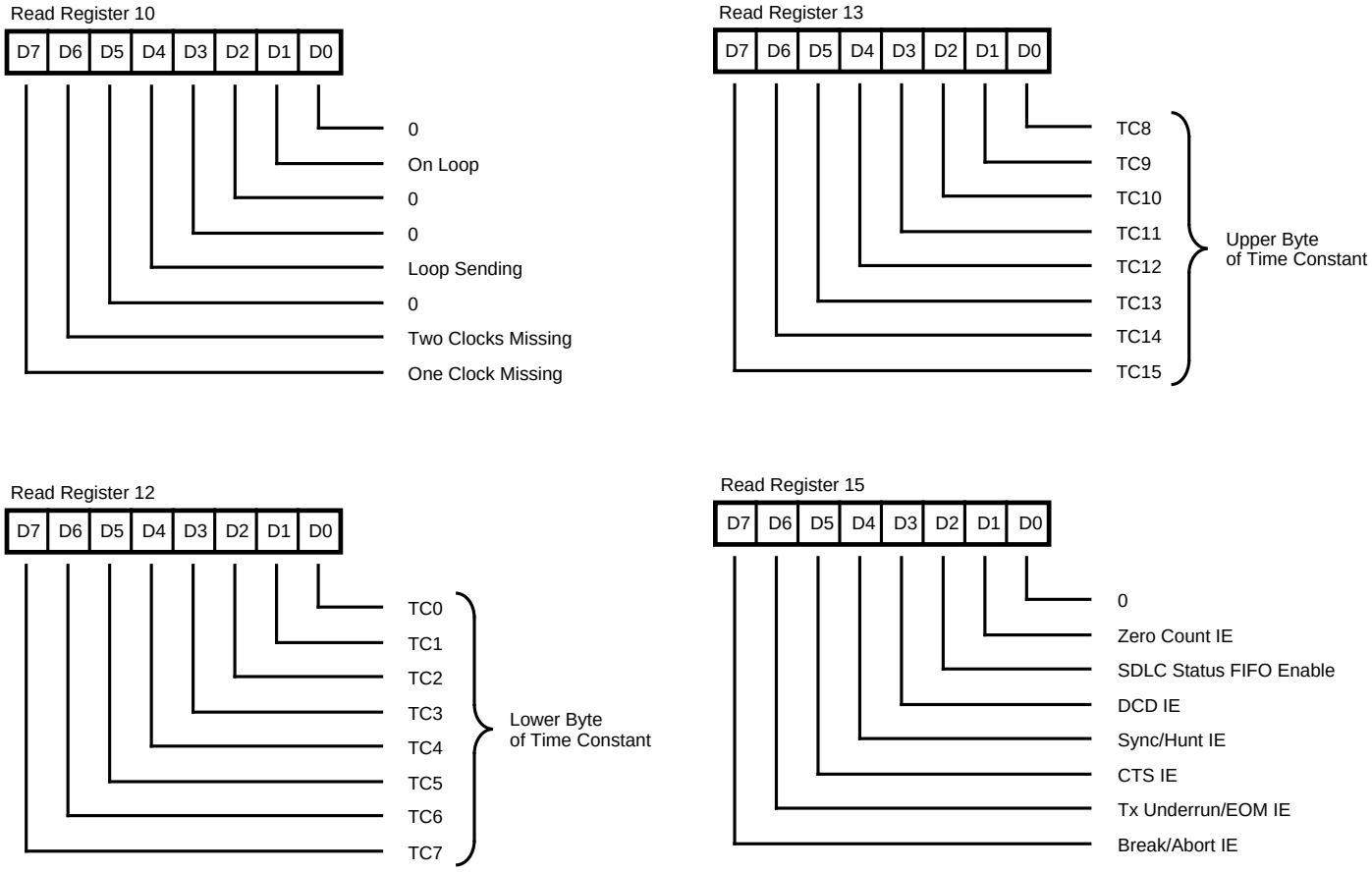


Figure 53. Read Register Bit Functions

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Table 12b. Data Bus Direction (Z182 Bus Master)

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral (IEI=1)	Intack For Off-Chip Peripheral (IEI=0)
Z80182/Z8L182 Data Bus (DD_{OUT}=0)	Z	In
Z80182/Z8L182 Data Bus (DD_{OUT}=1)	Out	In

Table 13a. Data Bus Direction (Z80182/Z8L182 ***is not*** Bus Master)

I/O And Memory Transactions

	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 Idle Mode
Z80182 /Z8L182 Data Bus DD_{OUT}=0)	In	Out	Z	Z	Z	In	Z	Z
Z80182 /Z8L182 Data Bus (DD_{OUT}=1)	In	Out	Z	Z	Z	In	Z	Z

Table 13b. Data Bus Direction (Z80182/Z8L182 ***is not*** Bus Master)

Interrupt Acknowledge Transaction

	Intack For On-Chip Peripheral	Intack For Off-Chip Peripheral
Z80182/Z8L182 Data Bus (DD_{OUT}=0)	Out	In
Z80182/Z8L182 Data Bus (DD_{OUT}=1)	Out	In

Interrupt Enable Register

The IE Register allows each of the 16550/8250 interrupts to the Z180™ MPU to be masked off individually or globally.

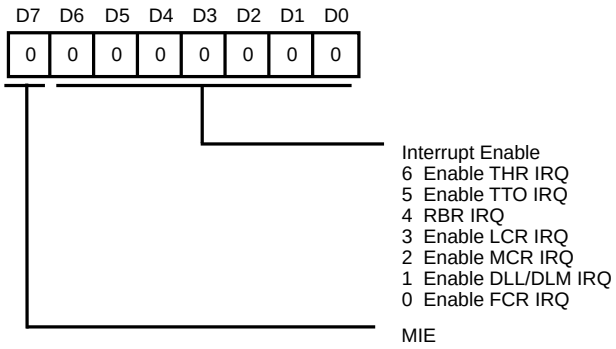


Figure 62. IE Register
(Z180 MPU, Address xxFDH)

Bit 7 Master Interrupt Enable (Read/Write)
If bit 7 is 0, all interrupts from the 16550 MIMIC are masked off. If this bit is 1, then interrupts are enabled individually by setting the appropriate bit.

Bit 6 Enable THR Interrupt (Read/Write)
If this bit is 1, it enables the Transmit Holding Register Interrupt.

Bit 5 Enable TTO Interrupt (Read/Write)
If this bit is 1, it enables the Transmitter Timeout Interrupt. This interrupts the CPU when characters remain in the FIFO below the trigger level and the FIFO is not read or written for the length of time in the transmitter timeout register.

Bit 4 Enable RBR Interrupt (Read/Write)
If this bit is 1, it enables the Receive Buffer Register Interrupt.

Bit 3 Enable LCR Interrupt (Read/Write)
If this bit is 1, it enables the Line Control Register interrupt.

Bit 2 Enable MCR Interrupt (Read/Write)
If this bit is 1, it enables the Modem Control Register Interrupt.

Bit 1 Enable DLL/DLM Interrupt (Read/Write)
If this bit is 1, it enables the Divisor Latch Least and Most Significant Byte interrupts.

Bit 0 Enable FCR Interrupt (Read/Write)
If this bit is 1 , then interrupts are enabled for a PC write to the FIFO control register (FCR) or for occurrence of Tx Overrun.

Priority of interrupts are in this order:

(Highest)	6	THR IRQ
	5	TTO IRQ
	4	RBR IRQ
	3	MCR IRQ
	2	LCR IRQ
	1	DLL IRQ
	1	DLM IRQ
(Lowest)	0	FCR or Tx OVERRUN IRQ

Interrupt Vector Register

The Interrupt Vector Register contains either the opcode (Z180 Interrupt Mode 0) or the modified vector used as the lower address for a Z180 interrupt service routine (Z180 Interrupt Mode 2), depending upon the VIS bit in the MMC Register (MIMIC Master Control Register). If the VIS bit is 0, then Z180 Mode 0 interrupt is selected; if VIS is 1, then Z180 Mode 2 is selected. Note that in Z180 Interrupt Mode 0, the data input to the MPU during the interrupt acknowledge cycle is an instruction opcode; in Z180 Interrupt Mode 2, this data (modified depending on the source of the interrupt) becomes part of an address from which to get the starting address of the interrupt service routine.

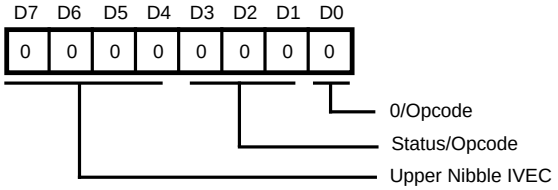


Figure 63. IVEC Register
(Z180 MPU, Address xxFCH)

Bits 7-4 Upper Nibble IVEC (Read/Write)
These four bits generate either an opcode for Z180 Interrupt Mode 0, or the upper four bits of the interrupt modified vector used as an 8-bit address to support the Z180 Interrupt Mode 2. These bits are read/write and always read back what was last written to them.

Bits 3-1 Interrupt Modified Vector/Opcode (Read/Write Table 16)
These three bits are the Interrupt Status bits when VIS in the MMC register is 1 (Z180 Interrupt Mode 2). If VIS bit is 0, then this field contains bit 3-bit 1 of the opcode. If the VIS bit is 0, then these bits contain what was last written to them.

Interrupt Vector Register (Continued)

Table 16. Interrupt Status Bits

Bits 3, 2, 1	Interrupt Request
000	NO IRQ
001	FCR or Tx OVRN IRQ
010	DLL/DLM IRQ
011	LCR IRQ*
100	MCR IRQ*
101	RBR IRQ
110	TTO IRQ
111	THR IRQ

Note: * The order of LCR and MCR does not follow that of the IE Register.

Bit 0 0/Opcode (Read/Write)
This bit is always 0 when the VIS bit is 1. If the VIS bit is 0, this bit reads back what was last written to it.

The Interrupt Vector Register serves both interrupt modes. When the VIS bit is 0, the last value written to the register can be read back. If the VIS bit is 1, and an interrupt is pending, the value read is the last value written to the upper nibble plus the status for the interrupt that is pending. If no interrupt is pending, then the last value written to the upper nibble plus the lower nibble is read from the register.

If the vector includes the status, then the lower four bits of the vector change asynchronously depending on the interrupting source. Since this vector changes asynchronously, then the interrupt service routine to read the IVEC register might read the source of the most recent IRQ/INTACK cycle if that IRQ does not have its IUS set.

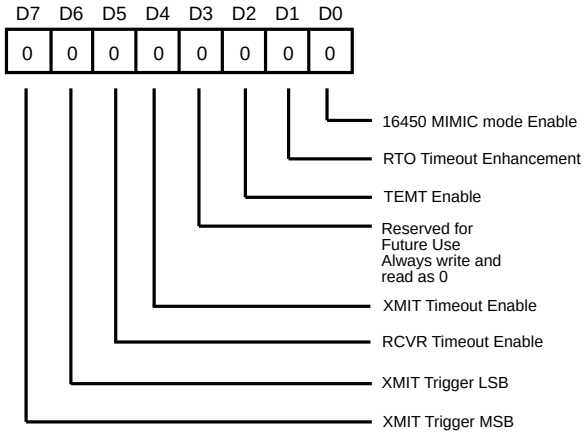


Figure 64. FIFO Status and Control Register
(Z180 MPU Read/Write, Address xxECH)

Bit 7 and Bit 6 XMIT Trigger MSB,LSB
This field determines the number of bytes available to read in the transmitter FIFO before an interrupt occurs to the MPU (Table 17).

Table 17. Transmitter Trigger Level

b7	b6	Level (# bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Bit 5 Receive Timeout Enable
This bit enables the Z80182/Z8L182 Receive Timeout Timer that is used to emulate the four character timeout delay that is specified by the 16550. If no read or write to the RCVR FIFO has taken place and data bytes are available, but are below the PC trigger level. If this timer reaches zero, an interrupt is sent to the PC.

Bit 4 Transmitter Timeout Enable
This bit enables the Z80182/Z8L182 timer that is used to interrupt the Z180 MPU if characters are available, but are below the trigger level. The timer is enabled to count down if this bit is 1 and the number of bytes is below the set transmitter trigger level. The timer will timeout and interrupt the MPU if no read or write to the XMIT FIFO takes place within the timer interval.

Bit 3 Reserved. Program to zero.

Bit 2 (Reset value = 0) TEMT/Double Buffer
When enabled the Tx buffer can hold one extra byte (2 bytes total in 16450 mode). **(Do not enable in 16550 mode.)**

TEMT Emulation
If character delay emulation is not used the TEMT bit is automated. (Refer to page 26 for TEMT/Double Buffer information.)

Bit 1 RTO Timeout Enhancement
(Reset value = 0) Setting this bit will enable the RTO timeout to emulate the 16550 device. When enabling this feature, the receive timeout timer will not begin counting down until the character emulation timer for each byte of data in the Rx FIFO has expired.

Bit 0 16450 MIMIC Mode Enable
(Reset value=0) This bit = 1 will force the mimic into 16450 mode. Bit 0 in the FCR reg is forced to zero as well as the mimic internal FIFO enable. When used, this bit should be programmed at MIMIC initialization and not modified afterwards.

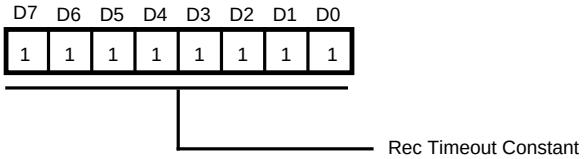


Figure 65. Receive Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEAH)

This register contains an 8-bit constant for emulation of the 16550 four character timeout feature. Software must determine the value to load into this register based on the bit rate and word length specified by the MIMIC interface with the PC. This timer receives its input from the /TRxCB Clock of the ESCC. This timer is enabled to down count when the enable bit in the FSR register is set and the trigger level interrupt has not been activated on the RCVR FIFO. The counter reloads and counts down each time there is a read or write to the RCVR FIFO.

The receive timeout timer is enhanced to emulate the actual 16550 when bit 1 of the FIFO status and control register is enabled. Under most circumstances, this register should be programmed for four character timers (40d, 8-N-1).

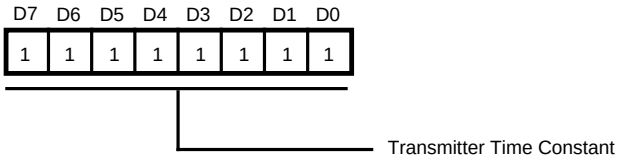


Figure 66. Transmit Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEBH)

This register contains an 8-bit constant for determining the interval for the Transmit Timeout Timer. If allowed to decrement to zero, this timer interrupts the MPU by setting the THR bit in the IUS/IP register. This timer receives its input from the /TRxCB Clock of the SCC. The timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the XMIT FIFO. The counter reloads each time there is a read or write to the XMIT FIFO.

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z180™ MPU and the PC/XT/AT, two timers have been added to alleviate any software problems that a high speed parallel data transfer might cause. These timers allow the programmer to slow down the data transfer just as if the 16550 MIMIC interface had to shift the data in and out serially. The Timers receive their input from the /TRxCB Clock since, in 16550 MIMIC mode, the ESCC channel B is disabled. For example, the clock source for the 8-bit registers: RTTC (Receive Timeout Time Constant, xxEAH), TTTC (Transmit Timeout Time Constant, xxEBH), TTCR (Transmit Time Constant Register, xxFAH) and RTCR (Receive Time Constant Register, xxFBH) uses the /TRxCB Clock output. The /TRxCB Clock output needs to be generated by the ESCC's channel B's 16-bit BRG as its clock source, thus allowing the programmer to access a total of 24 bits as a timer to slow down the data transfer.

In most cases, ESCC Ch. B BRG should be programmed to output at a frequency equivalent to the desired serial transfer rate. The output of the BRG should be routed to the /TRxCB pin.

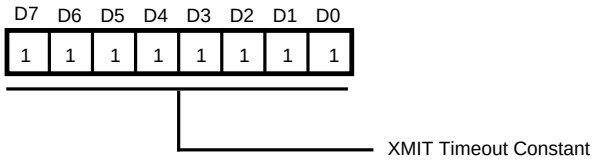


Figure 67. Transmitter Time Constant Register
(Z180 MPU Read/Write, Address xxFAH)

Transmit And Receive Timers (Continued)

When a write from the PC/XT/AT is made to the Transmit Holding Register, an interrupt to the Z180 MPU is generated. The Z180 MPU then reads the data in the Transmit Holding Register. Upon this read, if the Transmitter timer is enabled, the time constant from the Transmitter Time Constant Register is loaded into the Transmitter timer and enables the count. After the timer reaches a count of zero the Transmit Holding Register Empty bit is set. However, the above is only true when the PC/XT/AT is reading the Transmit Holding Register Empty bit. To allow the Z180 MPU to know that it has already read the byte of data, immediately following a read from the Transmit Holding Register, a mirrored Transmit Holding Register, Empty bit is set. This mirrored bit is always read back to the Z180 MPU when it reads the Line Status Register.

If the transmitter timer is not enabled when the Z180 MPU reads the Transmit Holding Register, both Transmit Holding Register Empty bits are set immediately. In FIFO mode of operation, the effect is similar as the status to PC is always delayed such that a PC interrupt for empty FIFO will not occur before the time required for each character read from the FIFO by the Z180 has elapsed. The effect is that the PC will not see data requests from an empty FIFO any faster than would occur with a true UART when the delay feature is enabled. This timer is also used to delay data transfer for TSR buffer to Z80182 THR in double buffer mode.

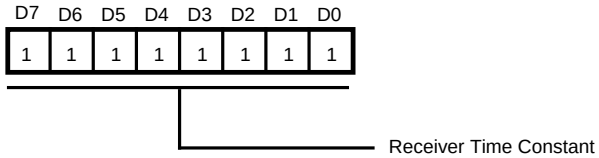


Figure 68. Receive Time Constant Register
(Z180 MPU Read/Write, Address xxFBH)

When the Z180™ MPU writes to the Receive Buffer register and the Receive Timer is enabled, the Receive Timer is loaded with the Receive Time Constant, the timer is enabled and counts down to zero. When the timer reaches zero, the Data Ready bit in the Line Status Register is set. As with the Transmit Timer, the Data Ready bit is also mirrored. Immediately upon a write to the Receive Buffer, the mirrored bit is set to let the Z180 MPU know that the byte has already been written. If the timer is not enabled, then both Data Ready bits are set immediately upon a write to the Receive Buffer. The FIFO mode of operation is similar in that the status to the PC is always delayed by the time required for each character written to the FIFO by the Z180. The effect is that the PC will not see a FIFO trigger level or DMA request faster than would occur with a true UART when the delay feature is enabled.

16550 MIMIC REGISTERS (Continued)

Line Status Register

Bit 7 Error in RCVR FIFO
In 16450 mode, this bit will read logic 0. In 16550 mode this bit is set if at least one data byte is available in the FIFO with one of its associated error bits set. This bit will clear when there are no more errors (or break detects) in the FIFO.

Bit 6 Transmitter Empty
This bit must be set or reset by the MPU by a write to this register bit. If Double Buffer Mode is enabled, the TEMT bit is set/reset automatically. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 5 Transmit Holding Register Empty, THRE
This bit is set to 1 when either the THR has been read (emptied) by the MPU (16450 mode) or the XMIT FIFO is empty (16550 mode). This bit is set to 0 when either the THR or XMIT FIFO become non-empty. A shadow bit exists so that the register bit setting to 1 is delayed by the Transmitter Timer if enabled. The MPU when reading this bit will not see the delay. Both shadow and register bits are cleared when the PC writes to the THR of XMIT FIFO. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 2, 3, 4 Parity Error, Framing Error, Break Detect
These bits are written, indirectly, by the MPU as follows: The bits are first written to shadow bit locations when the MPU write accesses the LSR. When the next character is written to the Receive Buffer or RCVR FIFO, the data in the shadow bits is then copied to the LSR (16450 mode) or FIFO RAM (16550 mode). In FIFO mode bits become available to the PC when the data byte associated with the bits is next to be read (top of FIFO). In FIFO mode, with successive reads of the receiver, the status bits will be set if an error occurs on any byte. Once the MPU writes to the Receive Buffer or RCVR FIFO, the shadow bits are auto cleared. The register bits are cleared upon the PC reading the LSR. In FIFO mode these bits will be set if any byte has the respective error bit set while the PC reads multiple characters from the FIFO.

Bit 1 Overrun Error
This bit is set if the Z180 MPU makes a second write to the Receive Buffer before the PC reads the data in the Buffer (16450 mode) or with a full RCVR FIFO (16550 mode.) No data will be transferred to the RCVR FIFO under these circumstances. This bit is reset when the PC reads the Line Status Register.

Bit 0 Data Ready
This bit is set to 1 when received data is available, either in the RCVR FIFO (16550 mode) or Receive Buffer Register (16450 mode). This bit is set immediately upon the MPU writing data to the Receive Buffer or FIFO if the Receive Timer is not enabled but is delayed by the timer interval if the Receive Timer is enabled. For MPU read access a shadow bit exists so that the MPU does not see the delay the PC does. Both bits are cleared to logic zero immediately upon reading all the data in either the Receive Buffer or FIFO.

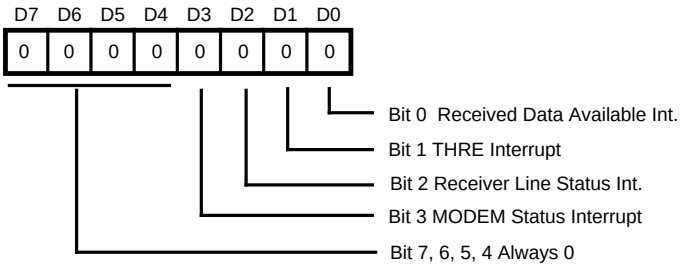


Figure 75. Interrupt Enable Register
(PC Read/Write, Address 01H)
(Z180 MPU Read Only, Address xxF1H)

Interrupt Enable Register

Bits 7, 6, 5, 4 Reserved
These bits will always read 0 (PC and MPU).

Bit 3 Modem Status IRQ
If bits 0, 1, 2 or 3 of the Modem Status Register are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 2 Receive Line Status IRQ
If bits 1, 2, 3 or 4 of the LSR are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 1 Transmit Holding Register Empty IRQ
If bit 5 of the LSR is set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 0 Received Data Available IRQ
If bit 0 of the LSR is set or a Receive Timeout occurs and this enable bit is a logic 1, then an interrupt to the PC is generated.

The data direction register determines which are inputs and outputs in the PC Data Register. When a bit is set to 1 the corresponding bit in the PC Data Register is an input. If the bit is 0, then the corresponding bit is an output.

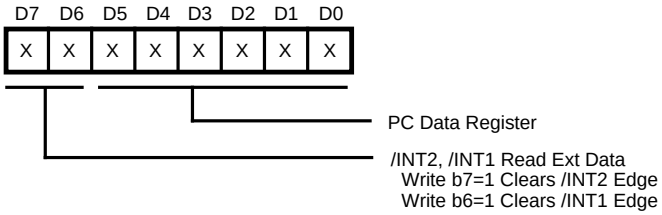


Figure 88. PC, Port C, Data Register
(Z180 MPU Read/Write, Address xxDEH)

When the Z180 MPU writes to the PC Data Register, the data is stored in the internal buffer. The values of Port C data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PC Data Register, the data on the external pins is returned.

Bits 6 and 7 serve the special function of reading the value of the external /INT2 and /INT1 lines. When operating either /INT2 or /INT1 in edge detection mode, the edge detect latch is reset by writing a 1 to bit 6 or 7 respectively. Writing a 0 has no effect. ***These latches should be reset at the end of an /INT1 or /INT2 interrupt service routine when using edge-triggered interrupt modes.***

16550 MIMIC INTERFACE DMA

The 16550 MIMIC is also able to do direct DMA with the PC/XT/AT. DMA is enabled by setting bits 3, 4 and 5 of the Master Control Register. DMA is accomplished by using the two DMA pins and the Transmitter Holding and Receive Data Registers.

If bit 5 is 1, the /HTxRDY pin is equal to the complement of the Transmit Holding Register Empty bit. If bit 5 is 1 and bit 3 is 0 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement of the Transmit Holding Register Empty Shadow bit. If bit 5 is 1 and bit 3 is 1 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Transmit Holding Register Empty Shadow bit.

If bit 4 is 1, then the /HRxRDY pin is equal to the complement of the Data Ready bit. If bit 4 is 1 and bit 3 is 0 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Data Ready Shadow bit. If bit 4 is 1 and bit 3 is 1 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement or the Data Ready Shadow bit.

TIMING DIAGRAMS (Continued)

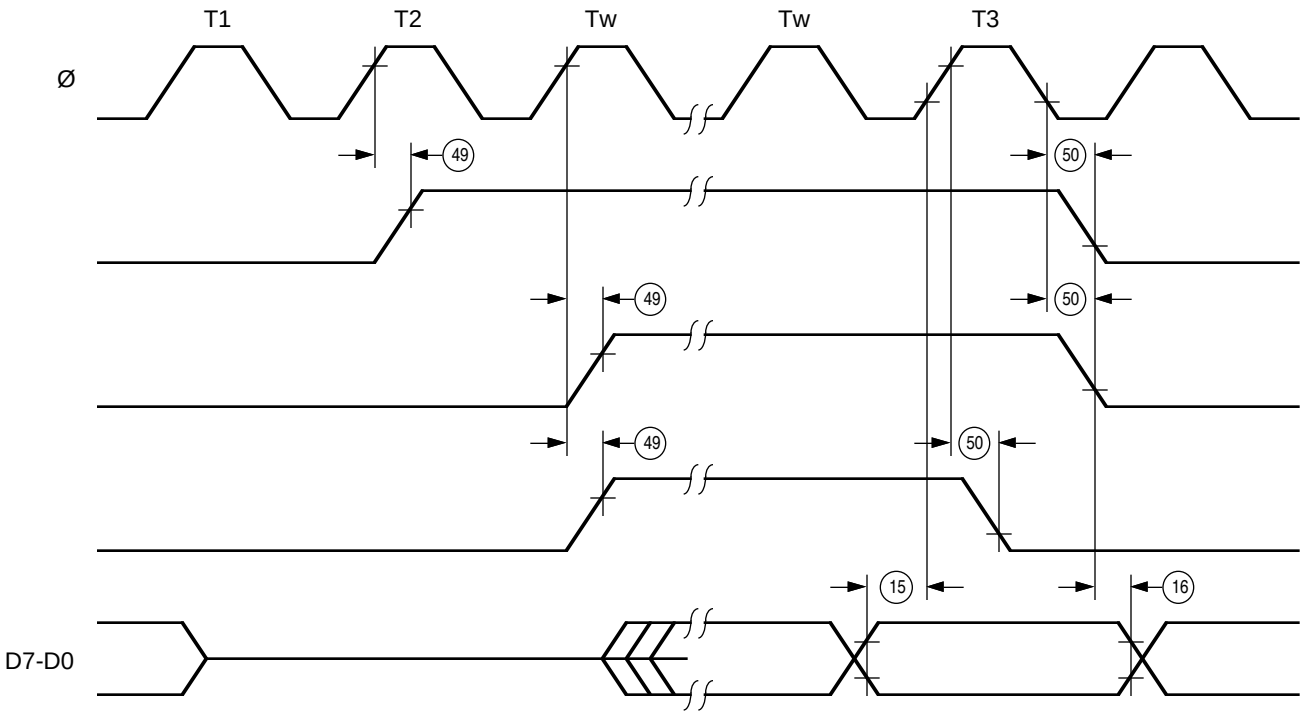


Figure 94. E Clock Timing
(Memory Read/Write Cycle
I/O Read/Write Cycle)

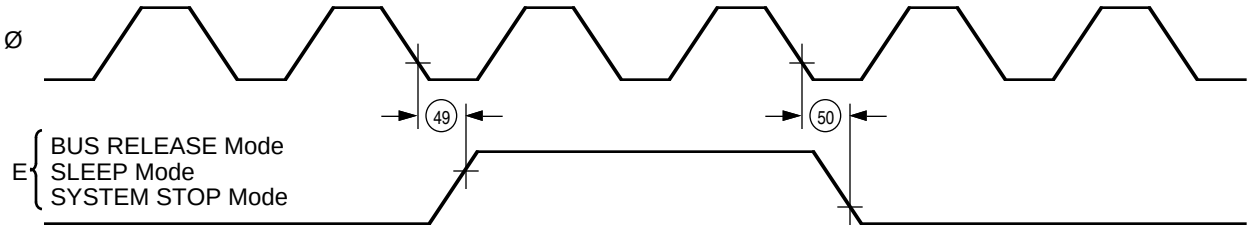


Figure 95. E Clock Timing

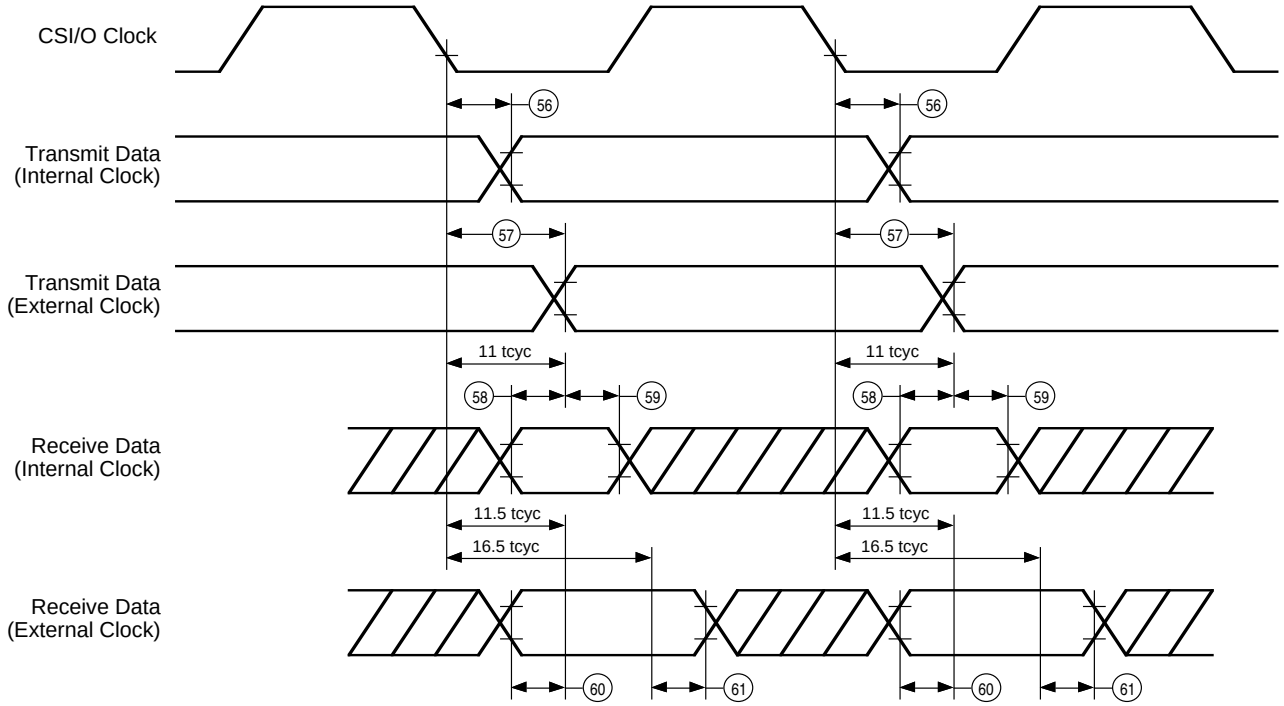


Figure 99. CSI/O Receive/Transmit Timing

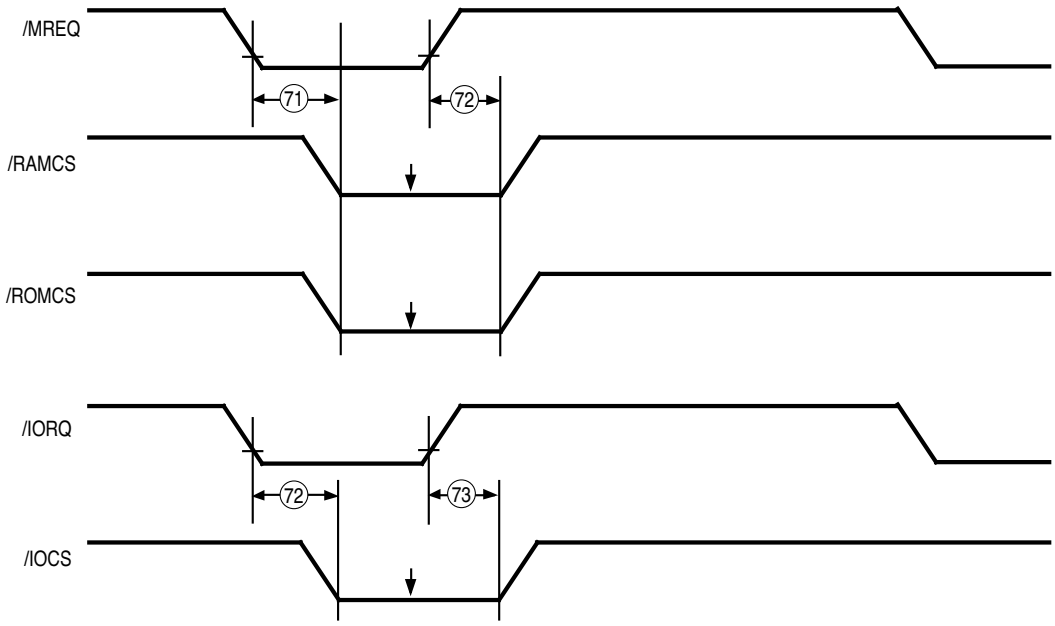


Figure 100 /ROMCS and /RAMCS Timing