Zilog - Z8018233ASC00TR Datasheet

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Understanding Embedded - Microprocessors

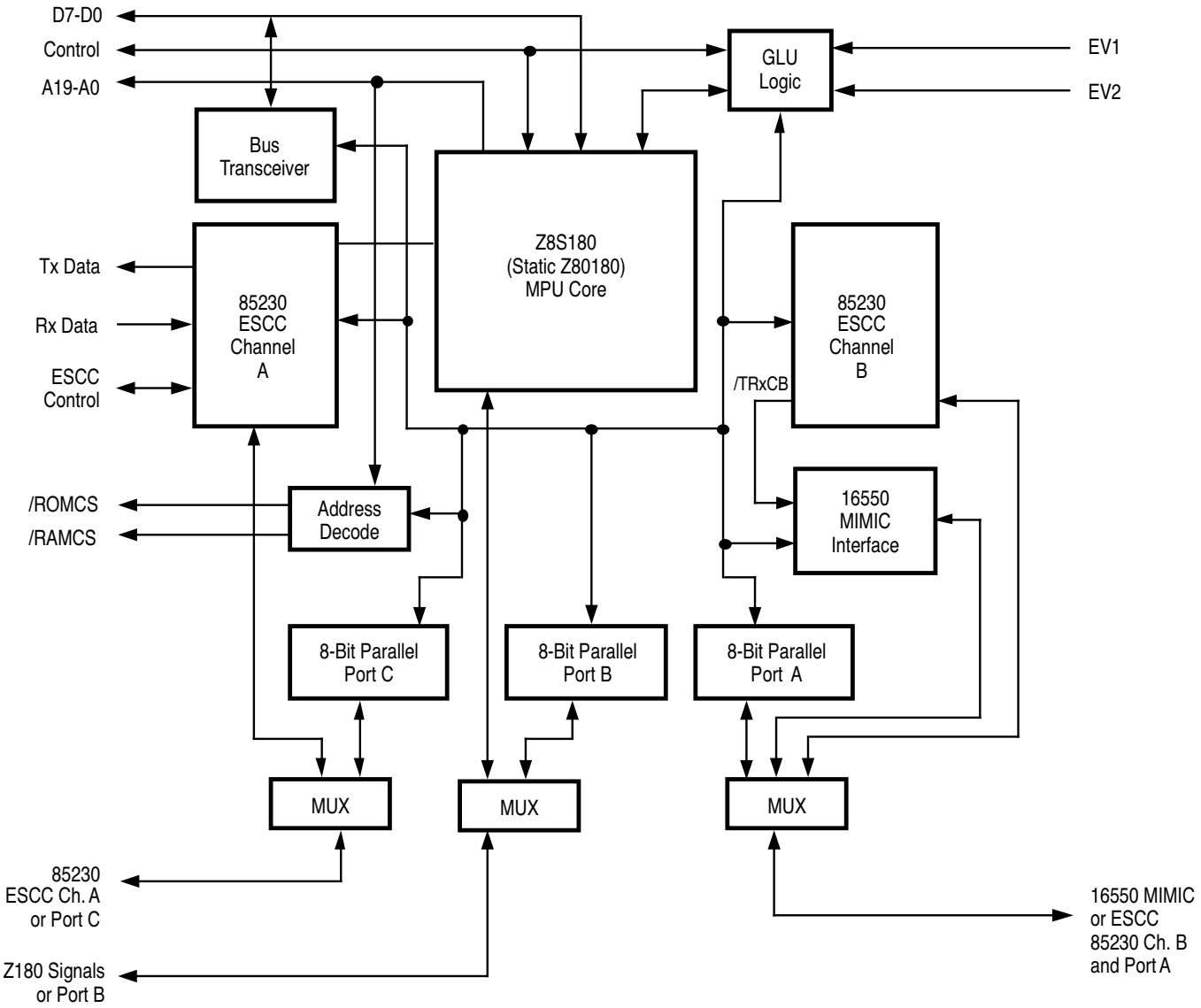
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018233asc00tr

GENERAL DESCRIPTION (Continued)



Note: Conventional use of the term "MPU side" refers to all interface through the Z180 MPU core and "PC side" refers to all interface through the16550 MIMIC interface.

Figure 1. Z80182/Z8L182 Functional Block Diagram

Table 5. Primary, Secondary and Tertiary Pin Functions

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
1	4	ST			
2	5	A0			
3	6	A1			
4	7	A2			
5	8	A3			
6	9	A4			
7	10	A5			
8	11	A6			
9	12	A7			
10	13	A8			
11	14	A9			
12	15	A10			
13	16	A11			
14	17	A12			
15	18	V_{SS}			
16	19	A13			
17	20	A14			
18	21	A15			
19	22	A16			
20	23	A17			
21	24	A18/T_{OUT}			
22	25	V_{DD}			
23	26	A19			
24	27	D0			
25	28	D1			
26	29	D2			
27	30	D3			
28	31	D4			
29	32	D5			
30	33	D6			
31	34	D7			
32	35	/RTS0	PB0		SYS CONF REG Bit 5
33	36	/CTS0	PB1		SYS CONF REG Bit 5
34	37	/DCD0	PB2		SYS CONF REG Bit 5
35	38	TxA0	PB3		SYS CONF REG Bit 5
36	39	RxA0	PB4		SYS CONF REG Bit 5
37	40	TxA1	PB5		SYS CONF REG Bit 6
38	41	RxA1	PB6		SYS CONF REG Bit 6
39	42	RxS//CTS1	PB7		SYS CONF REG Bit 6
40	43	CKA0//DREQ0			

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source
  - Up to 5 Mbits/sec at 20 MHz PCLK (ESCC).
- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit
- NRZ, NRZI or FM encoding/decoding. Manchester Code Decoding (Encoding with External Logic).
- Baud Rate Generator in each Channel
- Digital Phase-Locked Loop (DPLL) for Clock Recovery
- Crystal Oscillator

The following features are implemented in the ESCC™ for the Z80182/Z8L182 only:

- New 32-bit CRC-32 (Ethernet Polynomial)
- ESCC Programmable Clock
  - programmed to be equal to system clock divided by one or two
  - programmed by Z80182 Enhancement Register

Note: The ESCC™ programmable clock must be programmed to divide-by-two mode when operating above the following conditions:

– PHI > 20 MHz at 5.0V

– PHI > 10 MHz at 3.0V

Z85230 ESCC™ BLOCK DIAGRAM

For a detailed description of the Z85230 ESCC, refer to the ESCC Technical Manual. The following figure is the block diagram of the discrete ESCC, which was integrated into the Z182. The /INT line is internally connected to "INTO of the Z182.

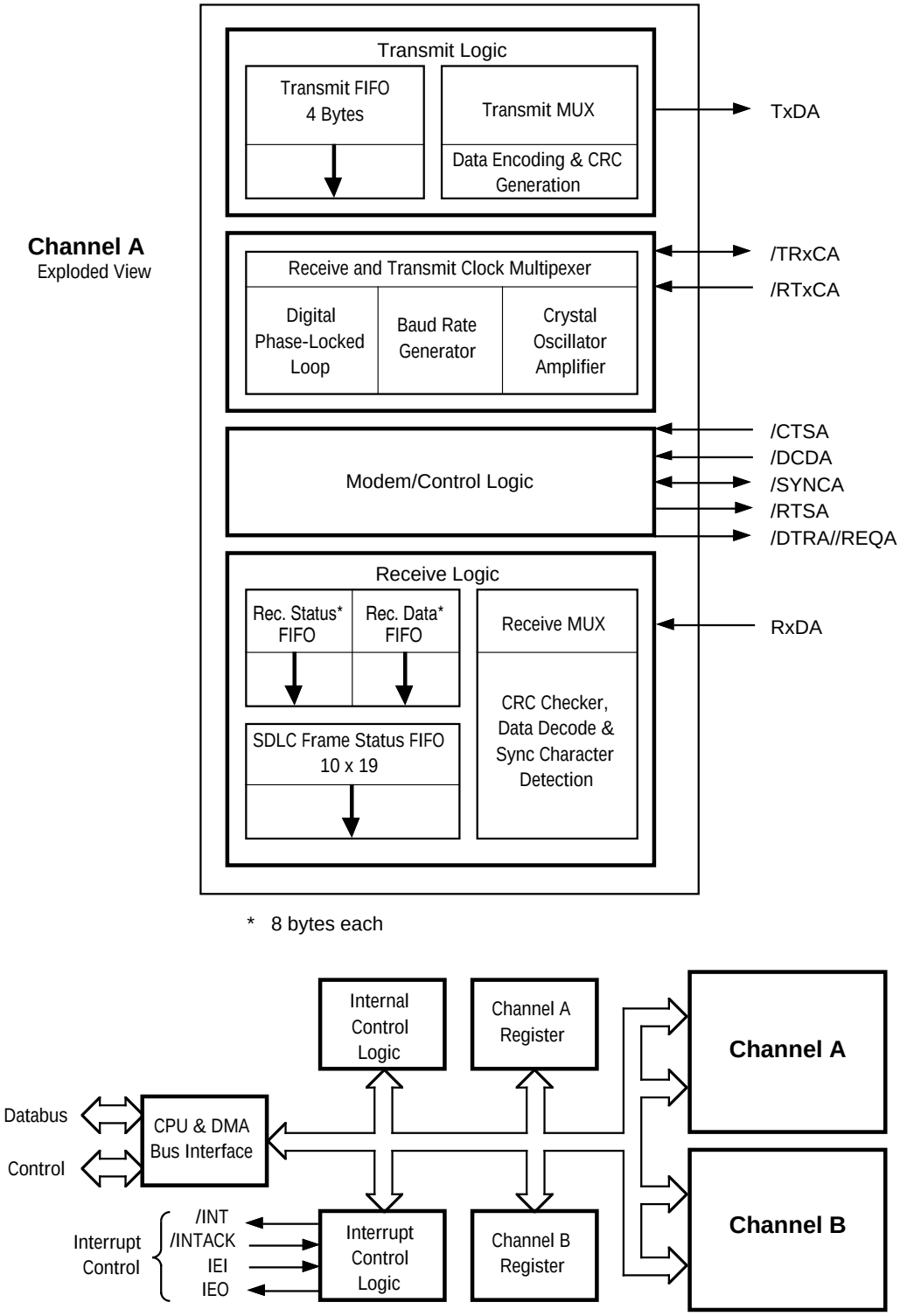


Figure 5. ESCC Block Diagram

Table 6. 16550 Line Status Register

Error	Description	How to Set	How to Clear
Error in RCVR FIFO	At least one data byte available in FIFO with one error	At least one error in receiver FIFO	When there are no more errors
*TEMT	Transmitter empty	MPU writes a 1	MPU writes a 0
† *THRE	Transmitter holding register is empty	When MPU has read or emptied the holding register	When holding register is not empty
Break Detect	Break occurs when received data input is held in logic-0 for longer than a full word transmission	MPU writes 1	There is a PC-side read of the LSR
Framing Error	Received character did not have a valid stop bit	MPU writes 1	There is a PC-side read of the LSR
Parity Error	Received character did not have correct even or odd parity	MPU writes 1	There is a PC-side read of the LSR
Overrun Error	Overlapping received characters, thereby destroying the previous character	MPU makes two writes to receiver buffer register	There is a PC-side read of the LSR
†Data Ready	Indicates complete incoming data has been received	MPU writes to RCVR FIFO or receiver buffer register	Empty Receiver or Receiver FIFO

Notes:

* The TEMT and THRE bits take on different functions when TEMT/Double Buffer mode is enabled.

† These signals are delayed to HOST when using character emulation delay.

PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only). The Ports are controlled through two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

PROGRAMMING

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for Z182 peripheral access. The full sixteen address lines are decoded for on-chip Z180 MPU access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers through the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated through the System Configuration Register and the Interrupt Edge/Pin MUX Register.

Table 7. Z80182/Z8L182 MPU Registers

Register Name	MPU Addr	PC Addr
Z80182/Z8L182 MPU Control Registers	0000H to 00x3FH (Relocatable to 0040H to 007FH or 0080H to 00BFH)	None

Note:
"x" indicates don't care condition

Table 8. Z80182/Z8L182 MIMIC Register MAP

Register Name	MPU Addr/Access		PC Addr/Access	
MMC MIMIC Master Control Register	xxFFH	R/W	None	
IUS/IP Interrupt Pending	xxFEH	R/Wb7	None	
IE Interrupt Enable	xxFDH	R/W	None	
IVEC Interrupt Vector	xxFCH	R/W	None	
TTCR Transmit Time Constant	xxFAH	R/W	None	
RTCR Receive Time Constant	xxFBH	R/W	None	
FSCR FIFO Status and Control	xxECH	R/W7-4	None	
RTTC Receive Timeout Time Constant	xxEAH	R/W	None	
TTTC Transmit Timeout Time Constant	xxEBH	R/W	None	
RBR Receive Buffer Register	xxF0H	W only	00H	DLAB=0 R only
THR Transmit Holding Register	xxF0H	R only	00H	DLAB=0 W only
IER Interrupt Enable Register	xxF1H	R only	01H	DLAB=0 R/W
IIR Interrupt Identification	None		02H	R only
FCR FIFO Control Register	xxE9H	R only	02H	W only
MM REGISTER	XXE9H	W only	None	
LCR Line Control Register	xxF3H	R only	03H	R/W
MCR Modem Control Register	xxF4H	R only	04H	R/W
LSR Line Status Register	xxF5H	R/Wb6432	05H	R only
MSR Modem Status Register	xxF6H	R/Wb7-4	06H	R only
SCR Scratch Register	xxF7H	R only	07H	R/W
DLL Divisor Latch (LSByte)	xxF8H	R only	00H	DLAB=1 R/W
DLM Divisor Latch (MSByte)	xxF9H	R only	01H	DLAB=1 R/W

SYSTEM CONTROL REGISTERS

IL — Addr 33H

Bit	IL7	IL6	IL5	-	-	-	-	-
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W					

Interrupt Vector Low

Figure 46. Interrupt Vector Low Register

ITC — Addr 34H

Bit	TRAP	UFO	-	-	-	ITE2	ITE1	ITE0
Upon Reset	0	0	1	1	1	0	0	1
R/W	R/W	R				R/W	R/W	R/W

/INT Enable 2, 1, 0
Undefined Fetch Object
TRAP

Figure 47. INT/TRAP Control Register

RCR — Addr 36H

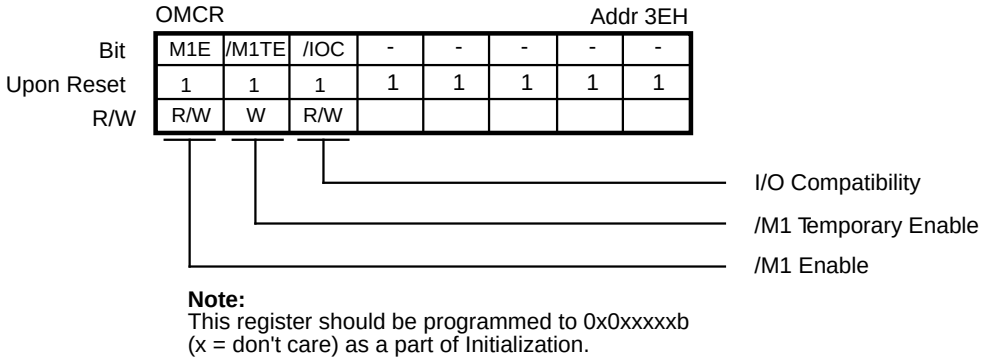
Bit	REFE	REFW	-	-	-	-	CYC1	CYC0
Upon Reset	1	1	1	1	1	1	0	0
R/W	R/W	R/W					R/W	R/W

Cycle Select
Refresh Wait State
Refresh Enable

CYC1, 0	Interval of Refresh Cycle
00	10 states
01	20 states
10	40 states
11	80 states

Figure 48. Refresh Control Register

SYSTEM CONTROL REGISTERS (Continued)



Note:
This register should be programmed to 0x0xxxxxb (x = don't care) as a part of Initialization.

Figure 49. Operation Mode Control Register

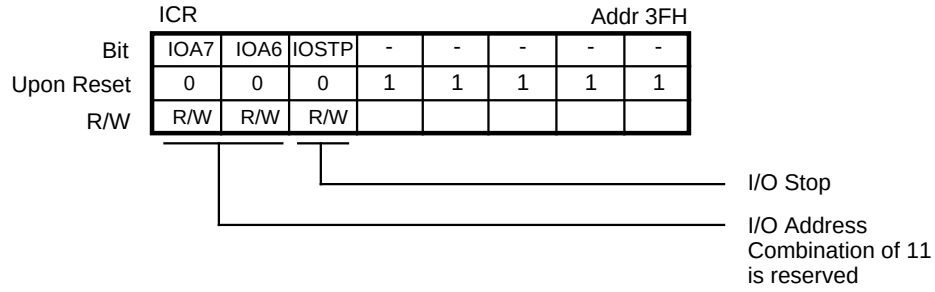


Figure 50. I/O Control Register

STANDBY Mode Exit with BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the Z8S180 exits STANDBY mode when the /BUSREQ input is asserted; the crystal oscillator is then restarted. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the Z8S180 are resumed.

The Z8S180 relinquishes the system bus after the clocking is resumed by:

- Tri-State the address outputs A19 through A0.
- Tri-State the bus control outputs /MREQ, /IORQ, /RD and /WR.
- Asserting /BUSACK

The Z8S180 regains the system bus when /BUSREQ is deactivated. The address outputs and the bus control outputs are then driven High; the STANDBY mode is exited.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the /BUSREQ would not cause the Z8S180 to exit STANDBY mode.

If STANDBY mode is exited due to a reset or an external interrupt, the Z8S180 remains relinquished from the system bus as long as /BUSREQ is active.

STANDBY Mode Exit with External Interrupts

STANDBY mode can be exited by asserting input /NMI. The STANDBY mode may also exit by asserting /INT0, /INT1 or /INT2, depending on the conditions specified in the following paragraphs.

/INT0 wake-up requires assertion throughout duration of clock stabilization time (2^{17} clocks).

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180 are resumed.

1. Exit with Non-Maskable Interrupts

If /NMI is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

2. Exit with External Maskable Interrupts

If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H):

a. If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input would not cause the Z8S180 to exit STANDBY mode. This is true regardless of the state of the Global Interrupt Enable Flag IEF1.

b. If the Global Interrupt Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the Z8S180 to exit STANDBY mode. The CPU performs an interrupt acknowledge sequence appropriate to the input being asserted when clocking is resumed if:

- The interrupt input follows the normal interrupt daisy chain protocol.
- The interrupt source is active until the acknowledge cycle is completed.

c. If the Global Interrupt Flag IEF1 is disabled, i.e., reset to 0, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input will still cause the Z8S180 to exit STANDBY mode. The CPU will proceed to fetch and execute instructions that follow the SLEEP instruction when clocking is resumed.

If the External Maskable Interrupt input is not active until clocking resumes, the Z8S180 will not exit STANDBY mode. If the Non-Maskable Interrupt (/NMI) is not active until clocking resumes, the Z8S180 still exits the STANDBY mode even if the interrupt sources go away before the timer times out, because /NMI is edge-triggered. The condition is latched internally once /NMI is asserted Low.

IDLE Mode

IDLE mode is another power-down mode offered by the Z8S180. To enter IDLE mode:

1. Set D6 and D3 to 0 and 1, respectively.

2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.

3. Execute the SLEEP instruction.

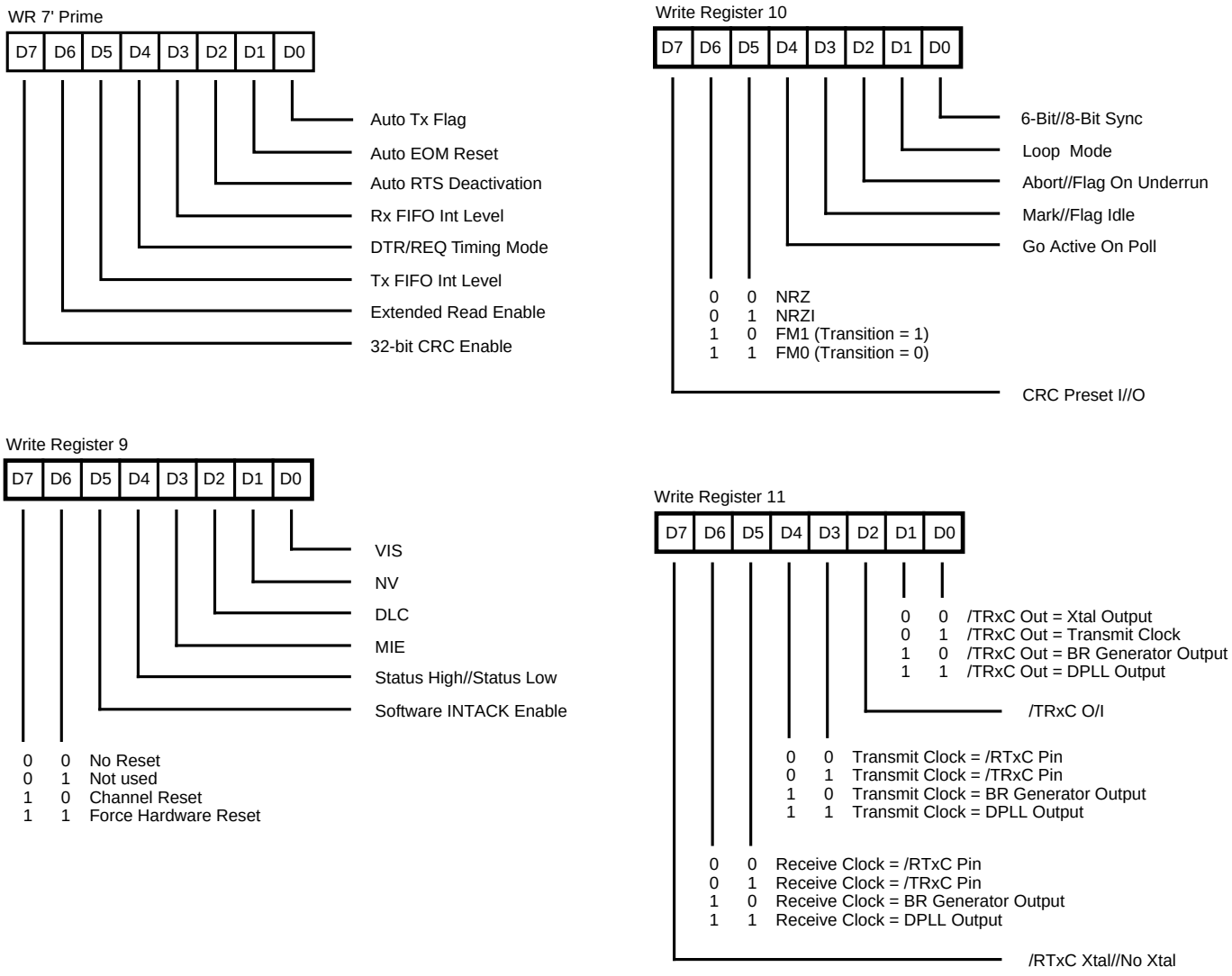


Figure 52. Write Register Bit Functions (Continued)

CONTROL REGISTERS (Continued)

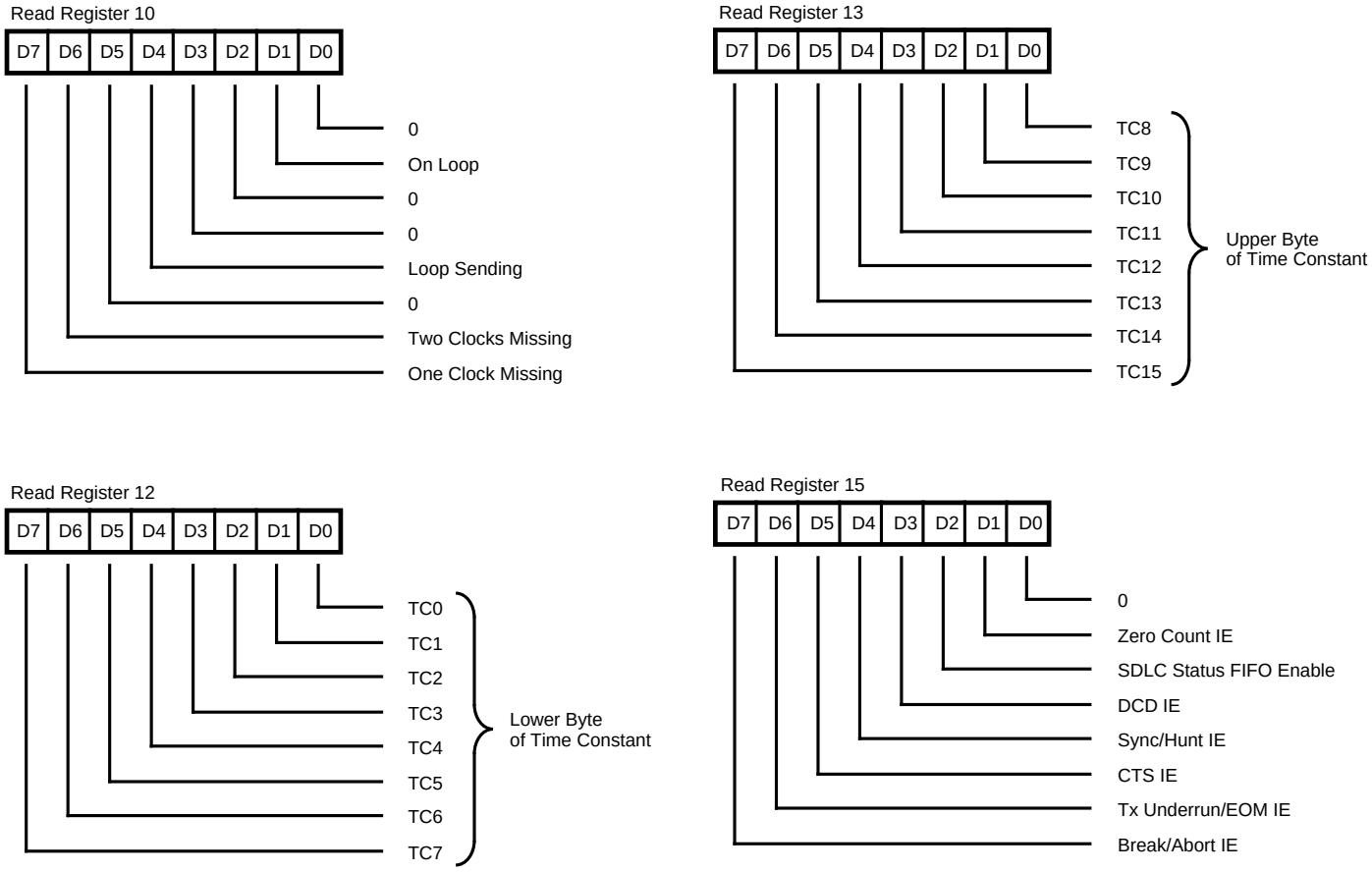


Figure 53. Read Register Bit Functions

INTERRUPT EDGE/PIN MUX REGISTER (Continued)

Bit 0. Programming this bit to 1 selects a 16 cycle wait delay on recovery from HALT. Halt Recovery is disabled if bit 5 of the enhancement register is set to 1. A 0 selects no wait delay on Halt recovery.

If Halt Recovery is selected, the following pins assume the following states during halt and during the recovery, whether it is in HALT, SLP, IDLE or STBY Modes:

Address	=	Z
Data Bus	=	Z
RD	=	Z
WR	=	Z
MREQ/MRD	=	Z
M1	=	1
ST	=	1
IORQ	=	1
BUSACK	=	1
RFSH	=	1
E	=	Note 3
IOCS	=	Z
MWR	=	1 ***(Note 4)***

Notes:

1. This assumes that BUSREQ is not activated during the halt.

2. This assumes that the refresh is not enabled. This would not be a logical case since the address bus is tri-stated during the Halt mode.

3. There is no control on the E line during the halt recovery so transitions on the pin are possible.

4. This is only true if MWR function is enabled.

The Halt recovery mode is implemented by applying wait states to the next CPU operation following the exit from halt. All signals listed above are forced to their specified state (unless otherwise noted) during halt and also during the recovery state. Sixteen cycles after the halt pin goes High the signals are released to their normal state, then eight wait states are inserted to allow proper access to accommodate slow memories.

After the first memory access, the wait states will be inserted as programmed in the wait state generators.

In addition, if bit 4 of the Z80182 Enhancement Register is set, the TxDA pin will be tri-stated during Halt and Recovery modes.

16550 MIMIC INTERFACE REGISTERS

MIMIC Master Control Register (MMC)

The 16550 MIMIC interface is controlled by the MMC register. Setting it allows for different modes of operation such as using the 8-bit counters, DMA accesses, and which IRQ structure is used with the PC/XT/AT.

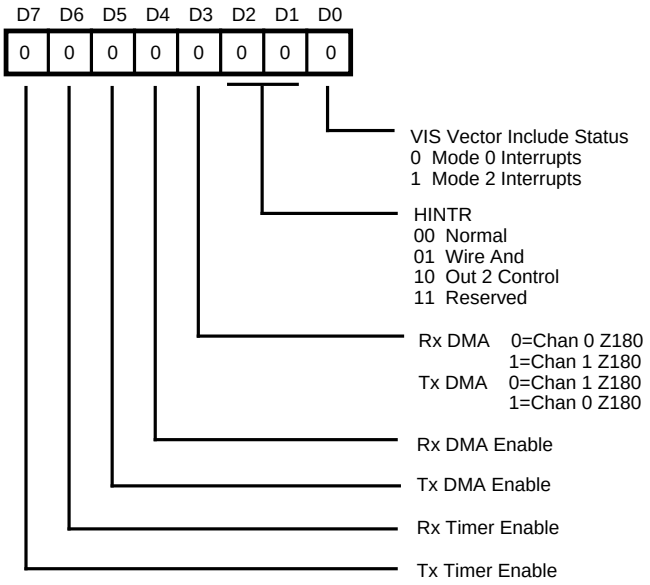


Figure 60. MIMIC Master Control Register
(Z180 MPU Read/Write, Address xxFFH)

Bit 7 Transmit Emulation Delay Counter Enable (Read/Write)
If bit 7 is set to 1, it enables the transmit delay timer. When the Z180 reads the Transmit Register, it loads the transmit delay timer from the Transmit Time Constant Register and enables the timer to count down to zero. This timer delays setting the Transmit Holding Register Empty (THRE) bit until the timer times out. If this bit is 0, then THRE is set immediately on a Z180 read of the Transmit Register. This bit also enables the emulation timer used in Transmitter Double Buffering.

Bit 6 Receive Emulation Delay Counter Enable (Read/Write)
If bit 6 is set to 1, it enables the receive delay timer. When the Z180 writes to the Receive Buffer, it loads the receive delay timer from the Receive Time Constant Register and enables the timer to count down to zero. This timer delays setting the Data Ready (DR) bit in the LSR until the timer times out. If this bit is 0 then DR is set immediately on a Z180 write to the Receive Buffer.

Both counters are single pass and stop on a count of Zero. Their purpose is to delay data transfer just as if the 16550 UART had to shift the data in and out. This is provided to alleviate any software problems a high speed continuous data transfer might cause to existing software. If this is not a concern, then data can be read and written as fast as the two machines can access the devices. In FIFO mode of operation , the timers are used to delay the status to the PC interface by the time required to actually shift the characters out, or in, if an actual UART were present.

Bit 5 Transmit DMA Enable (Read/Write)
If this bit is set to 1, it enables the Transmit DMA function.

Bit 4 Receive DMA Enable (Read/Write)
If this bit is set to 1, it enables the Receive DMA function.

Bit 3 Receive DMA Channel Select (Read/Write)
If bit 3 is set to 0, then Receive DMA transfer is done through Z180 DMA channel 0 and the Transmit DMA is done through DMA channel 1. If bit 3 is set to 1, then Receive DMA transfer is done through Z180 DMA channel 1 and the Transmit DMA is done through DMA channel 0.

Bits 2,1 Interrupt Select (Read/Write).
See Table 15.

Bit 0 Vector Include Status (Read/Write)
This bit is used to select the interrupt response mode of the Z180. A 0 in this bit enables Mode 0 interrupts; a 1 enables Mode 2 response.

Table 15. MIMIC Master Control Register Interrupt Select

Bit 2	Bit 1	HINTR Function
0	0	HINTR is set to normal 16550 MIMIC mode. A fully driven output is required when external priority arbiters are used.
0	1	A wired AND condition on the HINTR pin is possible to the PC/XT/AT. The interrupt is active High with only the pull-up of the HINTR pin driving; otherwise this pin is tri-state. Wired AND is needed when an external arbiter is not available.
1	0	HINTR is driven when out 2 of the Modem Control Register is 1. HINTR is tri-state when MCR out 2 is 0.
1	1	RESERVED

Although this bit is disabled by default, it is advised that this bit is enabled to prevent interrupt conflict between MIMIC and ESCC interrupts.

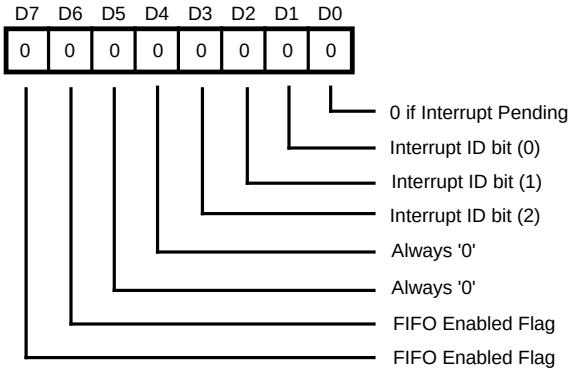


Figure 73. Interrupt Identification Register
(PC Read Only, Address 02H)
(Z180 MPU no access)

Interrupt Identification Register

Bit 7 and Bit 6 FIFO's Enabled
These bits will read 1 if the FIFO mode is enabled on the MIMIC.

Bit 5 and Bit 4 Always Read 0
Reserved bits.

Bits 3-1 Interrupt ID Bits
This 3-bit field is used to determine the highest priority interrupt pending (see Table 19).

Bit 0 Interrupt Pending
This bit is logic 0 and interrupt is pending.

When the PC accesses the IIR, the contents of the register and all pending interrupts are frozen. Any new interrupts will be recorded, but not acknowledged, during the IIR access.

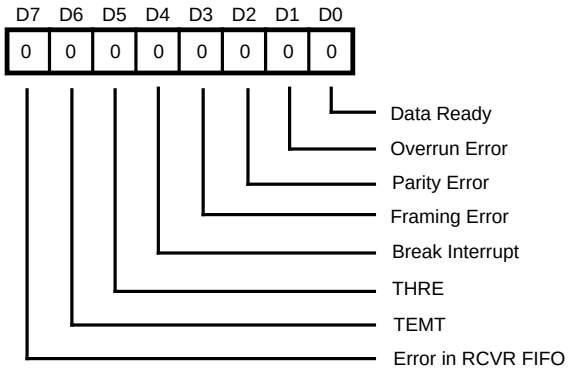


Figure 74. Line Status Register
(PC Read Only, Address 05H)
(Z180 MPU Read/Write bits 6, 4, 3, 2, Address xxF5H)

Table 19. Interrupt Identification Field

b3	b2	b1	Priority	Interrupt Source	INT Reset Control
0	1	1	Highest	Overrun, Parity, Framing error or Break detect bits set by MPU	Read Line Status Register
0	1	0	2nd	Received Data trigger level	RCVR FIFO drops below trigger level
1	1	0	2nd	Receiver Timeout with data in RCVR FIFO.	Read RCVR FIFO
0	0	1	3rd	Transmitter Holding Register Empty.	Writing to the Transmitter Holding Register or reading the Interrupt Identification Register when the THRE is the source of the interrupt.
0	0	0	4th	MODEM status: CTS, DSR, RI or DCD	Reading the MODEM status register.

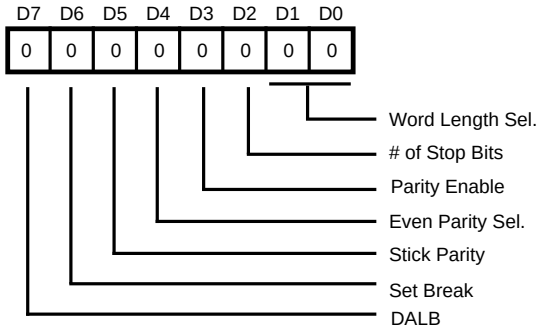


Figure 76. Line Control Register
(PC Read/Write, Address 03H)
(Z180 MPU Read Only, Address xxF3H)

Line Control Register

Bit 7 Divisor Latch Access Bit (DALB)
This bit allow access to the divisor latch by the PC/XT/AT. If this bit is set to 1, access to the Transmitter, Receiver and Interrupt Enable Registers is disabled. When an access is made to address 0 the Divisor Latch Least Significant byte is accessed. If an access is made to address 1, the Divisor Latch Most Significant byte is accessed.

Bit 6 - Bit 0
These bits do not affect the Z80182/Z8L182 directly, however they can be read by the Z180 MPU and the 16550 MIMIC modes can be emulated by the Z180 MPU.

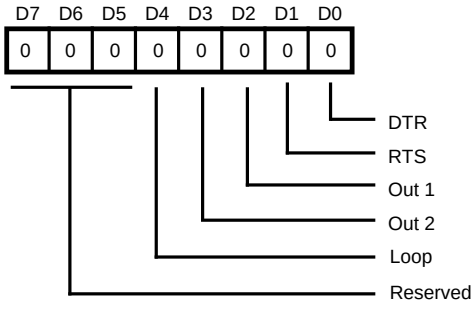


Figure 77. Modem Control Register
(PC Read/Write, Address 04H)
(Z180 MPU Read Only, Address xxF4H)

Modem Control Register

Bit 7-5 Reserved
Reserved for future use, always 0.

Bit 4 Loop
When this bit is set to 1, D3-D0 field reflects the status of Modem Status Register, as follows:

RI = Out 1
DCD = Out 2
DSR = DTR
CTS = RTS

Emulation of the 16550 UART loop back feature must be done by the Z180 MPU, except in the above conditions.

Bit 3 Out 2
This bit controls the tri-state on the HINTR pin if bits 2 and 1 are 10. Otherwise it can be read by the Z180 MPU.

Bits 2, 1, 0
These bits have no direct control of the 16550 MIMIC interface and the Z180 MPU must emulate the function if it is to be implemented.

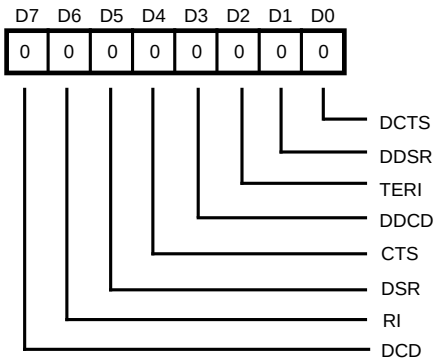


Figure 78. Modem Status Register
(PC Read Only, Address 06H)
(Z180 MPU Read/Write bits 7-4, Address xxF6H)

TIMING DIAGRAMS (Continued)

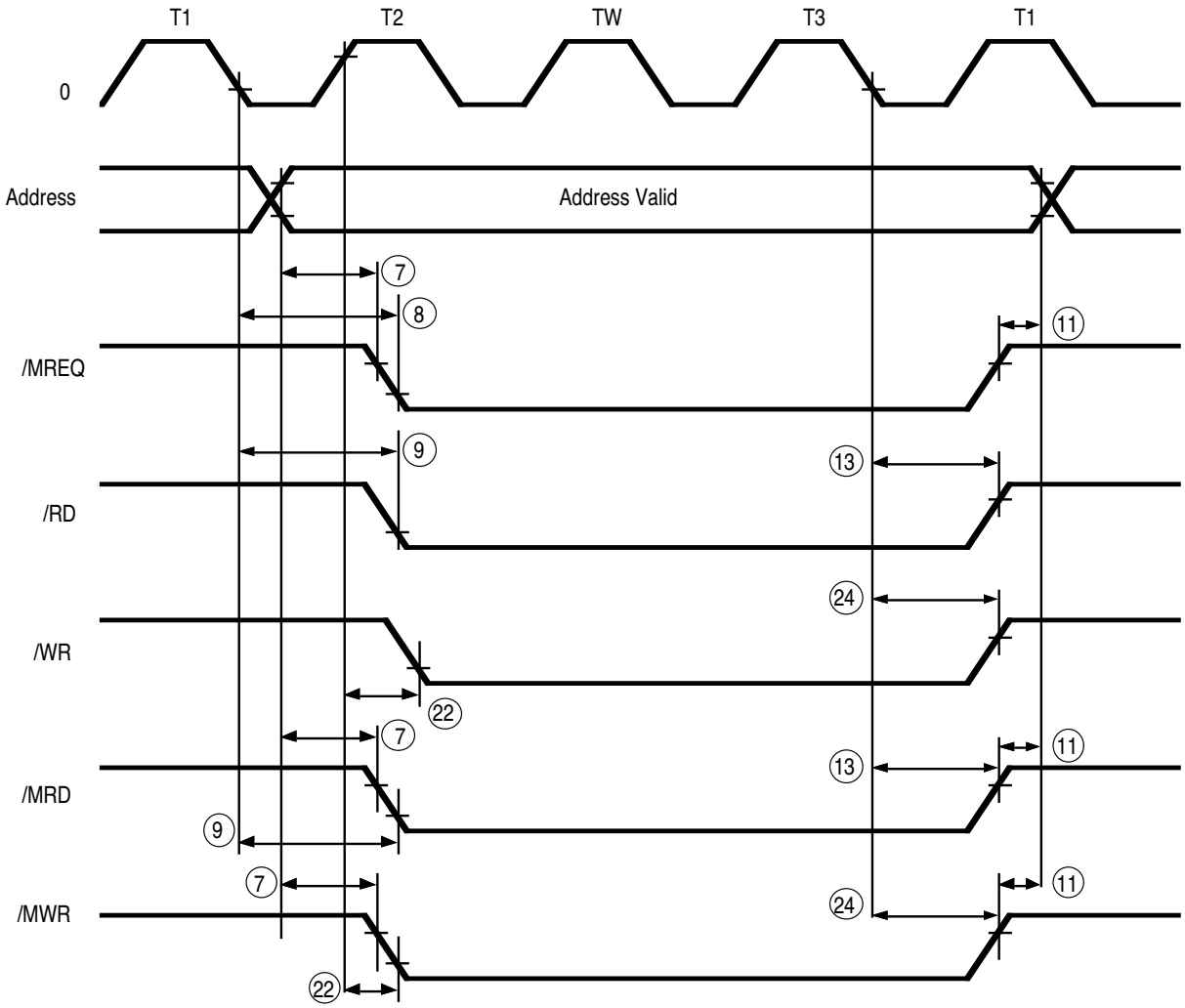


Figure 101. /MWR and /MRD Timing

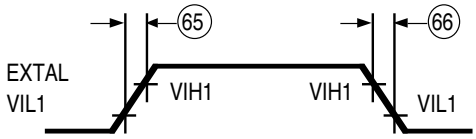


Figure 102. External Clock Rise Time and Fall Time

Figure 103. Input Rise and Fall Time
(Except EXTAL, /RESET)

ESCC Timing

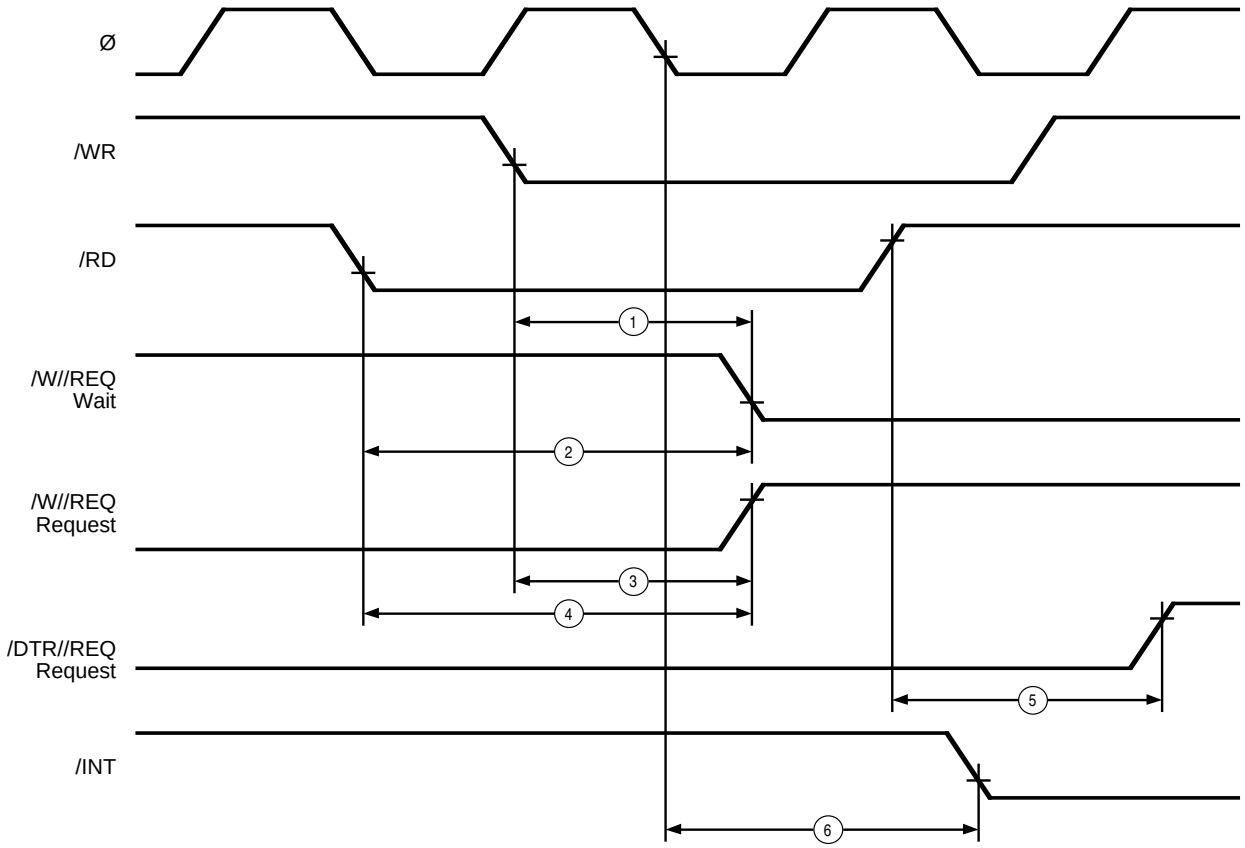


Figure 104. ESCC AC Parameter

Table B. ESCC Timing Parameters

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Unit
1	TdWR(W)	/WR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50	
3	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		65	
4	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		65	
5	TdRdr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay		TBD	
6	TdPC(INT)	Clock to /INT Valid Delay		160	

AC CHARACTERISTICS (Continued)

Z85230 System Timing Diagram

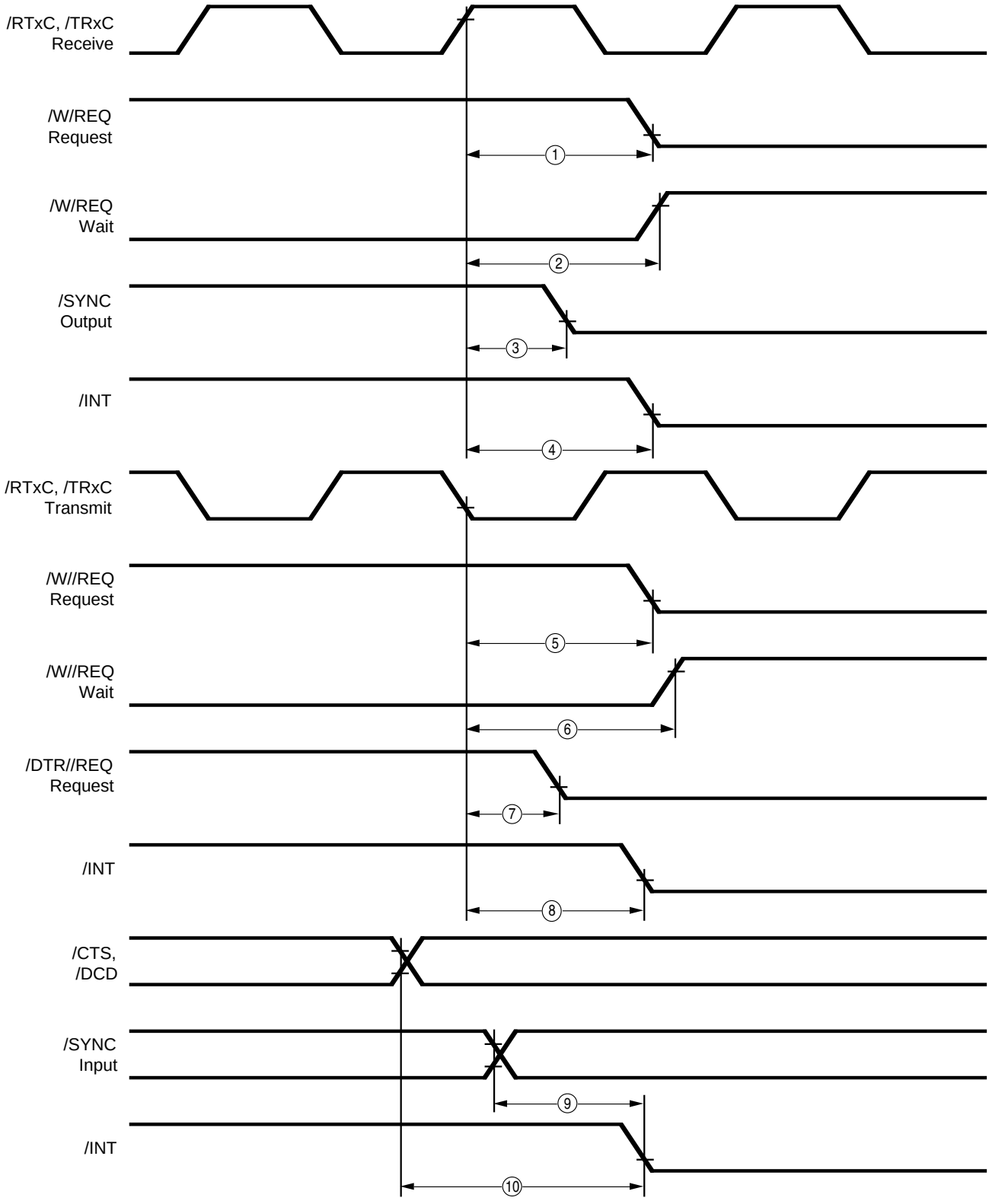


Figure 106. Z85230 System Timing

16550 MIMIC TIMING (Continued)

Table K. Interrupt Timing RCVR FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
14	tSINT	Delay from Stop to Set Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles
15	tRINT	Delay from /HRD (RD RBR or RD LSR) to Reset Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles

Note:
These AC parameter values are preliminary and are subject to change without notice.

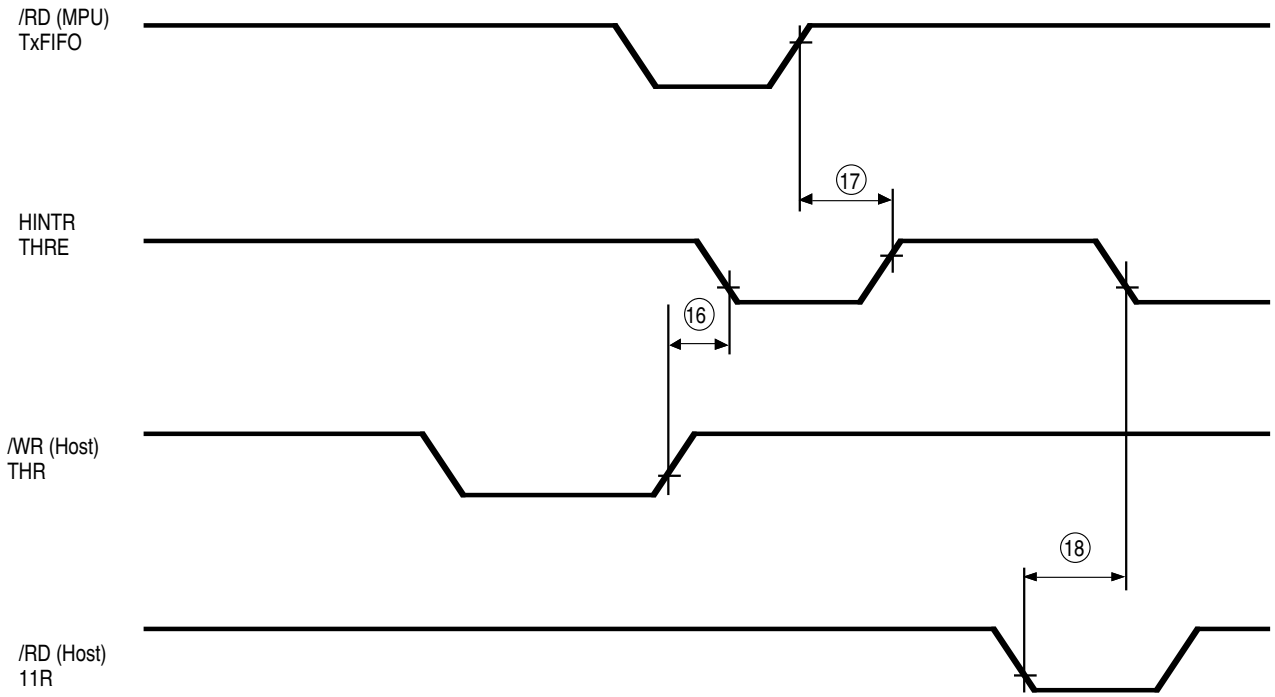


Figure 115. Interrupt Timing Transmitter FIFO

Table L. Interrupt Timing Transmitter FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
16	tHR	Delay from /WR (WR THR) to Reset Interrupt		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles
17	TSTI	Delay from Stop to Interrupt (THRE)	2 MPU Clock Cycles		2 MPU Clock Cycles	
18	TIR	Delay from /RD (RD IIR) to Reset Interrupt (THRIE)		75		75

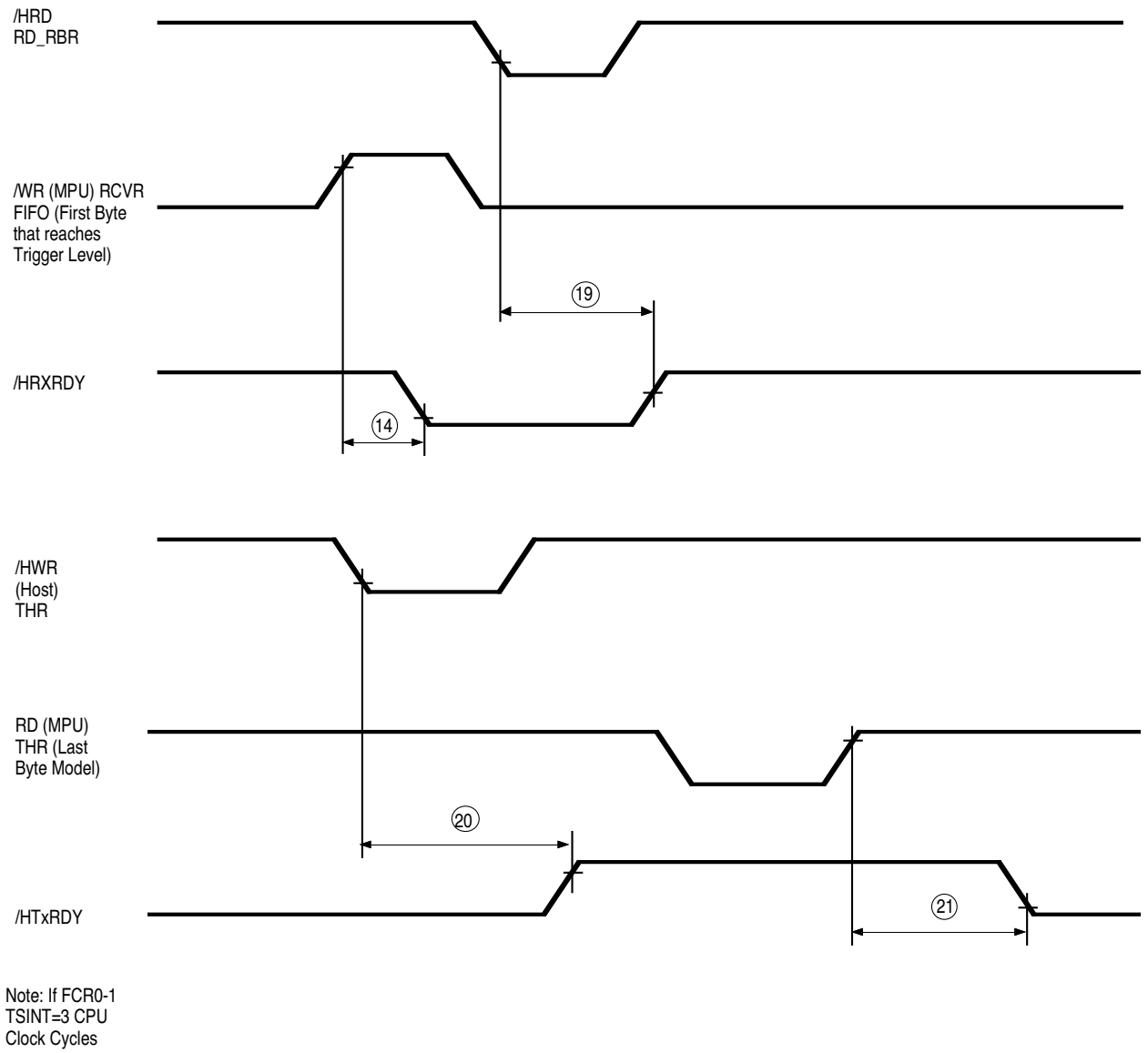


Figure 116 RCVR FIFO Bytes Other Than First