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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018233asg

Z180 MPU DMA SIGNALS

/TEND0. *Transfer End 0 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND0 is multiplexed with CKA1 on the CKA1//TEND0 pin.

/TEND1. *Transfer End 1 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND1 is multiplexed with the ESCC signal /RTSB and the 16550 MIMIC interface signal /HRxRDY on the /TEND1//RTSB//HRxRDY pin.

/DREQ0. *DMA request 0 (input, active Low).* /DREQ0 is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. /DREQ0 is multiplexed with CKA0 on the CKA0//DREQ0 pin.

/DREQ1. *DMA request 1 (input, active Low).* /DREQ1 is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

Z180™ MPU TIMER SIGNALS

$T_{OUT.}$ *Timer Out (output, active High).* T_{OUT} is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/T_{OUT} pin.

Z85230 ESCC™ SIGNALS

TxDA. *Transmit Data (output, active High).* This output signal transmits channel A's serial data at standard TTL levels. This output can be tri-stated during power down modes.

TxDB. *Transmit Data (output, active High).* This output signal transmits channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface /HDDIS signal on the TxDB//HDDIS pin.

RxDA. *Receive Data (inputs, active High).* These inputs receive channel A's serial data at standard TTL levels.

RxDB. *Receive Data (input, active High).* These inputs receive channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB/HA1 pin.

/TRxCA. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel A program control. /TRxCA may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/TRxCB. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel B program control. /TRxCB may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in output mode. In Z80182/Z8L182 mode 1 /TRxCB is multiplexed with the 16550 MIMIC interface HA0 input on the /TRxCB/HA0 pin.

/RTxCA. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel A program control. In channel A, /RTxCA may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCA pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

/RTxCB. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel B program control. In channel B, /RTxCB may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCB pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182/Z8L182 mode 1 the /RTxCB signal is multiplexed with 16550 MIMIC interface HA2 input on the /RTxCB/HA2 pin.

Z85230 ESCC SIGNALS (Continued)

/SYNCA, /SYNCB. *Synchronization (inputs/outputs, active Low).* These pins can act as either inputs, outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to /CTS and /DCD. In this mode, transitions on these lines affect the state of the Sync /Hunt status bits in Read Register 0, but have no other function. /SYNCA is also multiplexed with PC4 (parallel Port C, bit 4) on the /SYNCA/PC4 pin.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode /SYNC must be driven Low two receive clock cycles after the last bit in the sync character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.

In the Internal Synchronization mode, (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync character is recognized (regardless of the character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. In Z80182/Z8L182 mode 1 the /SYNCB signal is multiplexed with the 16550 MIMIC interface /HCS input on the /SYNCB //HCS pin.

/CTSA. *Clear To Send (input, active Low).* If this pin is programmed as auto enable, a Low on this input enables the channel A transmitter. If not programmed as auto enable, it may be used as a general-purpose input. The input is Schmitt-trigger buffered to accommodate slow rise-time input. The ESCC™ detects transitions on this input and can interrupt the Z180™ MPU on either logic level transitions. /CTSA is multiplexed with PC1 (parallel Port C, bit 1) on the /CTSA/PC1 pin.

/CTSB. *Clear To Send (input, active Low).* This pin is similar to /CTSA's functionality but is applicable to the channel B transmitter. In Z80182/Z8L182 mode, the /CTSB signal is multiplexed with the 16550 MIMIC interface /HWR input on the /CTSB //HWR pin.

/DCDA. *Data Carrier Detect (input, active Low).* This pin functions as receiver enables if it is programmed as an auto enable bit; otherwise, it may be used as a general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects transitions on this pin and can interrupt the Z180 MPU on either logic level transitions. /DCDA is also multiplexed with PC0 (parallel Port C, bit 0) on the /DCDA/PC0 pin.

/DCDB. *Data Carrier Detect (input, active Low).* This pin's functionality is similar to /DCDA but applicable to the channel B receiver. In Z80182/Z8L182 mode 1, /DCDB is multiplexed with the 16550 MIMIC interface /HRD input on the /DCDB//HRD pin.

/RTSA. *Request to Send (output, active Low).* When the Request to Send (RTS) bit in Write Register 5 channel A is set, the /RTSA signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with auto enables off, the /RTSA pin strictly follows the state of the RTS bit. The pin can be used as general-purpose output. /RTSA is multiplexed with PC2 (parallel Port C bit 2). This /RTSA or PC2 combination is pin multiplexed with /MWR (active when both the internal /MREQ and /WR are active) on the /MWR/PC2//RTSA pin. The default function of this pin on power-up is /MWR which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/RTSB. *Request to Send (output, active Low).* This pin is similar in functionality as /RTSA but is applicable on channel B. The /RTSB signal is multiplexed with the Z180 MPU /TEND1 signal and the 16550 MIMIC interface /HRxRDY signal on the /TEND1//RTSB//HRxRDY pin.

/DTR//REQA. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. /DTR//REQA is also multiplexed with PC3 (parallel Port C, bit 3) on the /DTR//REQA /PC3 pin.

/DTR//REQB. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. The /DTR//REQB signal is multiplexed with the Z180 MPU TxS signal and the 16550 MIMIC interface HINTR signal on the /TxS//DTR//REQB //HINTR pin.

/W//REQA. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This dual-purpose output can be programmed as Request (receive) lines for a DMA controller or as Wait lines to synchronize the Z180 MPU to the ESCC data rate. The reset state is Wait. The ESCC allows full duplex DMA transfers. /W//REQA is also multiplexed with PC5 (parallel Port C, bit 5) on the /W//REQA/PC5 pin.

Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 4.

Table 4. Multiplexed Port Pins

Port Mode Function	ASCI/ESCC Mode Function
PB7	RxS,/CTS1
PB6 Select with bit 6=1	RxA1
PB5 System Config Reg.	TxA1
PB4	RxA0
PB3	TxA0
PB2 Select with bit 5=1	/DCD0
PB1 System Config Reg.	/CTS0 (Note 1)
PB0	/RTS0
PC7	Always Reads /INT2 Ext. Status
PC6	Always Reads /INT1 Ext. Status
PC5	/W//REQA
PC4	/SYNCA
PC3 Select with bit 7=1	/DTR//REQA
PC2 System Config Reg.	/RTSA (Note 2)
PC1	/CTSA
PC0	/DCDA

Note 1:
When the Port function (PB1) is selected, the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

Note 2:
Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functions.

Table 5. Primary, Secondary and Tertiary Pin Functions

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
1	4	ST			
2	5	A0			
3	6	A1			
4	7	A2			
5	8	A3			
6	9	A4			
7	10	A5			
8	11	A6			
9	12	A7			
10	13	A8			
11	14	A9			
12	15	A10			
13	16	A11			
14	17	A12			
15	18	V_{SS}			
16	19	A13			
17	20	A14			
18	21	A15			
19	22	A16			
20	23	A17			
21	24	A18/T_{OUT}			
22	25	V_{DD}			
23	26	A19			
24	27	D0			
25	28	D1			
26	29	D2			
27	30	D3			
28	31	D4			
29	32	D5			
30	33	D6			
31	34	D7			
32	35	/RTS0	PB0		SYS CONF REG Bit 5
33	36	/CTS0	PB1		SYS CONF REG Bit 5
34	37	/DCD0	PB2		SYS CONF REG Bit 5
35	38	TxA0	PB3		SYS CONF REG Bit 5
36	39	RxA0	PB4		SYS CONF REG Bit 5
37	40	TxA1	PB5		SYS CONF REG Bit 6
38	41	RxA1	PB6		SYS CONF REG Bit 6
39	42	RxS//CTS1	PB7		SYS CONF REG Bit 6
40	43	CKA0//DREQ0			

MULTIPLEXED PIN DESCRIPTIONS (Continued)

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
41	44	V_{SS}			
42	45	CKA1//TEND0			
43	46	TxS	/DTR//REQB	HINTR	SYS CONF REG Bit 1,2
44	47	CKS	/W//REQB	/HTxRDY	SYS CONF REG Bit 1,2
45	48	/DREQ1			
46	49	V_{DD}			
47	50	/TEND1	/RTSB	/HRxRDY	SYS CONF REG Bit 1,2
48	51	/RAMCS			
49	52	/ROMCS			
50	53	EV1			
51	54	EV2			
52	55	PA0	HD0		SYS CONF REG Bit 1
53	56	PA1	HD1		SYS CONF REG Bit 1
54	57	PA2	HD2		SYS CONF REG Bit 1
55	58	PA3	HD3		SYS CONF REG Bit 1
56	59	PA4	HD4		SYS CONF REG Bit 1
57	60	PA5	HD5		SYS CONF REG Bit 1
58	61	PA6	HD6		SYS CONF REG Bit 1
59	62	PA7	HD7		SYS CONF REG Bit 1
60	63	/W//REQA	PC5		SYS CONF REG Bit 7
61	64	/DTR//REQA	PC3		SYS CONF REG Bit 7
62	65	/MWR	PC2	RTSA	SYS CONF REG Bit 7 *
63	66	/CTSA	PC1		SYS CONF REG Bit 7
64	67	/DCDA	PC0		SYS CONF REG Bit 7
65	68	/SYNCA	PC4		SYS CONF REG Bit 7
66	69	/RTxCA			
67	70	V_{SS}			
68	71	/IOCS	IEO		INT EDG/PIN REG Bit 2
69	72	IEI			
70	73	V_{DD}			

Z85230 ESCC™ BLOCK DIAGRAM

For a detailed description of the Z85230 ESCC, refer to the ESCC Technical Manual. The following figure is the block diagram of the discrete ESCC, which was integrated into the Z182. The /INT line is internally connected to "INTO of the Z182.

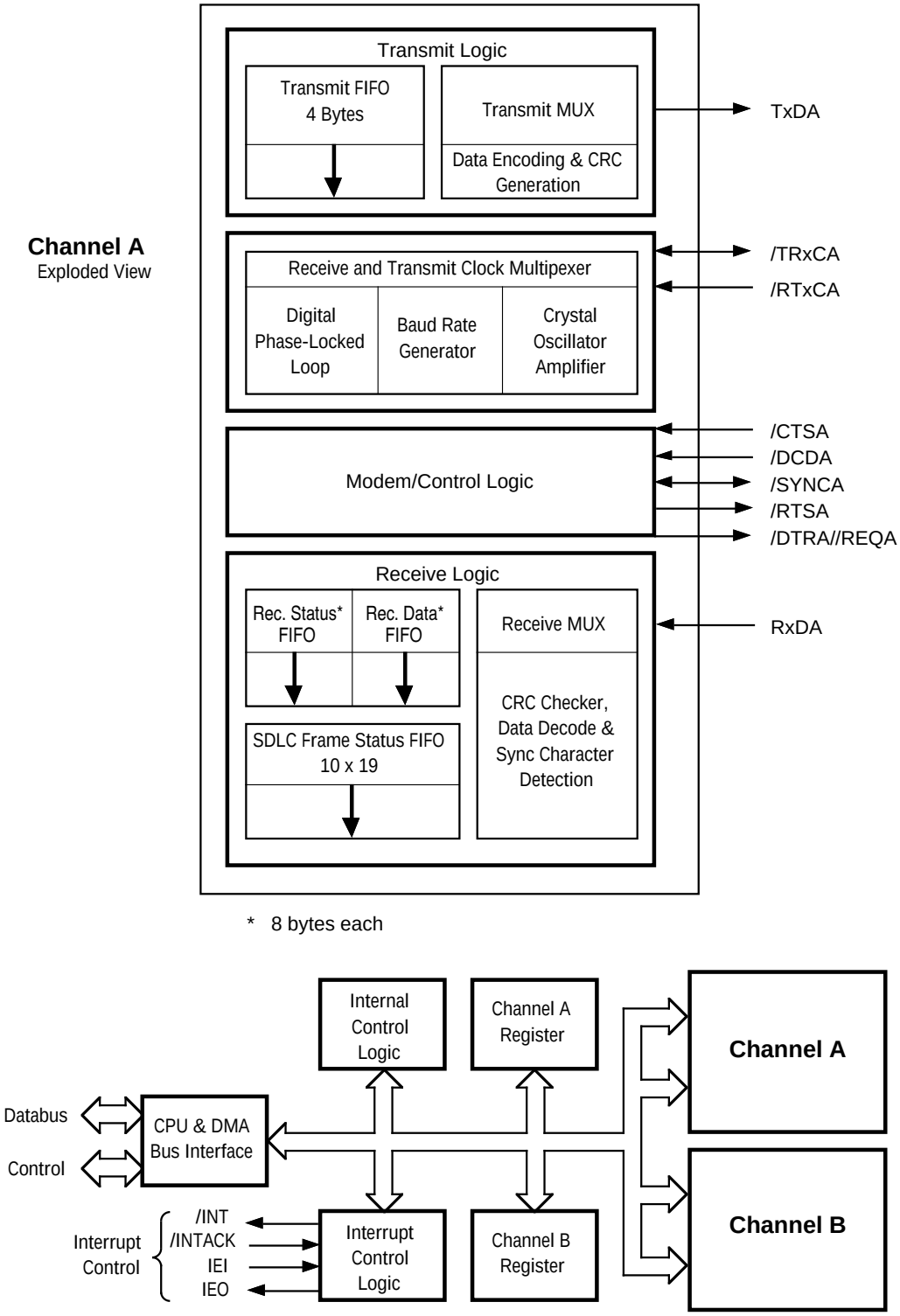


Figure 5. ESCC Block Diagram

PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only). The Ports are controlled through two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

PROGRAMMING

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for Z182 peripheral access. The full sixteen address lines are decoded for on-chip Z180 MPU access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers through the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated through the System Configuration Register and the Interrupt Edge/Pin MUX Register.

Table 7. Z80182/Z8L182 MPU Registers

Register Name	MPU Addr	PC Addr
Z80182/Z8L182 MPU Control Registers	0000H to 00x3FH (Relocatable to 0040H to 007FH or 0080H to 00BFH)	None

Note:
"x" indicates don't care condition

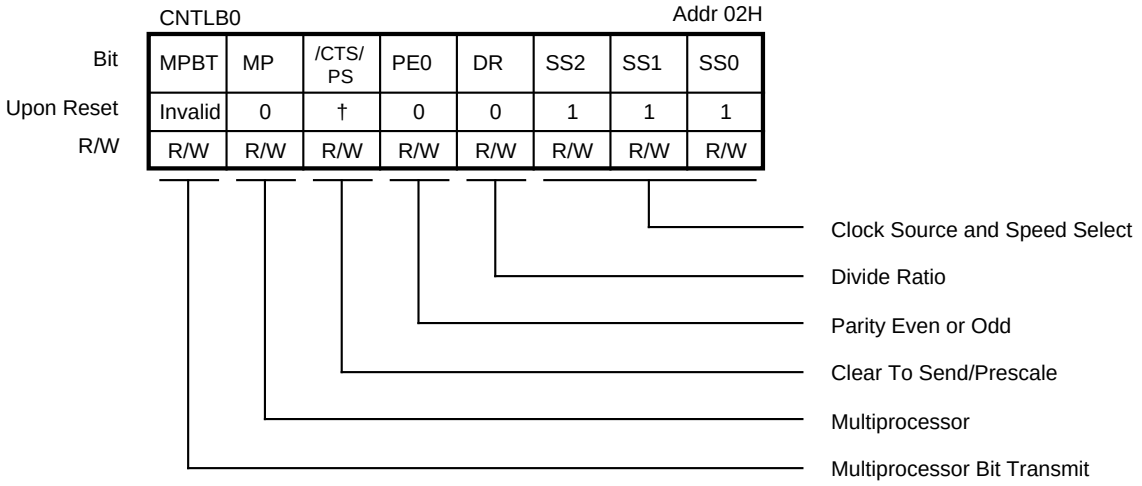
Table 8. Z80182/Z8L182 MIMIC Register MAP

Register Name	MPU Addr/Access		PC Addr/Access	
MMC MIMIC Master Control Register	xxFFH	R/W	None	
IUS/IP Interrupt Pending	xxFEH	R/Wb7	None	
IE Interrupt Enable	xxFDH	R/W	None	
IVEC Interrupt Vector	xxFCH	R/W	None	
TTCR Transmit Time Constant	xxFAH	R/W	None	
RTCR Receive Time Constant	xxFBH	R/W	None	
FSCR FIFO Status and Control	xxECH	R/W7-4	None	
RTTC Receive Timeout Time Constant	xxEAH	R/W	None	
TTTC Transmit Timeout Time Constant	xxEBH	R/W	None	
RBR Receive Buffer Register	xxF0H	W only	00H	DLAB=0 R only
THR Transmit Holding Register	xxF0H	R only	00H	DLAB=0 W only
IER Interrupt Enable Register	xxF1H	R only	01H	DLAB=0 R/W
IIR Interrupt Identification	None		02H	R only
FCR FIFO Control Register	xxE9H	R only	02H	W only
MM REGISTER	XXE9H	W only	None	
LCR Line Control Register	xxF3H	R only	03H	R/W
MCR Modem Control Register	xxF4H	R only	04H	R/W
LSR Line Status Register	xxF5H	R/Wb6432	05H	R only
MSR Modem Status Register	xxF6H	R/Wb7-4	06H	R only
SCR Scratch Register	xxF7H	R only	07H	R/W
DLL Divisor Latch (LSByte)	xxF8H	R only	00H	DLAB=1 R/W
DLM Divisor Latch (MSByte)	xxF9H	R only	01H	DLAB=1 R/W

PROGRAMMING (Continued)

Table 9. Z80182/Z8L182 ESCC, PIA and MISC Registers

Register Name	MPU Addr/Access		PC Addr/Access
WSG Chip Select Register	xxD8H	R/W	None
Z80182 Enhancements Register	xxD9H	R/W	None
PC Data Direction Register	xxDDH	R/W	None
PC Data Register	xxDEH	R/W	None
Interrupt Edge/Pin MUX Control	xxDFH	R/W	None
ESCC Chan A Control Register	xxE0H	R/W	None
ESCC Chan A Data Register	xxE1H	R/W	None
ESCC Chan B Control Register	xxE2H	R/W	None
ESCC Chan B Data Register	xxE3H	R/W	None
PB Data Direction Register	xxE4H	R/W	None
PB Data Register	xxE5H	R/W	None
RAMUBR RAM Upper Boundary Register	xxE6H	R/W	None
RAMLBR RAM Lower Boundary Register	xxE7H	R/W	None
ROM Address Boundary Register	xxE8H	R/W	None
PA Data Direction Register	xxEDH	R/W	None
PA Data Register	xxEEH	R/W	None
System Configuration Register	xxEFH	R/W	None



† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

General Divide Ratio	PS = 0 (Divide Ratio = 10)		PS = 1 (Divide Ratio = 30)	
SS, 2, 1, 0	**DR = 0 (x16)**	**DR = 1 (x64)**	**DR = 0 (x16)**	**DR = 1 (x64)**
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

Figure 11. ASCI Control Register B (Ch. 0)

ASCI CHANNELS CONTROL REGISTERS (Continued)

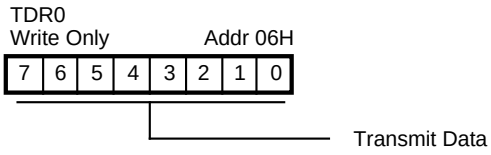


Figure 15. ASCI Transmit Data Register (Ch. 0)

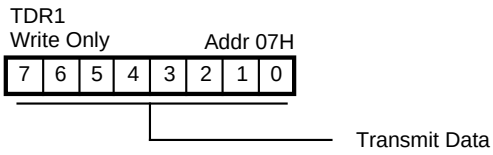


Figure 16. ASCI Transmit Data Register (Ch. 1)

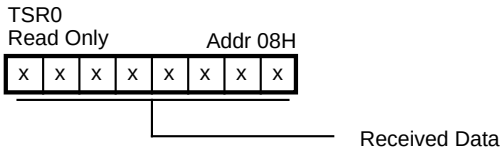


Figure 17. ASCI Receive Data Register (Ch. 0)

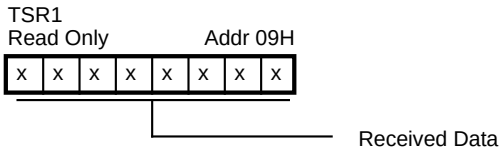


Figure 18. ASCI Receive Data Register (Ch. 1)

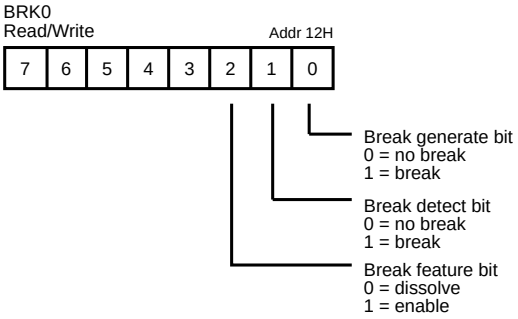


Figure 19. ASCI Break Control Register (Ch. 0)

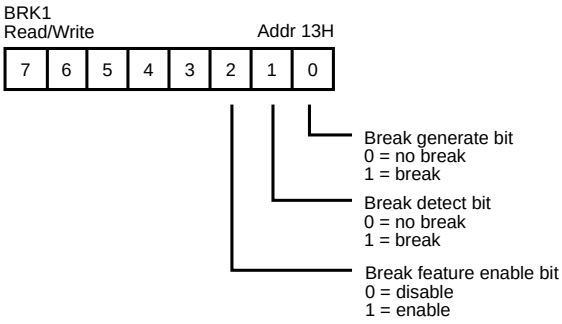
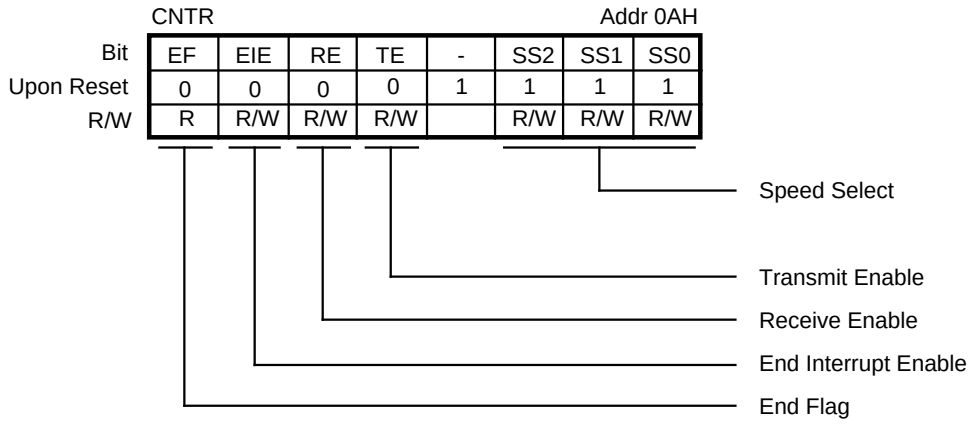


Figure 20. ASCI Break Control Register (Ch. 1)

CSI/O REGISTERS



SS2, 1, 0	Baud Rate
000	Ø ÷ 20
001	Ø ÷ 40
010	Ø ÷ 80
011	Ø ÷ 100

SS2, 1, 0	Baud Rate
100	Ø ÷ 320
101	Ø ÷ 640
110	Ø ÷ 1280
111	External Clock (Frequency < Ø ÷ 20)

Figure 21. CSI/O Control Register

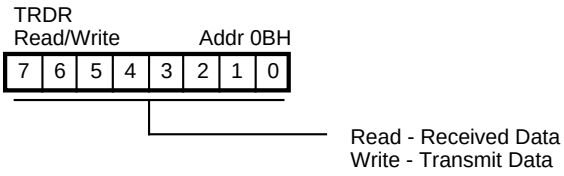


Figure 22. CSI/O Transmit/Receive Data Register

CONTROL REGISTERS (Continued)

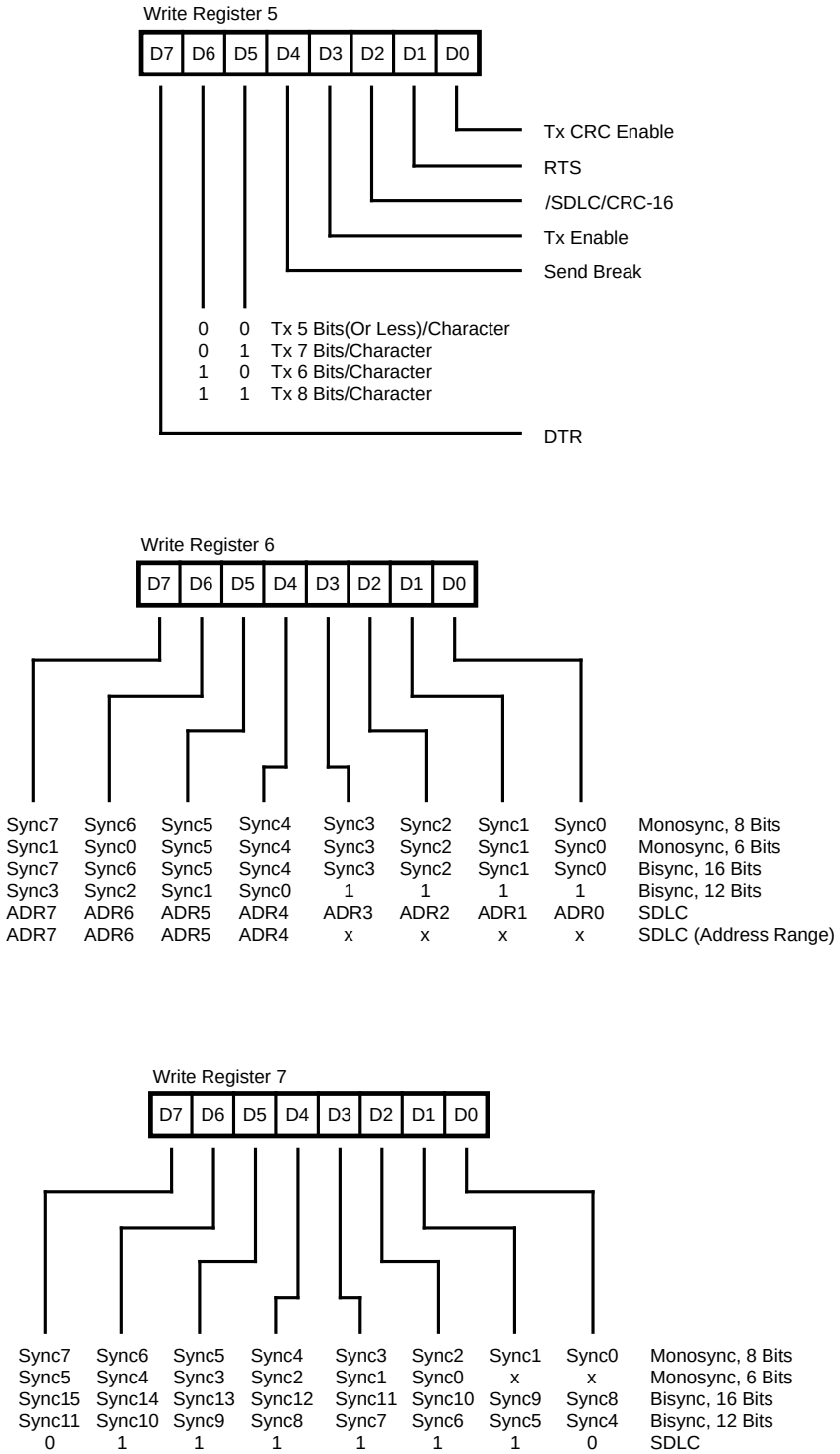


Figure 52. Write Register Bit Functions (Continued)

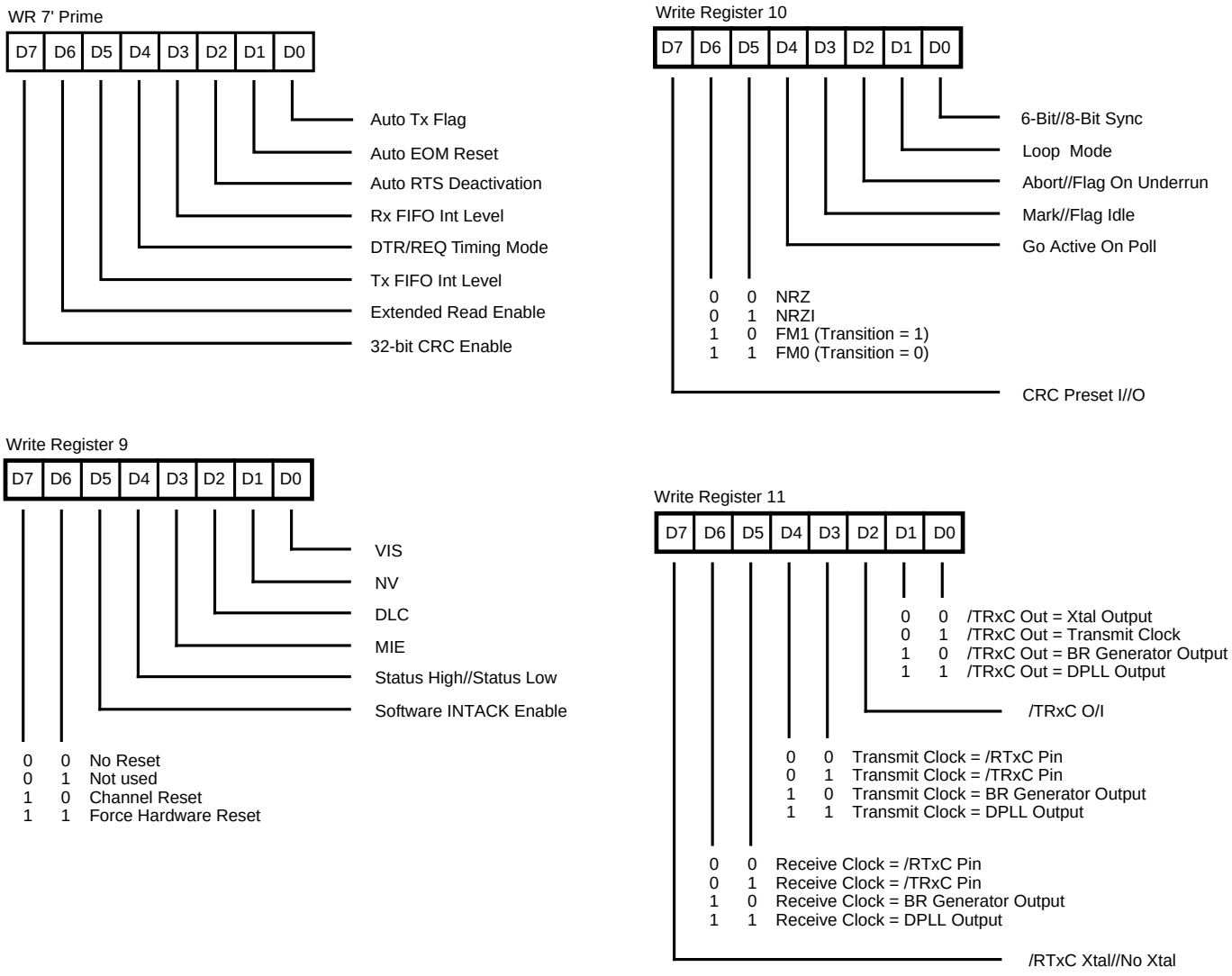


Figure 52. Write Register Bit Functions (Continued)

16550 MIMIC INTERFACE REGISTERS

MIMIC Master Control Register (MMC)

The 16550 MIMIC interface is controlled by the MMC register. Setting it allows for different modes of operation such as using the 8-bit counters, DMA accesses, and which IRQ structure is used with the PC/XT/AT.

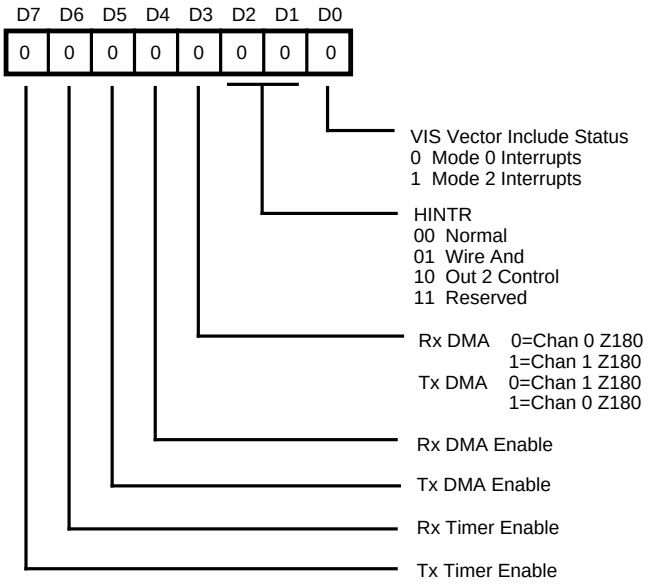


Figure 60. MIMIC Master Control Register
(Z180 MPU Read/Write, Address xxFFH)

Bit 7 Transmit Emulation Delay Counter Enable (Read/Write)
If bit 7 is set to 1, it enables the transmit delay timer. When the Z180 reads the Transmit Register, it loads the transmit delay timer from the Transmit Time Constant Register and enables the timer to count down to zero. This timer delays setting the Transmit Holding Register Empty (THRE) bit until the timer times out. If this bit is 0, then THRE is set immediately on a Z180 read of the Transmit Register. This bit also enables the emulation timer used in Transmitter Double Buffering.

Bit 6 Receive Emulation Delay Counter Enable (Read/Write)
If bit 6 is set to 1, it enables the receive delay timer. When the Z180 writes to the Receive Buffer, it loads the receive delay timer from the Receive Time Constant Register and enables the timer to count down to zero. This timer delays setting the Data Ready (DR) bit in the LSR until the timer times out. If this bit is 0 then DR is set immediately on a Z180 write to the Receive Buffer.

Both counters are single pass and stop on a count of Zero. Their purpose is to delay data transfer just as if the 16550 UART had to shift the data in and out. This is provided to alleviate any software problems a high speed continuous data transfer might cause to existing software. If this is not a concern, then data can be read and written as fast as the two machines can access the devices. In FIFO mode of operation , the timers are used to delay the status to the PC interface by the time required to actually shift the characters out, or in, if an actual UART were present.

Bit 5 Transmit DMA Enable (Read/Write)
If this bit is set to 1, it enables the Transmit DMA function.

Bit 4 Receive DMA Enable (Read/Write)
If this bit is set to 1, it enables the Receive DMA function.

Bit 3 Receive DMA Channel Select (Read/Write)
If bit 3 is set to 0, then Receive DMA transfer is done through Z180 DMA channel 0 and the Transmit DMA is done through DMA channel 1. If bit 3 is set to 1, then Receive DMA transfer is done through Z180 DMA channel 1 and the Transmit DMA is done through DMA channel 0.

Bits 2,1 Interrupt Select (Read/Write).
See Table 15.

Bit 0 Vector Include Status (Read/Write)
This bit is used to select the interrupt response mode of the Z180. A 0 in this bit enables Mode 0 interrupts; a 1 enables Mode 2 response.

Table 15. MIMIC Master Control Register Interrupt Select

Bit 2	Bit 1	HINTR Function
0	0	HINTR is set to normal 16550 MIMIC mode. A fully driven output is required when external priority arbiters are used.
0	1	A wired AND condition on the HINTR pin is possible to the PC/XT/AT. The interrupt is active High with only the pull-up of the HINTR pin driving; otherwise this pin is tri-state. Wired AND is needed when an external arbiter is not available.
1	0	HINTR is driven when out 2 of the Modem Control Register is 1. HINTR is tri-state when MCR out 2 is 0.
1	1	RESERVED

16550 MIMIC REGISTERS

The Z80182/Z8L182 contains the following set of registers for interfacing with the PC/XT/AT.

- Receive Buffer Register
- Transmit Holding Register
- Interrupt Enable Register
- Interrupt Identification Register
- FIFO Control Register
- Line Control Register
- Modem Control Register
- Line Status Register
- Modem Status Register
- Scratch Register
- Divisor Latch Least/Most Significant Bytes
- FIFO Control Register

These registers emulate the 16550 UART and enable the PC/XT/AT to interface with them as with an actual 16550 UART. This allows the Z80182/Z8L182 to be software compatible with existing modem software.

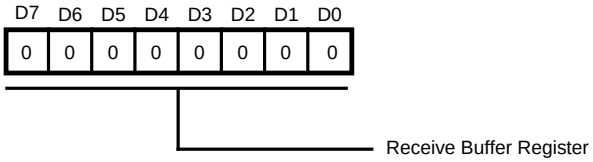


Figure 69. Receive Buffer Register
(PC Read Only, Address 00H, DLAB=0, R/W=Read)
(Z180™ MPU Write Only, Address XXF0H)

Receive Buffer Register

When the Z180 has assembled a byte of data to pass to the PC/XT/AT, it places it in the Receive Buffer Register. If the Received Data Available interrupt is enabled then an interrupt is generated for the PC/XT/AT and the Data Ready bit is set (if the Receive Timer is enabled, the interrupt and setting of the Data Ready bit is delayed until after the timer times out). Also the shadowed bits of the Line Status Register are transferred to their respective bits when the Z180 MPU writes to the Receive Buffer Register (See Line Status Register Bits 1, 2, 3 and 4). This allows a simultaneous setting of error bits when the data is written to the Receive Buffer Register. In FIFO, mode this address is used to read (PC) and write (Z180) the Receive FIFO.

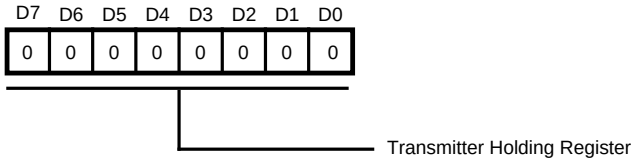


Figure 70. Transmit Holding Register
(PC Write Only, Address 00H, DLAB=0, R/W=Write)
(Z180 MPU Read Only, Address xxF0H)

Transmit Holding Register

When the PC/XT/AT writes to the Transmit Holding Register, the Z80182/Z8L182 responds by setting the appropriate bit in the IP register and by generating an interrupt to the Z180 MPU if it is enabled. When the Z180 MPU reads this register the Transmit Holding Register empty flag is set (if the transmitter timer is enabled , this bit is set after the timer times out). In FIFO mode of operation, this address is used to read (Z180) and write (PC) the Transmitter FIFO.

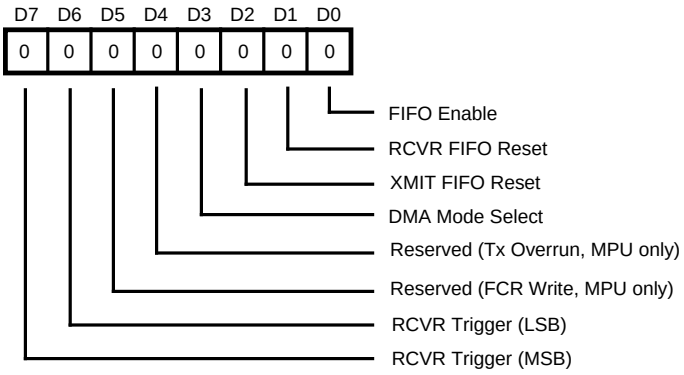


Figure 71. FIFO Control Register
(PC Write Only, Address 02H)
(Z180 MPU Read Only, Address xxE9H)

Z80182 ENHANCEMENTS REGISTER

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode
If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit is used to allow DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TxDA Tri-state
The TxDA pin can be tri-stated on assertion of the /HALT pin. This prevents the TxDA from driving and external device when /HALT output is used to force other devices into power-down modes. This feature is disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider
The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock will be Z180's PHI clock divided by two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5V or 10 MHz/3V, this bit should be set for ESCC divide-by-two mode.

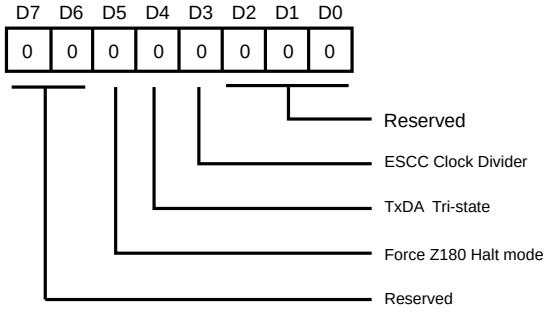


Figure 82. Z80182 Enhancements Register
(Z180 MPU Read/Write, Address xxD9H)

The data direction register determines which are inputs and outputs in the PC Data Register. When a bit is set to 1 the corresponding bit in the PC Data Register is an input. If the bit is 0, then the corresponding bit is an output.

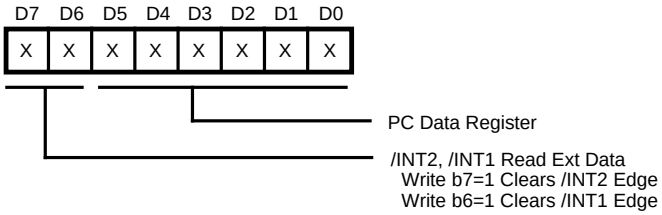


Figure 88. PC, Port C, Data Register
(Z180 MPU Read/Write, Address xxDEH)

When the Z180 MPU writes to the PC Data Register, the data is stored in the internal buffer. The values of Port C data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PC Data Register, the data on the external pins is returned.

Bits 6 and 7 serve the special function of reading the value of the external /INT2 and /INT1 lines. When operating either /INT2 or /INT1 in edge detection mode, the edge detect latch is reset by writing a 1 to bit 6 or 7 respectively. Writing a 0 has no effect. ***These latches should be reset at the end of an /INT1 or /INT2 interrupt service routine when using edge-triggered interrupt modes.***

16550 MIMIC INTERFACE DMA

The 16550 MIMIC is also able to do direct DMA with the PC/XT/AT. DMA is enabled by setting bits 3, 4 and 5 of the Master Control Register. DMA is accomplished by using the two DMA pins and the Transmitter Holding and Receive Data Registers.

If bit 5 is 1, the /HTxRDY pin is equal to the complement of the Transmit Holding Register Empty bit. If bit 5 is 1 and bit 3 is 0 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement of the Transmit Holding Register Empty Shadow bit. If bit 5 is 1 and bit 3 is 1 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Transmit Holding Register Empty Shadow bit.

If bit 4 is 1, then the /HRxRDY pin is equal to the complement of the Data Ready bit. If bit 4 is 1 and bit 3 is 0 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Data Ready Shadow bit. If bit 4 is 1 and bit 3 is 1 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement or the Data Ready Shadow bit.

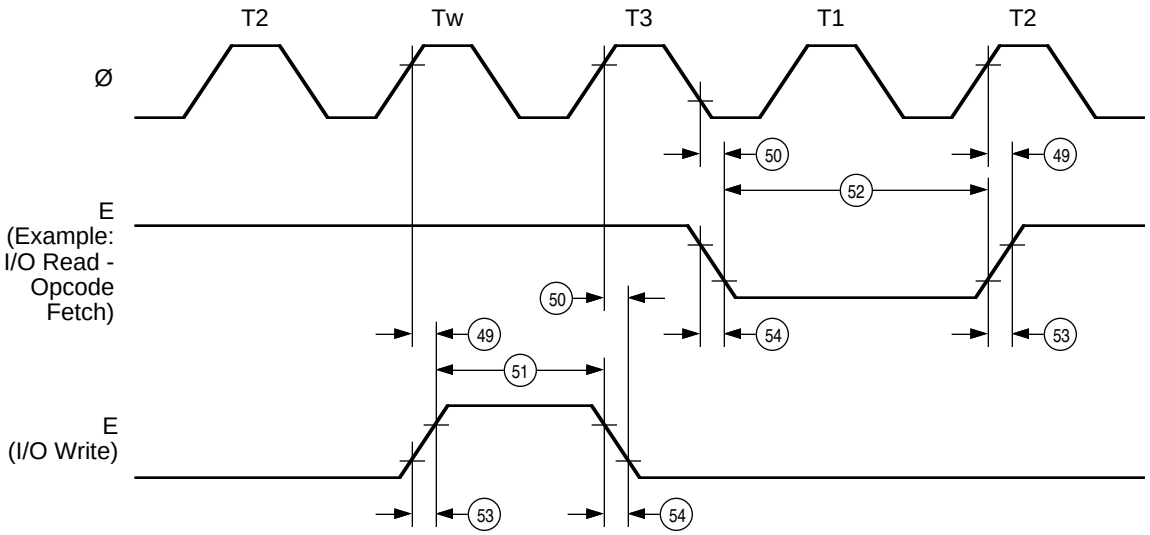


Figure 96. E Clock Timing
(Minimum timing example
of PWEL and PWEH)

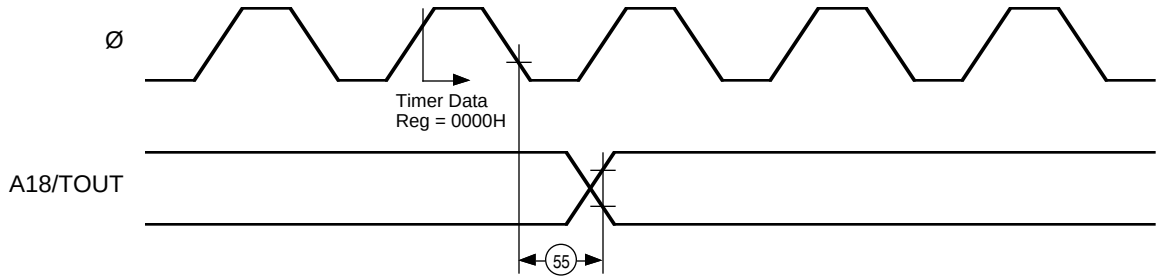


Figure 97. Timer Output Timing

AC CHARACTERISTICS (Continued)

Z85230 General Timing Diagram

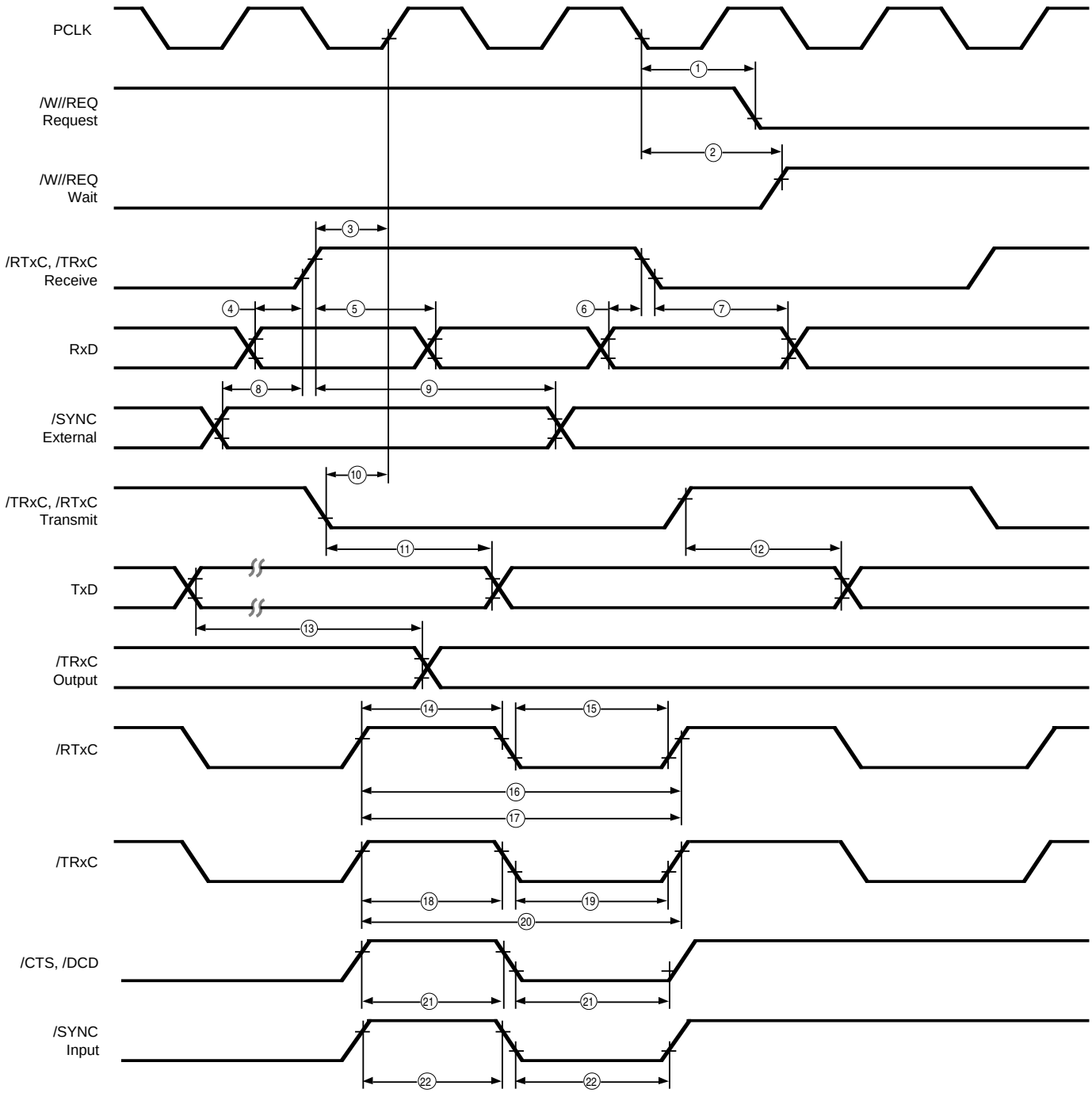
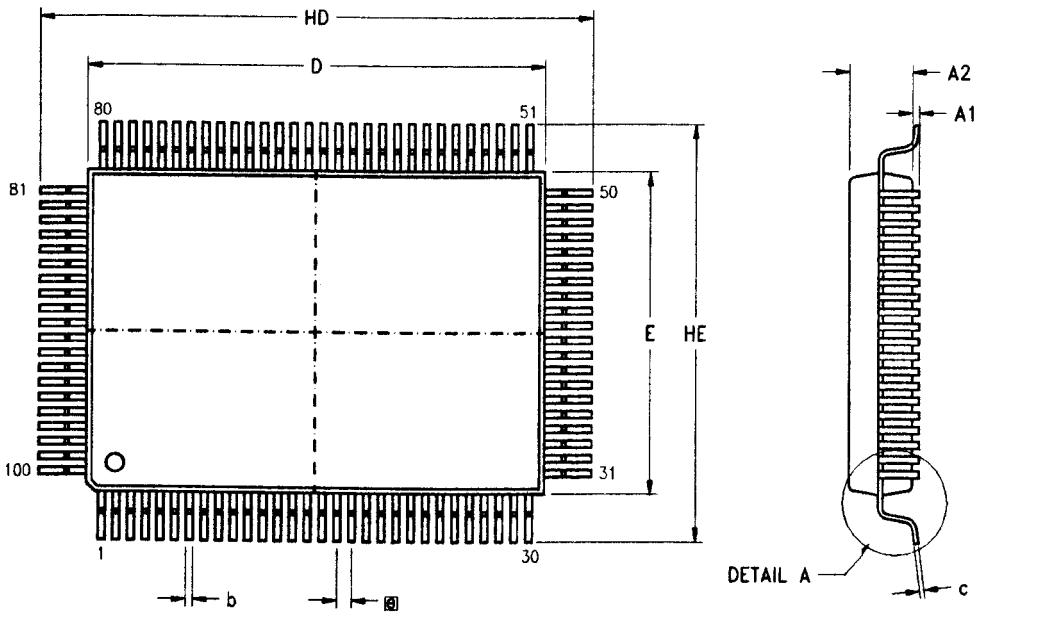
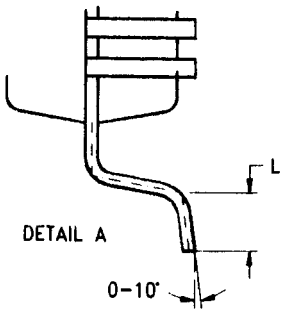


Figure 105. General Timing Diagram

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 TYP		.0256 TYP	
L	0.70	1.10	.028	.043



NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

100-Pin QFP Package Diagram