# Zilog - Z8018233ASG1838 Datasheet

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## Understanding Embedded - Microprocessors

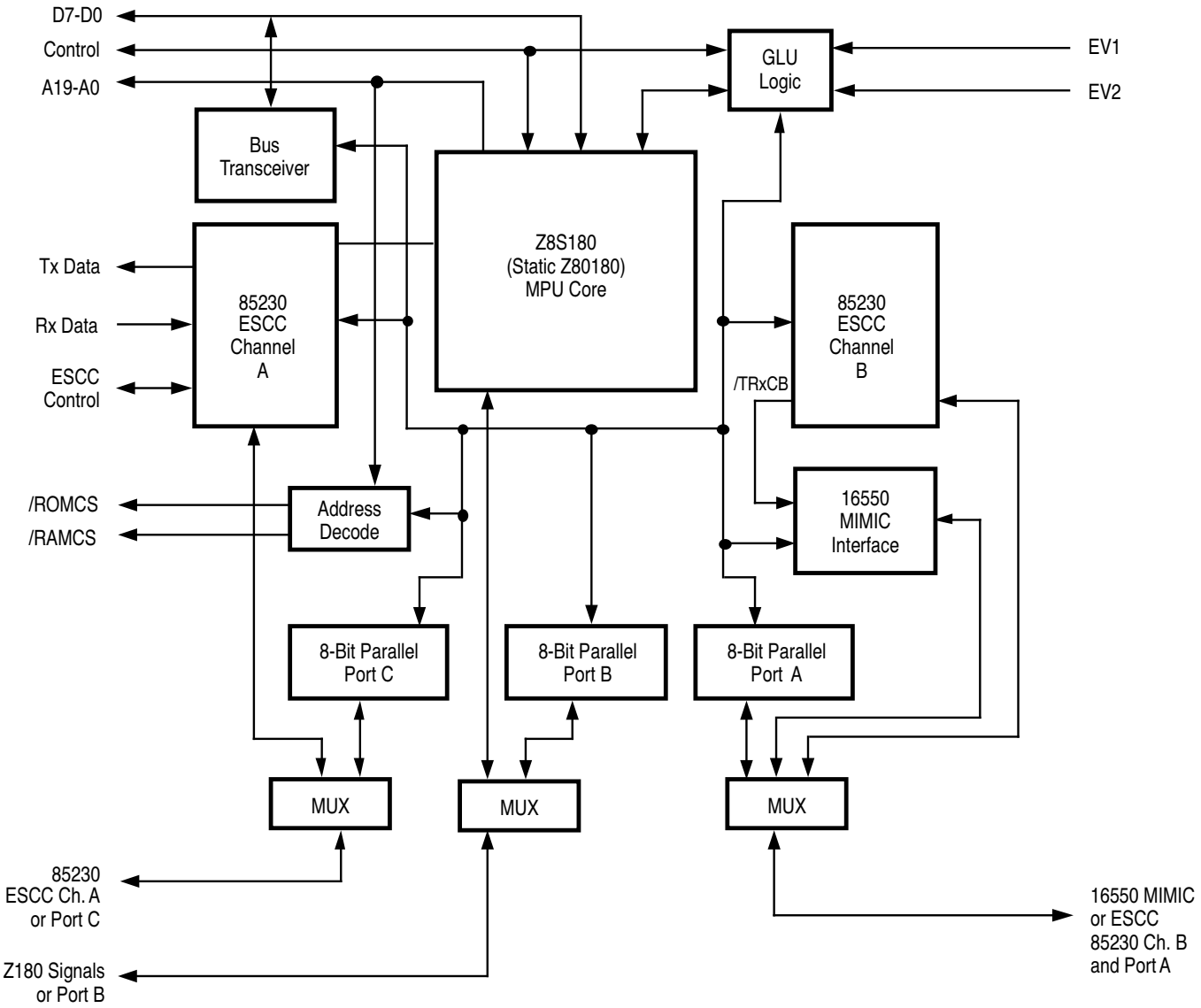
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z80180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 33MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8018233asg1838 |

## GENERAL DESCRIPTION (Continued)




**Note**: Conventional use of the term "MPU side" refers to all interface through the Z180 MPU core and "PC side" refers to all interface through the16550 MIMIC interface.

**Figure 1. Z80182/Z8L182 Functional Block Diagram**

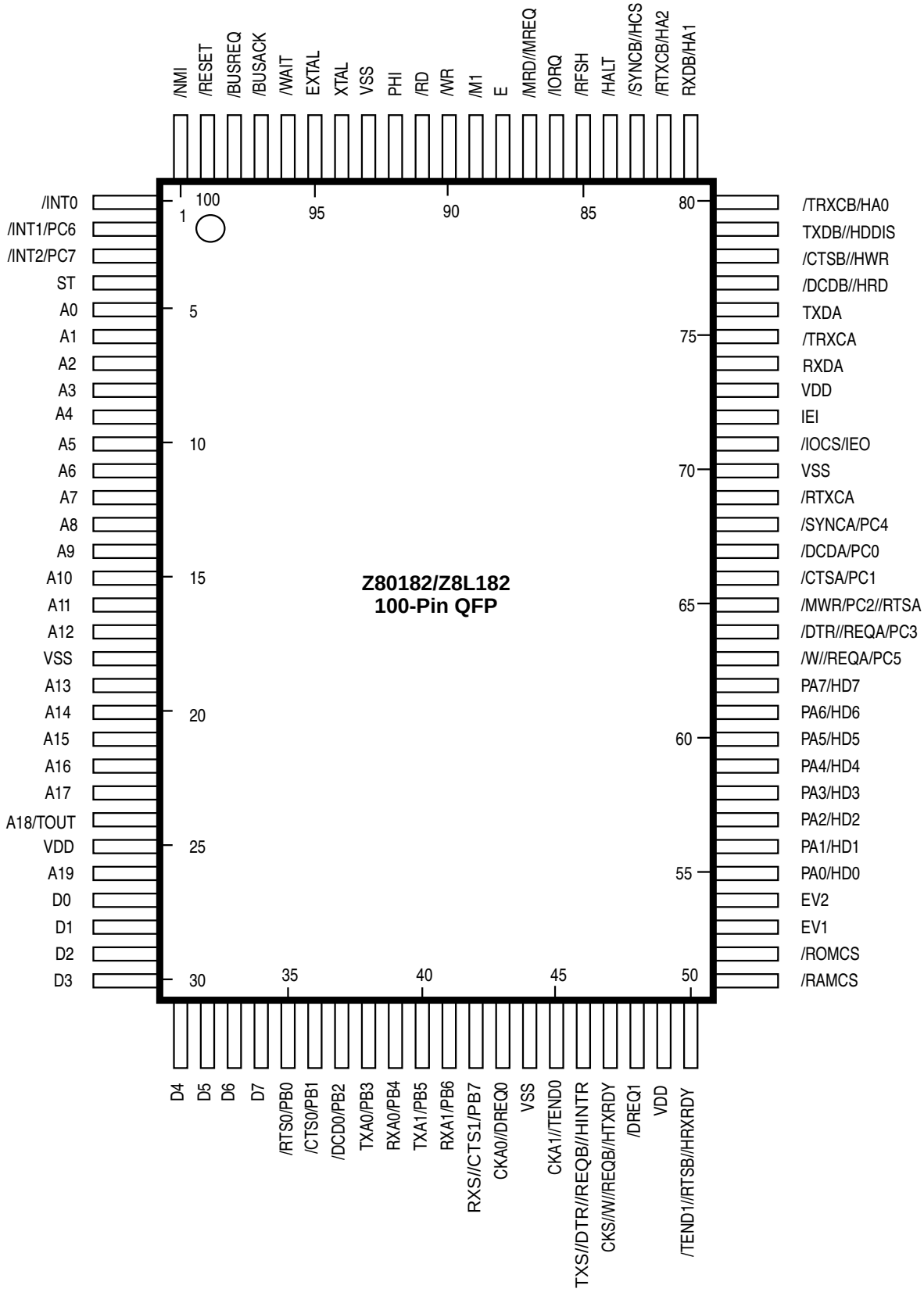



**Figure 2. Z80182/Z8L182 100-Pin QFP Pin Configuration**

## Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 4.

**Table 4. Multiplexed Port Pins**

| Port Mode Function | ASCI/ESCC Mode Function |
|---|---|
| PB7 | RxS,/CTS1 |
| PB6 Select with bit 6=1 | RxA1 |
| PB5 System Config Reg. | TxA1 |
| PB4 | RxA0 |
| PB3 | TxA0 |
| PB2 Select with bit 5=1 | /DCD0 |
| PB1 System Config Reg. | /CTS0 (Note 1) |
| PB0 | /RTS0 |
| PC7 | Always Reads /INT2 Ext. Status |
| PC6 | Always Reads /INT1 Ext. Status |
| PC5 | /W//REQA |
| PC4 | /SYNCA |
| PC3 Select with bit 7=1 | /DTR//REQA |
| PC2 System Config Reg. | /RTSA (Note 2) |
| PC1 | /CTSA |
| PC0 | /DCDA |

**Note 1:**
When the Port function (PB1) is selected, the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

**Note 2:**
Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functions.

## MULTIPLEXED PIN DESCRIPTIONS (Continued)

**Table 5. Primary, Secondary and Tertiary Pin Functions** (Continued)

| Pin Number VQFP | Pin Number QFP | 1st Function | 2nd Function | 3rd Function | MUX Control |
|---|---|---|---|---|---|
| 41 | 44 | $V_{SS}$ | | | |
| 42 | 45 | CKA1//TEND0 | | | |
| 43 | 46 | TxS | /DTR//REQB | HINTR | SYS CONF REG Bit 1,2 |
| 44 | 47 | CKS | /W//REQB | /HTxRDY | SYS CONF REG Bit 1,2 |
| 45 | 48 | /DREQ1 | | | |
| 46 | 49 | $V_{DD}$ | | | |
| 47 | 50 | /TEND1 | /RTSB | /HRxRDY | SYS CONF REG Bit 1,2 |
| 48 | 51 | /RAMCS | | | |
| 49 | 52 | /ROMCS | | | |
| 50 | 53 | EV1 | | | |
| 51 | 54 | EV2 | | | |
| 52 | 55 | PA0 | HD0 | | SYS CONF REG Bit 1 |
| 53 | 56 | PA1 | HD1 | | SYS CONF REG Bit 1 |
| 54 | 57 | PA2 | HD2 | | SYS CONF REG Bit 1 |
| 55 | 58 | PA3 | HD3 | | SYS CONF REG Bit 1 |
| 56 | 59 | PA4 | HD4 | | SYS CONF REG Bit 1 |
| 57 | 60 | PA5 | HD5 | | SYS CONF REG Bit 1 |
| 58 | 61 | PA6 | HD6 | | SYS CONF REG Bit 1 |
| 59 | 62 | PA7 | HD7 | | SYS CONF REG Bit 1 |
| 60 | 63 | /W//REQA | PC5 | | SYS CONF REG Bit 7 |
| 61 | 64 | /DTR//REQA | PC3 | | SYS CONF REG Bit 7 |
| 62 | 65 | /MWR | PC2 | RTSA | SYS CONF REG Bit 7 * |
| 63 | 66 | /CTSA | PC1 | | SYS CONF REG Bit 7 |
| 64 | 67 | /DCDA | PC0 | | SYS CONF REG Bit 7 |
| 65 | 68 | /SYNCA | PC4 | | SYS CONF REG Bit 7 |
| 66 | 69 | /RTxCA | | | |
| 67 | 70 | $V_{SS}$ | | | |
| 68 | 71 | /IOCS | IEO | | INT EDG/PIN REG Bit 2 |
| 69 | 72 | IEI | | | |
| 70 | 73 | $V_{DD}$ | | | |

## Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

## Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100% software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

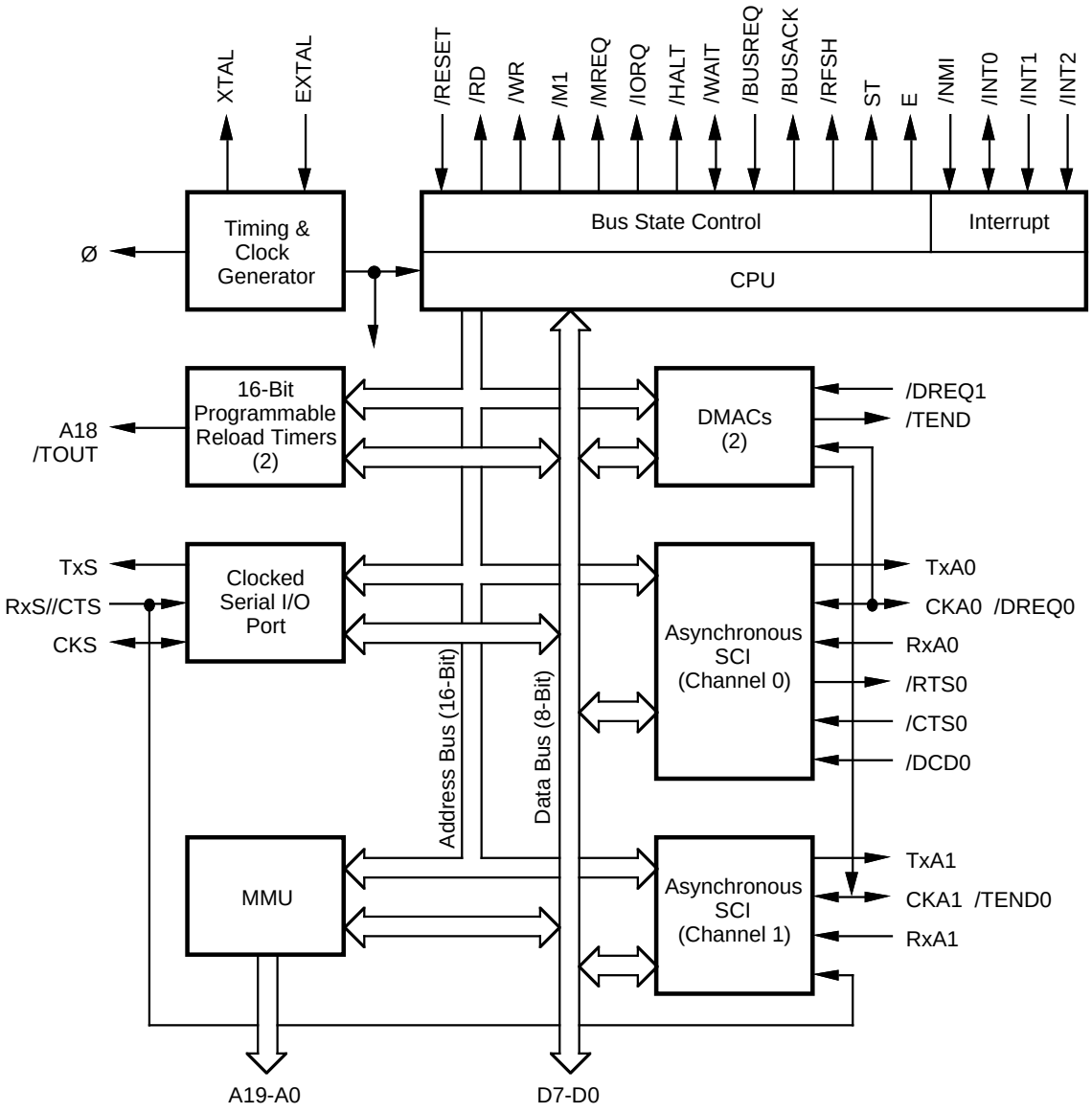



**Figure 4. S180 MPU Block Diagram of Z182**

The following features are common to both the ESCC and the CMOS SCC:

- Two independent full-duplex channels
- Synchronous/Isochronous data rates:
  - Up to 1/4 of the PCLK using external clock source
  - Up to 5 Mbits/sec at 20 MHz PCLK (ESCC).
- Asynchronous capabilities
  - 5, 6, 7 or 8 bits/character (capable of handling 4 bits/character or less)
  - 1, 1.5, or 2 stop bits
  - Odd or even parity
  - Times 1, 16, 32 or 64 clock modes
  - Break generation and detection
  - Parity, overrun and framing error detection
- Byte oriented synchronous capabilities:
  - Internal or external character synchronization
  - One or two sync characters (6 or 8 bits/sync character) in separate registers
  - Automatic Cyclic Redundancy Check (CRC) generation/detection
- SDLC/HDLC capabilities:
  - Abort sequence generation and checking
  - Automatic zero insertion and detection
  - Automatic flag insertion between messages
  - Address field recognition
  - I-field residue handling
  - CRC generation/detection
  - SDLC loop mode with EOP recognition/loop entry and exit
- NRZ, NRZI or FM encoding/decoding. Manchester Code Decoding (Encoding with External Logic).
- Baud Rate Generator in each Channel
- Digital Phase-Locked Loop (DPLL) for Clock Recovery
- Crystal Oscillator

The following features are implemented in the ESCC™ for the Z80182/Z8L182 only:

- New 32-bit CRC-32 (Ethernet Polynomial)
- ESCC Programmable Clock
  - programmed to be equal to system clock divided by one or two
  - programmed by Z80182 Enhancement Register

**Note:** The ESCC™ programmable clock must be programmed to divide-by-two mode when operating above the following conditions:

– PHI > 20 MHz at 5.0V

– PHI > 10 MHz at 3.0V

## 16550 MIMIC INTERFACE FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has a 16550 MIMIC interface that allows it to mimic the 16550 device. It has all the interface pins necessary to connect to the PC/XT/AT bus. It contains the complete register set of the part with the same interrupt structure. The data path allows parallel transfer of data to and from the register set by the internal Z80180 of the Z80182/Z8L182. There is no shift register associated with the mimic of the 16550 UART. This interface saves the application from doing a serial transfer before performing data compression or error correction on the data.

Control of the register set is maintained by six priority encoded interrupts to the Z80182/Z8L182. When the PC/XT/AT writes to THR, MCR, LCR, DLL, DLM, FCR or reads the RBR, an interrupt to the Z80182/Z8L182 is generated. Each interrupt can be individually masked off or all interrupts can be disabled by writing a single bit. Both mode 0 and mode 2 interrupts are supported by the 16550 MIMIC interface.

Two eight-bit timers are also available to control the data transfer rate of the 16550 MIMIC interface. Their input is tied to the ESCC channel B divide clock, so a down count of 24 bits is possible. An additional two eight bit timers are available for programming the FIFO timeout feature (Four Character Time Emulation) for both Receive and Transmit FIFO's.

The 16550 MIMIC interface supports the PC/XT/AT interrupt structure as well as an additional mode that allows for a wired Logic AND interrupt structure.

The 16550 MIMIC interface is also capable of high speed parallel DMA transfers by using two control lines and the transmit and receive registers of the 16550 MIMIC interface.

All registers of the 16550 MIMIC interface are accessible in any page of I/O space since only the lowest eight address lines are decoded. See Figure 6 for a block diagram of the 16550 MIMIC interface.

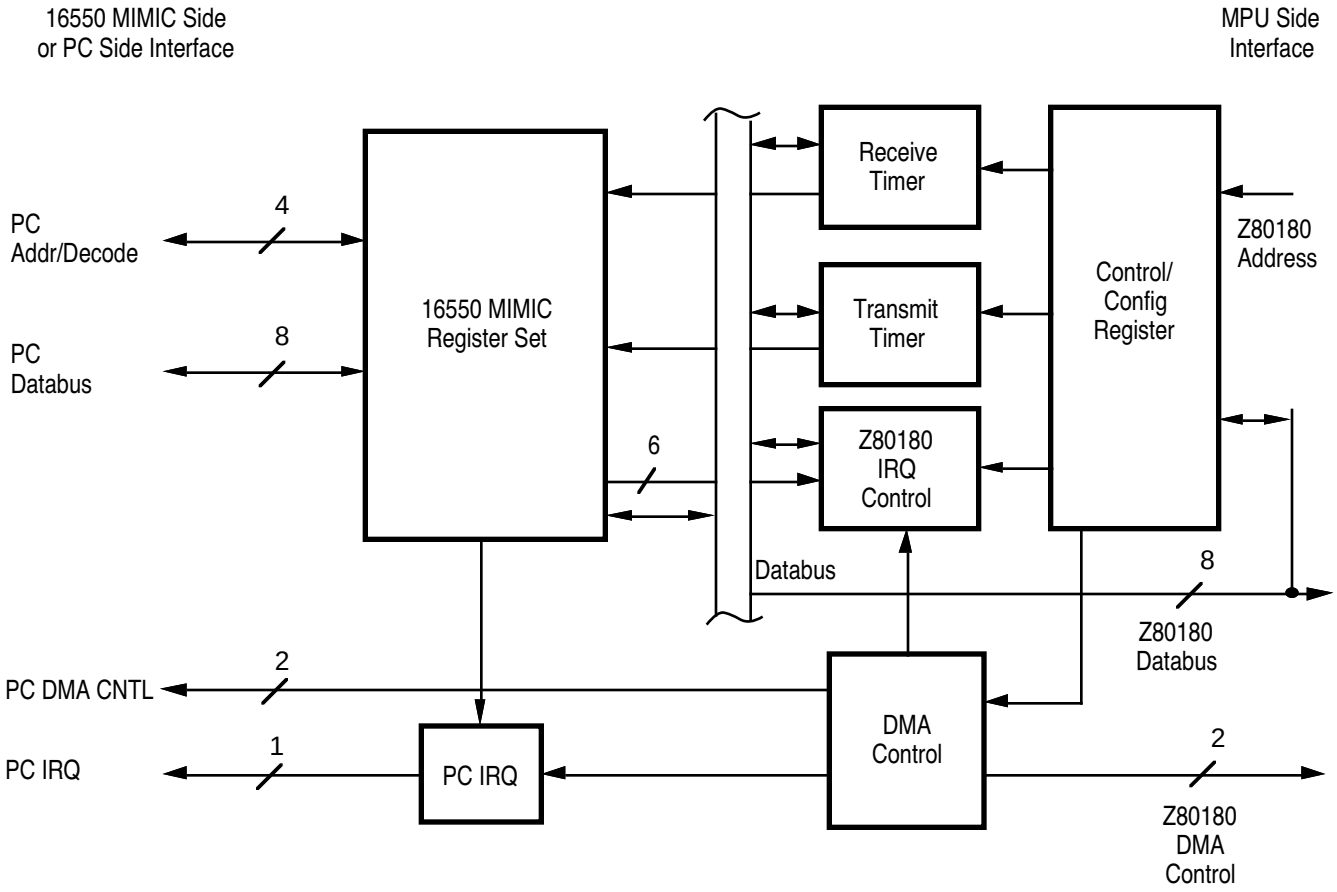



**Figure 6. 16550 MIMIC Block Diagram**

## ASCI CHANNELS CONTROL REGISTERS (Continued)

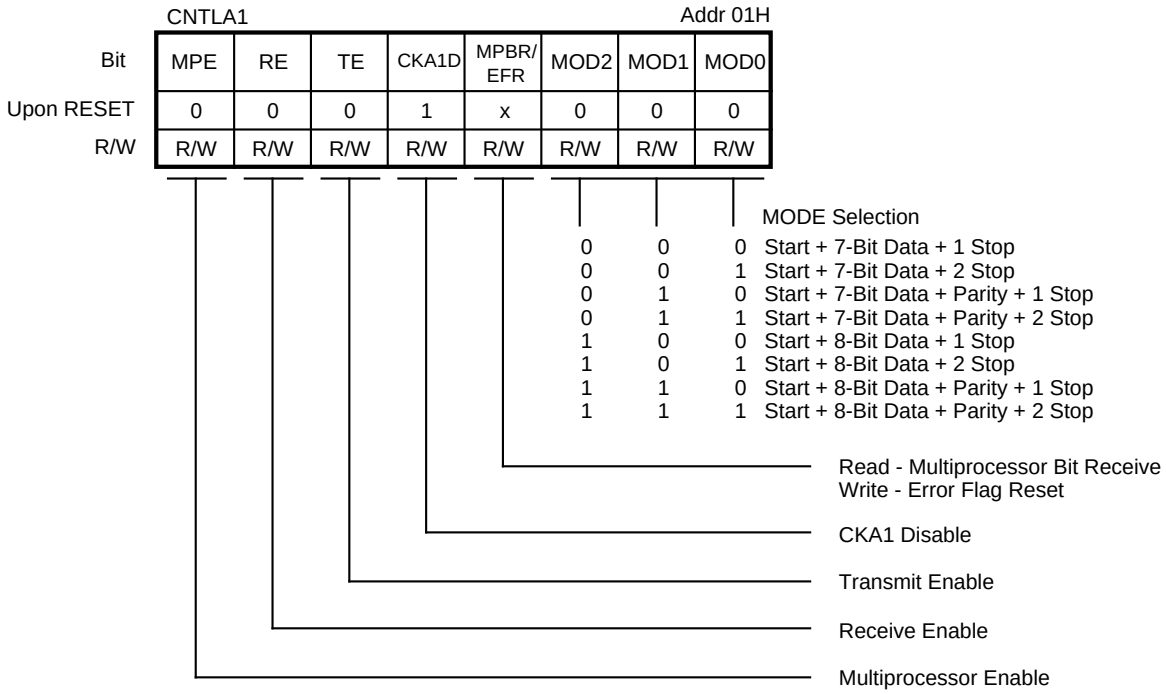



**Figure 10b. ASCI Control Register A** (Ch. 1)

## SYSTEM CONTROL REGISTERS

IL — Addr 33H

| Bit | IL7 | IL6 | IL5 | - | - | - | - | - |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | | | | | |

Interrupt Vector Low

**Figure 46. Interrupt Vector Low Register**

ITC — Addr 34H

| Bit | TRAP | UFO | - | - | - | ITE2 | ITE1 | ITE0 |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| R/W | R/W | R | | | | R/W | R/W | R/W |

/INT Enable 2, 1, 0
Undefined Fetch Object
TRAP

**Figure 47. INT/TRAP Control Register**

RCR — Addr 36H

| Bit | REFE | REFW | - | - | - | - | CYC1 | CYC0 |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| R/W | R/W | R/W | | | | | R/W | R/W |

Cycle Select
Refresh Wait State
Refresh Enable

| CYC1, 0 | Interval of Refresh Cycle |
|---|---|
| 00 | 10 states |
| 01 | 20 states |
| 10 | 40 states |
| 11 | 80 states |

**Figure 48. Refresh Control Register**

## ADDITIONAL FEATURES ON THE Z182 MPU

The following is a detailed description of the enhancements to the Z8S180 from the standard Z80180 in the areas of STANDBY, IDLE, and STANDBY-QUICK RECOVERY modes.

### Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce the current consumption. The Z8S180 has added two additional power-down modes, STANDBY and IDLE, to reduce the current consumption even further. The differences among these power-down modes are summarized in Table 10.

**Table 10. Power Down Modes**

| Power-Down Modes | CPU Core | On-Chip I/O | OSC. | CLKOUT | Recovery Source | Recovery Time (Minimum) |
|---|---|---|---|---|---|---|
| SLEEP | Stop | Running | Running | Running | RESET, Interrupts | 1.5 Clock |
| I/O STOP | Running | Stop | Running | Running | By Programming | - |
| SYSTEM STOP | Stop | Stop | Running | Running | RESET, Interrupts | 1.5 Clock |
| IDLE† | Stop | Stop | Running | Stop | RESET, Interrupts, BUSREQ | 8 +1.5 Clock |
| STANDBY† | Stop | Stop | Stop | Stop | RESET, Interrupts, BUSREQ | $2^{17}$ +1.5 Clock (Normal Recovery)<br>$2^{6}$ +1.5 Clock (Quick Recovery) |

**Notes:**
† IDLE and STANDBY modes are only offered in Z8S180. Note that the minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.

### STANDBY Mode

The Z8S180 has been designed to save power. Two low-power programmable power-down modes have been added; STANDBY mode and IDLE mode. The STANDBY/IDLE mode is selected by multiplexing D6 and D3 of the CPU Control Register (CCR, I/O Address = 1FH). To enter STANDBY mode:

1. Set D6 and D3 to 1 and 0, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY mode, it behaves similar to the SYSTEM STOP mode which currently exists on the Z80180, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to typically 50 μA..

Since the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter has been added in the Z8S180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down $2^{17}$ counts before acknowledgment is sent to the interrupt source.

The recovery source needs to remain asserted for duration of the $2^{17}$ count, otherwise standby will be resumed.

The following is a description of how the part exits STANDBY for different interrupts and modes of operation.

### STANDBY Mode Exit with /RESET

The /RESET input needs to be asserted for a duration long enough for the crystal oscillator to stabilize and then exit from the STANDBY mode. When /RESET is de-asserted, it goes through the normal reset timing to start instruction execution at address (logical and physical) 0000H.

The clocking is resumed within the Z8S180 and at the system clock output after /RESET is asserted when the crystal oscillator is restarted, but not yet stabilized.

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is stopped completely. IDLE mode is exited in a similar way as STANDBY mode, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS, except that the $2^{17}$ bit wake-up timer is bypassed; all control signals are asserted eight clock cycles after the exit conditions are gathered.

## STANDBY-QUICK RECOVERY Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from $2^{17}$ clock cycles (6.5 ms at 20 MHz) to $2^{6}$ clock cycles (3.2 µs at 20 MHz). This feature can only be used when providing an oscillator as clock source.

To enter STANDBY-QUICK RECOVERY mode:

1. Set D6 and D3 to 1 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS; the clock and other control signals are recovered sooner than the STANDBY mode.

**Note:** If STANDBY-QUICK RECOVERY is enabled, the user must make sure stable oscillation is obtained within 64 clock cycles.

## CPU Control Register

The Z8S180 has an additional register which allows the programmer to select options that directly affect the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU Control Register (CCR) allows the programmer to change the divide-by-two internal clock to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 can reduce the output drivers on selected groups of pins to 25% of normal pad driver capability which minimizes the EMI noise generated by the part.

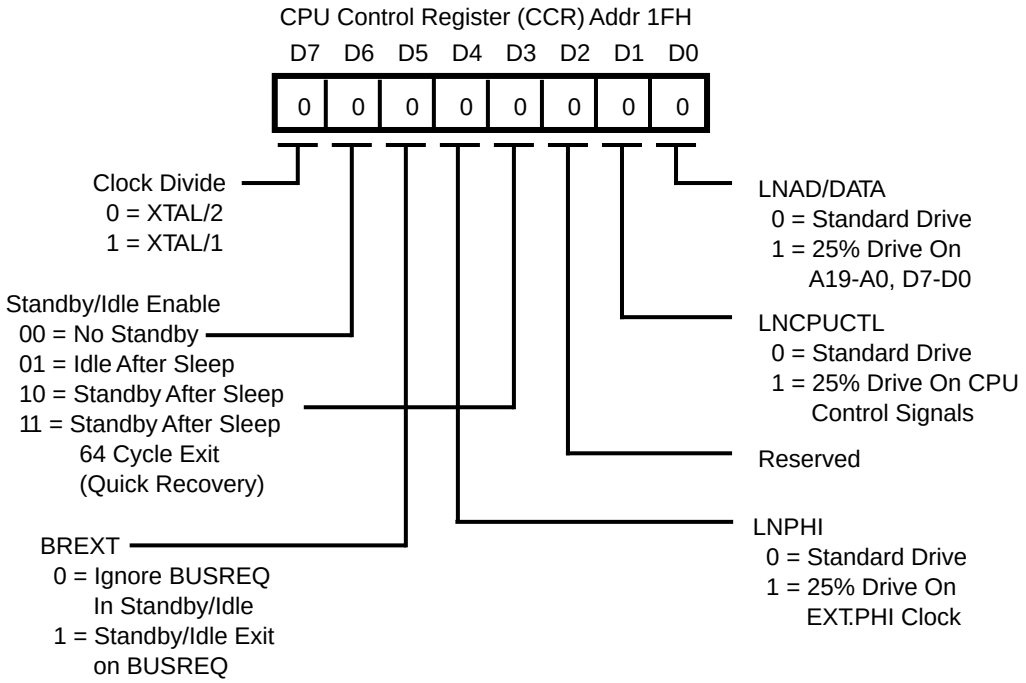



**Figure 51. CPU Control Register**

## 16550 MIMIC INTERFACE REGISTERS

### MIMIC Master Control Register (MMC)

The 16550 MIMIC interface is controlled by the MMC register. Setting it allows for different modes of operation such as using the 8-bit counters, DMA accesses, and which IRQ structure is used with the PC/XT/AT.

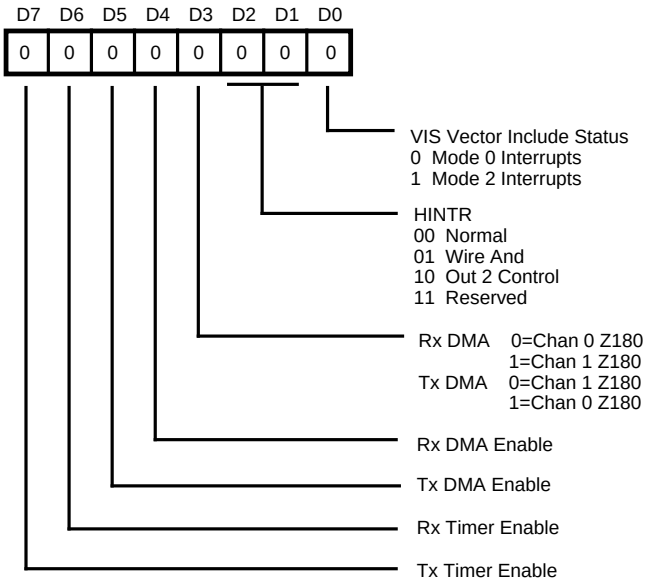



**Figure 60. MIMIC Master Control Register**
(Z180 MPU Read/Write, Address xxFFH)

**Bit 7 Transmit Emulation Delay Counter Enable (Read/Write)**
If bit 7 is set to 1, it enables the transmit delay timer. When the Z180 reads the Transmit Register, it loads the transmit delay timer from the Transmit Time Constant Register and enables the timer to count down to zero. This timer delays setting the Transmit Holding Register Empty (THRE) bit until the timer times out. If this bit is 0, then THRE is set immediately on a Z180 read of the Transmit Register. This bit also enables the emulation timer used in Transmitter Double Buffering.

**Bit 6 Receive Emulation Delay Counter Enable (Read/Write)**
If bit 6 is set to 1, it enables the receive delay timer. When the Z180 writes to the Receive Buffer, it loads the receive delay timer from the Receive Time Constant Register and enables the timer to count down to zero. This timer delays setting the Data Ready (DR) bit in the LSR until the timer times out. If this bit is 0 then DR is set immediately on a Z180 write to the Receive Buffer.

Both counters are single pass and stop on a count of Zero. Their purpose is to delay data transfer just as if the 16550 UART had to shift the data in and out. This is provided to alleviate any software problems a high speed continuous data transfer might cause to existing software. If this is not a concern, then data can be read and written as fast as the two machines can access the devices. In FIFO mode of operation , the timers are used to delay the status to the PC interface by the time required to actually shift the characters out, or in, if an actual UART were present.

**Bit 5 Transmit DMA Enable (Read/Write)**
If this bit is set to 1, it enables the Transmit DMA function.

**Bit 4 Receive DMA Enable (Read/Write)**
If this bit is set to 1, it enables the Receive DMA function.

**Bit 3 Receive DMA Channel Select (Read/Write)**
If bit 3 is set to 0, then Receive DMA transfer is done through Z180 DMA channel 0 and the Transmit DMA is done through DMA channel 1. If bit 3 is set to 1, then Receive DMA transfer is done through Z180 DMA channel 1 and the Transmit DMA is done through DMA channel 0.

**Bits 2,1 Interrupt Select (Read/Write).**
See Table 15.

**Bit 0 Vector Include Status (Read/Write)**
This bit is used to select the interrupt response mode of the Z180. A 0 in this bit enables Mode 0 interrupts; a 1 enables Mode 2 response.

**Table 15. MIMIC Master Control Register Interrupt Select**

| Bit 2 | Bit 1 | HINTR Function |
|---|---|---|
| 0 | 0 | HINTR is set to normal 16550 MIMIC mode. A fully driven output is required when external priority arbiters are used. |
| 0 | 1 | A wired AND condition on the HINTR pin is possible to the PC/XT/AT. The interrupt is active High with only the pull-up of the HINTR pin driving; otherwise this pin is tri-state. Wired AND is needed when an external arbiter is not available. |
| 1 | 0 | HINTR is driven when out 2 of the Modem Control Register is 1. HINTR is tri-state when MCR out 2 is 0. |
| 1 | 1 | RESERVED |

## Interrupt Enable Register

The IE Register allows each of the 16550/8250 interrupts to the Z180™ MPU to be masked off individually or globally.

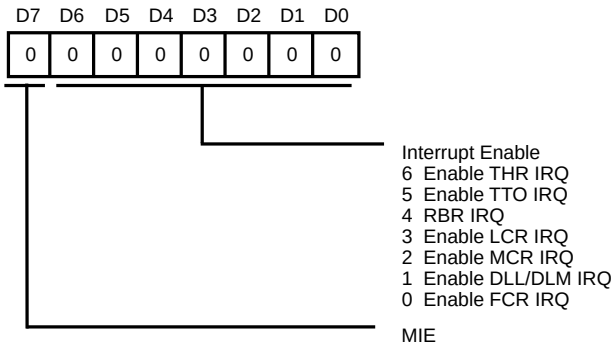



**Figure 62. IE Register**
(Z180 MPU, Address xxFDH)

**Bit 7 Master Interrupt Enable (Read/Write)**
If bit 7 is 0, all interrupts from the 16550 MIMIC are masked off. If this bit is 1, then interrupts are enabled individually by setting the appropriate bit.

**Bit 6 Enable THR Interrupt (Read/Write)**
If this bit is 1, it enables the Transmit Holding Register Interrupt.

**Bit 5 Enable TTO Interrupt (Read/Write)**
If this bit is 1, it enables the Transmitter Timeout Interrupt. This interrupts the CPU when characters remain in the FIFO below the trigger level and the FIFO is not read or written for the length of time in the transmitter timeout register.

**Bit 4 Enable RBR Interrupt (Read/Write)**
If this bit is 1, it enables the Receive Buffer Register Interrupt.

**Bit 3 Enable LCR Interrupt (Read/Write)**
If this bit is 1, it enables the Line Control Register interrupt.

**Bit 2 Enable MCR Interrupt (Read/Write)**
If this bit is 1, it enables the Modem Control Register Interrupt.

**Bit 1 Enable DLL/DLM Interrupt (Read/Write)**
If this bit is 1, it enables the Divisor Latch Least and Most Significant Byte interrupts.

**Bit 0 Enable FCR Interrupt (Read/Write)**
If this bit is 1 , then interrupts are enabled for a PC write to the FIFO control register (FCR) or for occurrence of Tx Overrun.

Priority of interrupts are in this order:

| | | |
|---|---|---|
| (Highest) | 6 | THR IRQ |
| | 5 | TTO IRQ |
| | 4 | RBR IRQ |
| | 3 | MCR IRQ |
| | 2 | LCR IRQ |
| | 1 | DLL IRQ |
| | 1 | DLM IRQ |
| (Lowest) | 0 | FCR or Tx OVERRUN IRQ |

## Interrupt Vector Register

The Interrupt Vector Register contains either the opcode (Z180 Interrupt Mode 0) or the modified vector used as the lower address for a Z180 interrupt service routine (Z180 Interrupt Mode 2), depending upon the VIS bit in the MMC Register (MIMIC Master Control Register). If the VIS bit is 0, then Z180 Mode 0 interrupt is selected; if VIS is 1, then Z180 Mode 2 is selected. Note that in Z180 Interrupt Mode 0, the data input to the MPU during the interrupt acknowledge cycle is an instruction opcode; in Z180 Interrupt Mode 2, this data (modified depending on the source of the interrupt) becomes part of an address from which to get the starting address of the interrupt service routine.

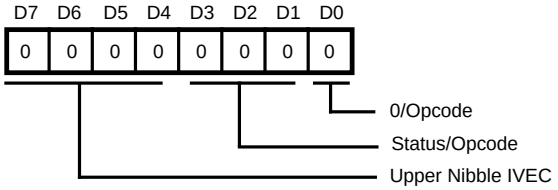



**Figure 63. IVEC Register**
(Z180 MPU, Address xxFCH)

**Bits 7-4 Upper Nibble IVEC (Read/Write)**
These four bits generate either an opcode for Z180 Interrupt Mode 0, or the upper four bits of the interrupt modified vector used as an 8-bit address to support the Z180 Interrupt Mode 2. These bits are read/write and always read back what was last written to them.

**Bits 3-1 Interrupt Modified Vector/Opcode (Read/Write Table 16)**
These three bits are the Interrupt Status bits when VIS in the MMC register is 1 (Z180 Interrupt Mode 2). If VIS bit is 0, then this field contains bit 3-bit 1 of the opcode. If the VIS bit is 0, then these bits contain what was last written to them.

## 16550 MIMIC REGISTERS

The Z80182/Z8L182 contains the following set of registers for interfacing with the PC/XT/AT.

- Receive Buffer Register
- Transmit Holding Register
- Interrupt Enable Register
- Interrupt Identification Register
- FIFO Control Register
- Line Control Register
- Modem Control Register
- Line Status Register
- Modem Status Register
- Scratch Register
- Divisor Latch Least/Most Significant Bytes
- FIFO Control Register

These registers emulate the 16550 UART and enable the PC/XT/AT to interface with them as with an actual 16550 UART. This allows the Z80182/Z8L182 to be software compatible with existing modem software.

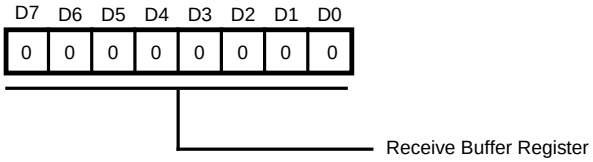



**Figure 69. Receive Buffer Register**
(PC Read Only, Address 00H, DLAB=0, R/W=Read)
(Z180™ MPU Write Only, Address XXF0H)

### Receive Buffer Register

When the Z180 has assembled a byte of data to pass to the PC/XT/AT, it places it in the Receive Buffer Register. If the Received Data Available interrupt is enabled then an interrupt is generated for the PC/XT/AT and the Data Ready bit is set (if the Receive Timer is enabled, the interrupt and setting of the Data Ready bit is delayed until after the timer times out). Also the shadowed bits of the Line Status Register are transferred to their respective bits when the Z180 MPU writes to the Receive Buffer Register (See Line Status Register Bits 1, 2, 3 and 4). This allows a simultaneous setting of error bits when the data is written to the Receive Buffer Register. In FIFO, mode this address is used to read (PC) and write (Z180) the Receive FIFO.

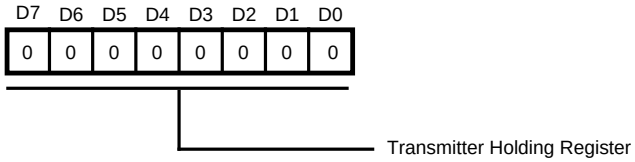



**Figure 70. Transmit Holding Register**
(PC Write Only, Address 00H, DLAB=0, R/W=Write)
(Z180 MPU Read Only, Address xxF0H)

### Transmit Holding Register

When the PC/XT/AT writes to the Transmit Holding Register, the Z80182/Z8L182 responds by setting the appropriate bit in the IP register and by generating an interrupt to the Z180 MPU if it is enabled. When the Z180 MPU reads this register the Transmit Holding Register empty flag is set (if the transmitter timer is enabled , this bit is set after the timer times out). In FIFO mode of operation, this address is used to read (Z180) and write (PC) the Transmitter FIFO.

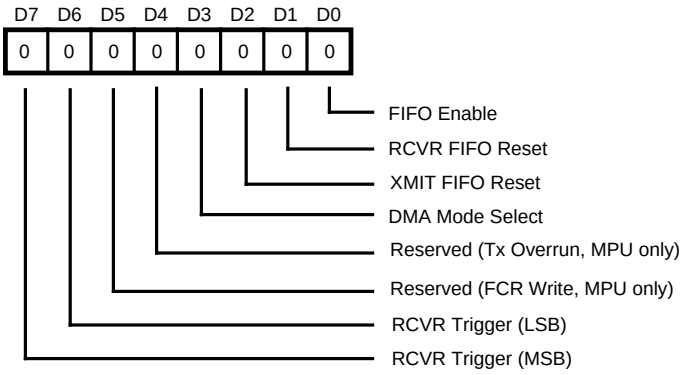



**Figure 71. FIFO Control Register**
(PC Write Only, Address 02H)
(Z180 MPU Read Only, Address xxE9H)

## PARALLEL PORTS REGISTERS

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output. The Ports consist of two registers the Port Direction Control Register and the Port Data Register. The Port and direction register can be accessed in any page of I/O space since only the lowest eight address lines are decoded. Bits PC7 and PC6 are input only bits and have the special function of reading the external value of the /INT2 and /INT1 pins. Writing '1' to these bits will clear the edge detect interrupt logic when operating /INT2 and/or /INT1 in edge detect mode.

When Port B and Port C bits 5-0 are deselected in the System Configuration Register, the Data and Data Direction Registers are still available as read/write scratch registers. If a Port is deselected and if the DDR bit is a '0', then the written value to that bit will be latched and this value can be read back. If a Port is deselected and if the DDR bit is a '1', then you could read only the external pin value; any write to that bit is latched but can be read back only with DDR=0.

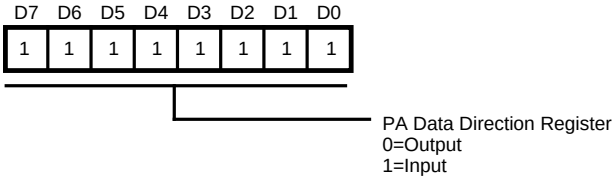



**Figure 83. PA, Port A, Data Direction Register**
(Z180 MPU Read/Write, Address xxEDH)

The data direction register determines which are inputs and outputs in the PA Data Register. When a bit is set to 1 the corresponding bit in the PA Data Register is an input. If the bit is 0, then the corresponding bit is an output.

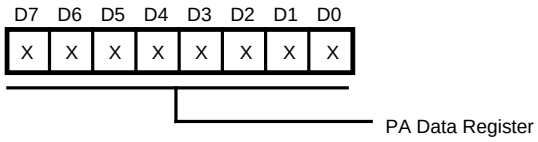



**Figure 84. PA, Port A, Data Register**
(Z180 MPU Read/Write, Address xxEEH)

When the Z180 MPU writes to the PA Data Register the data is stored in the internal buffer. The values of the PA Data Register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PA Data Register the data on the external pins is returned.

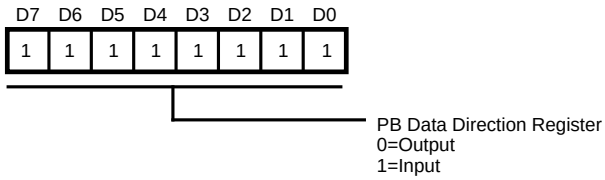



**Figure 85. PB, Port B, Data Direction Register**
(Z180 MPU Read/Write, Address xxE4H)

The data direction register determines which are inputs and outputs in the PB Data Register. When a bit is set to 1 the corresponding bit in the PB Data Register is an input. If the bit is 0 then the corresponding bit is an output.

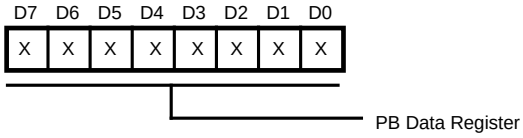



**Figure 86. PB, Port B, Data Register**
(Z180 MPU, Address xxE5H)

When the Z180 MPU writes to the PB Data Register the data is stored in the internal buffer. The values of Port B data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PB Data Register, the data on the external pins is returned.

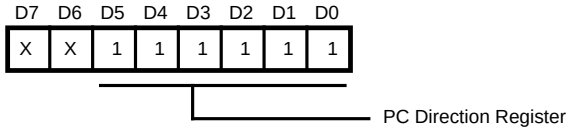



**Figure 87. PC, Port C, Data Direction Register**
(Z180 MPU Read/Write, Address xxDDH)

## TIMING DIAGRAMS

Z180 MPU Timing

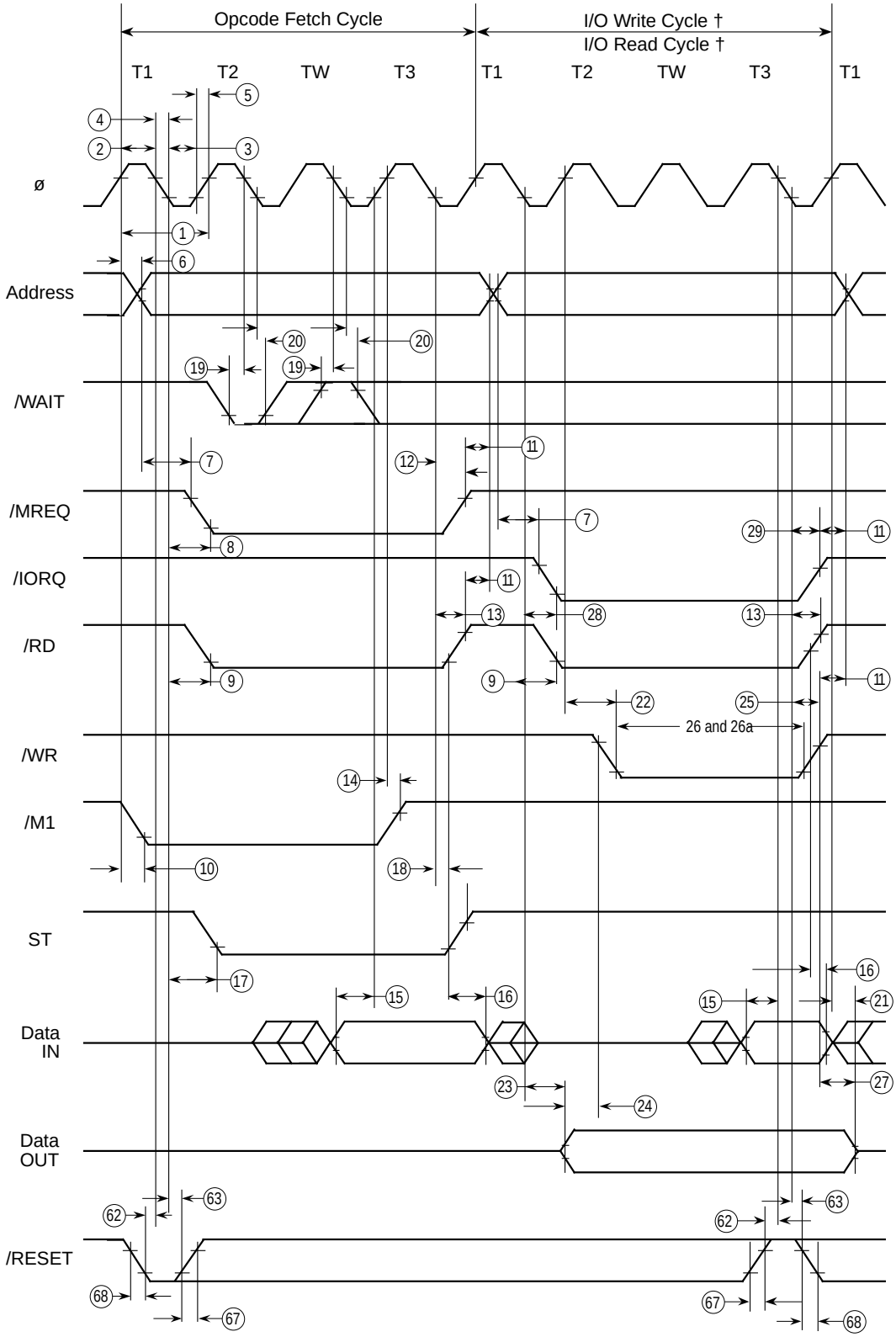



**Figure 90. CPU Timing**
(Opcode Fetch Cycle, Memory Read/Write Cycle
I/O Read/Write Cycle)

## AC CHARACTERISTICS (Continued)

Z85230 System Timing Diagram

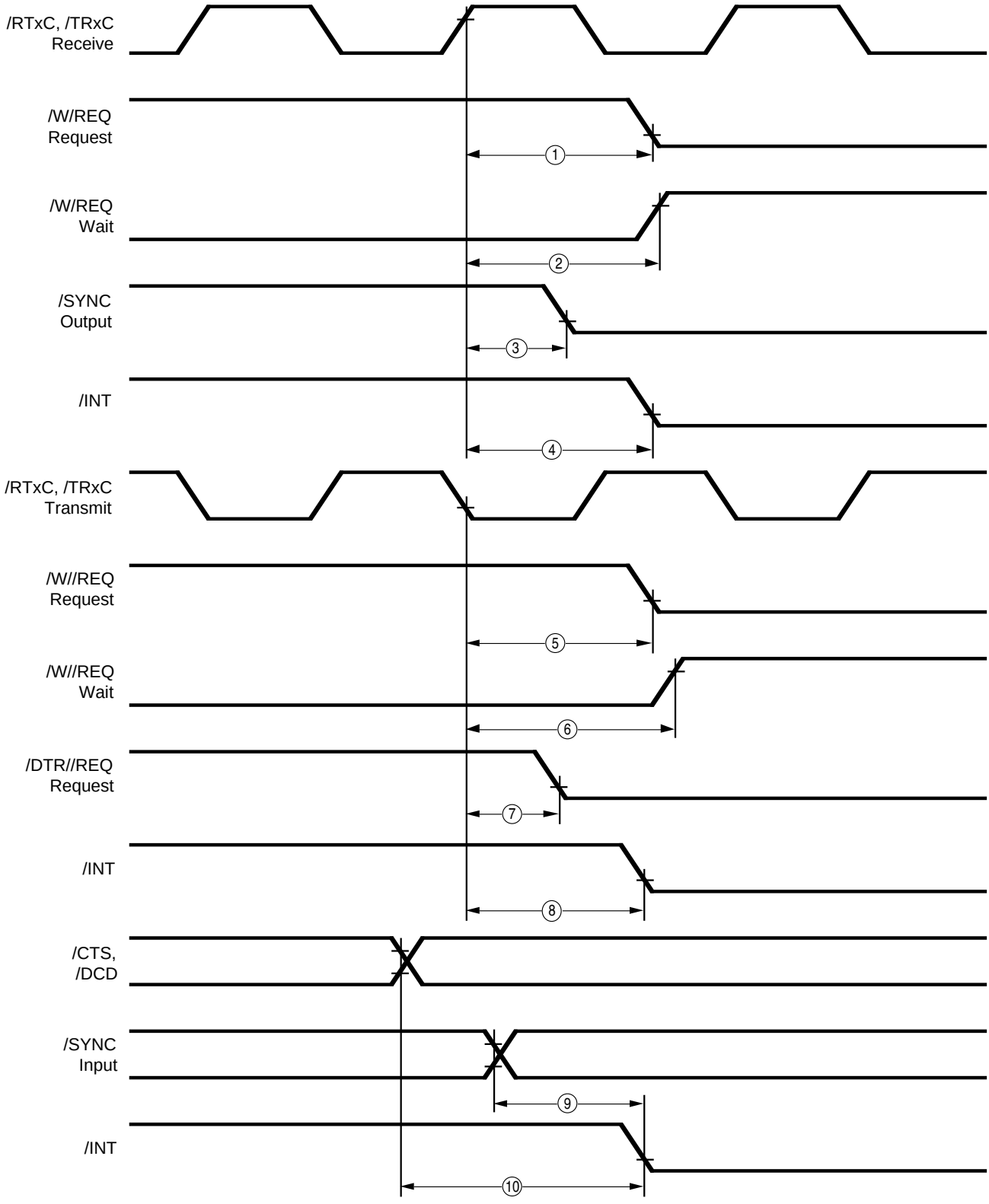



**Figure 106. Z85230 System Timing**

**Table D. Z85230 System Timing Table**

| No. | Symbol | Parameter | 20 MHz Min | 20 MHz Max | Notes [4] |
|---|---|---|---|---|---|
| 1 | TdRxC(REQ) | /RxC to /W//REQ Valid | 13 | 18 | [2] |
| 2 | TdRxC(W) | /RxC to /Wait Inactive | 13 | 18 | [1,2] |
| 3 | TdRxC(SY) | /RxC to /SYNC Valid | 9 | 13 | [2] |
| 4 | TdRxC(INT) | /RxC to /INT Valid | 15 | 22 | [1,2] |
| 5 | TdTxC(REQ) | /TxC to /W//REQ Valid | 8 | 12 | [3] |
| 6 | TdTxC(W) | /TxC to /Wait Inactive | 8 | 15 | [1,3] |
| 7 | TdTxC(DRQ) | /TxC to /DTR//REQ Valid | 7 | 11 | [3] |
| 8 | TdTxC(INT) | /TxC to /INT Valid | 9 | 14 | [1,3] |
| 9 | TdSY(INT) | /SYNC to /INT Valid | 2 | 6 | [1] |
| 10 | TdExT(INT) | /DCD or /CTS to /INT Valid | 3 | 9 | [1] |

**Notes:**
These AC parameters values are preliminary and subject to change without notice.
[1] Open-drain output, measured with open-drain test load.
[2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[4] Units equal to TcPc

**Table E. I/O Port Timing**

| No. | Symbol | Parameter | Z8L182 20 MHz Min | Z8L182 20 MHz Max | Z80182 33 MHz Min | Z80182 33 MHz Max |
|---|---|---|---|---|---|---|
| 1 | TsPIA(RD) | Port Data Input Setup to /RD Fall | 20 | | 20 | |
| 2 | ThPIA(RD) | Port Data Input Hold From /RD Rise | 0 | | 0 | |
| 3 | $TdWR_F$(PIA) | Port Data Output Delay From /WR Fall | | 60 | | 60 |
| 4 | $T_FWR_F$(PIA) | Port Data Output Float From /WR Fall | 0 | | 0 | |

**Table F. External Bus Master Timing**

| No. | Symbol | Parameter | Z8L182 20 MHz Min | Z8L182 20 MHz Max | Z80182 33 MHz Min | Z80182 33 MHz Max |
|---|---|---|---|---|---|---|
| 1 | TsA(IORQf) | Address to /IORQ Fall Setup | 10 | | 5 | |
| 2 | TsIOf(WRf) | /IORQ Fall to /WR Fall Setup | 0 | | 0 | |
| 3 | TsIOf(RDf) | /IORQ Fall to /RD Fall Setup | 0 | | 0 | |
| 4 | ThIOR($WR_R$) | /IORQ Rise From /WR Rise Hold | 0 | | 0 | |
| 5 | ThIOR($RD_R$) | /IORQ Rise From /RD Rise Hold | 0 | | 0 | |
| 6 | TdRDf(DO) | /RD Fall to Data Out Valid Delay | | 50 | | 45 |
| 7 | $T_HRD_R$(DO) | /RD Rise to Data Out Valid Hold | | 0 | | 0 |
| 8 | $T_SD(WR_R)$ | Data In to /WR Fall Setup | 50 | | 50 | |
| 9 | THD($WR_R$) | Data In From /WR Rise Hold | 10 | 8 | 10 | |

## ESCC External Bus Master Timing

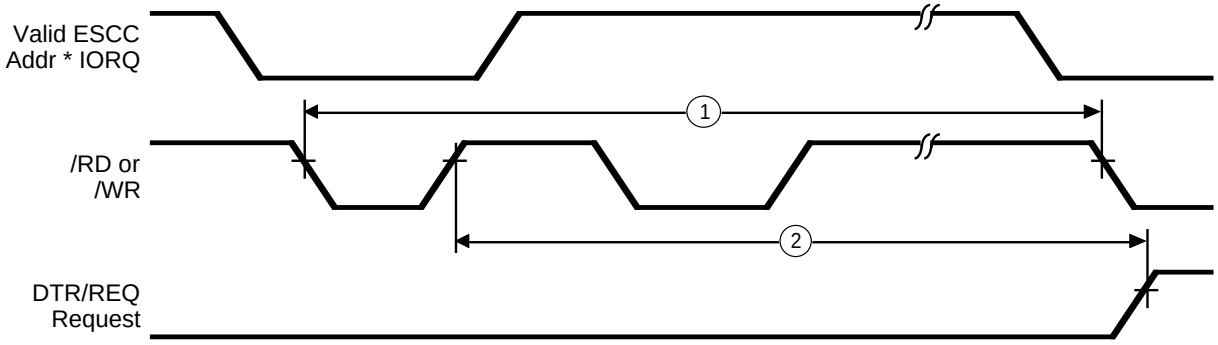


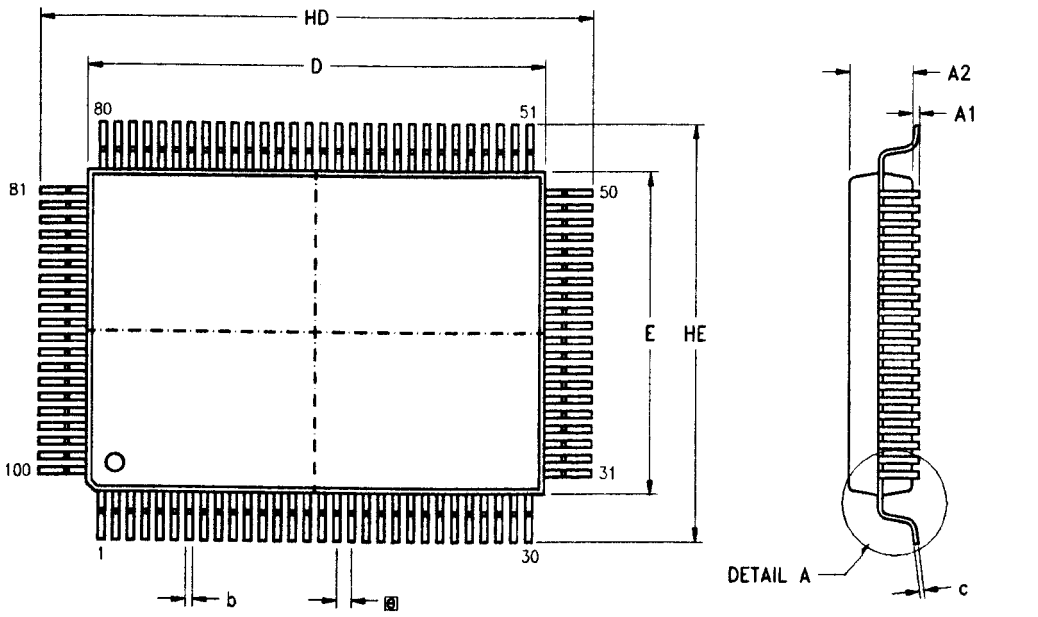

**Figure 109. ESCC External Bus Master Timing**

**Table G. External Bus Master Interface Timing** (SCC Related Timing)

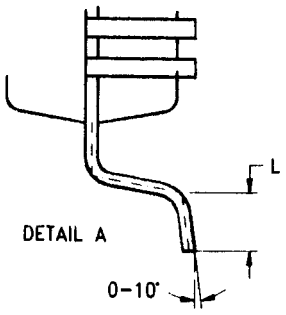
| No. | Symbol | Parameter | Z8L182 20 MHz Min | Z8L182 20 MHz Max | Z80182 33 MHz Min | Z80182 33 MHz Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| 1 | TrC | Valid Access Recovery Time | 4TcC | | 4TcC | | ns | [1] |
| 2 | TdRDr(REQ) | /RD Rise to /DTR//REQ Not Valid Delay | 4TcC | | 4TcC | | ns | |

**Notes:**
These AC parameter values are preliminary and are subject to change without notice.
[1] Applies only between transactions involving the ESCC.
$T_{CC}$ = ESCC clock period time

## PACKAGE INFORMATION (Continued)




| SYMBOL | MILLIMETER | | INCH | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A1 | 0.10 | 0.30 | .004 | .012 |
| A2 | 2.60 | 2.80 | .102 | .110 |
| b | 0.25 | 0.40 | .010 | .016 |
| c | 0.13 | 0.20 | .005 | .008 |
| HD | 23.70 | 24.15 | .933 | .951 |
| D | 19.90 | 20.10 | .783 | .791 |
| HE | 17.70 | 18.15 | .697 | .715 |
| E | 13.90 | 14.10 | .547 | .555 |
| e | 0.65 TYP | | .0256 TYP | |
| L | 0.70 | 1.10 | .028 | .043 |




NOTES:
1. CONTROLLING DIMENSIONS : MILLIMETER
2. MAX COPLANARITY : .10 / .004

**100-Pin QFP Package Diagram**