# Zilog - Z8018233FSC Datasheet

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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z80180 |
| Number of Cores/Bus Width | 1 Core, 8-Bit |
| Speed | 33MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DRAM |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | - |
| SATA | - |
| USB | - |
| Voltage - I/O | 5.0V |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Security Features | - |
| Package / Case | 100-QFP |
| Supplier Device Package | 100-QFP |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8018233fsc |

## Z180 CPU SIGNALS (Continued)

**/NMI.** *Non-maskable interrupt (input, negative edge triggered).* /NMI has a higher priority than /INT and is always recognized at the end of an instruction, regardless of the state of the interrupt enable flip-flops. This signal forces CPU execution to continue at location 0066H.

**/INT0.** *Maskable Interrupt Request 0 (input/output active Low).* This signal is generated by external I/O devices. The CPU will honor this request at the end of the current instruction cycle as long as the /NMI and /BUSREQ signals are inactive. The CPU acknowledges this interrupt request with an interrupt acknowledge cycle. During this cycle, both the /M1 and /IORQ signals become active. The internal Z180 MPU's /INT0 source is: /INT0 or ESCC or the MIMIC. This input is level triggered. /INT0 is an open-drain output, so you can connect other open-drain interrupts onto the circuit in addition to haveing a pull-up to VCC.

**/INT1, /INT2.** *Maskable Interrupt Requests 1 and 2 (inputs, active Low).* This signal is generated by external I/O devices. The CPU will honor these requests at the end of the current instruction cycle as long as the /NMI, /BUSREQ, and /INT0 signals are inactive. The CPU acknowledges these interrupt requests with an interrupt acknowledge cycle. Unlike the acknowledgment for /INT0, during this cycle neither the /M1 or /IORQ signals become active. These pins may be programmed to provide an active Low level on rising or falling edge interrupts. The level of the external /INT1 and /INT2 pins may be read through bits PC6 and PC7 of parallel Port C. Pin /INT1/PC6 multiplexes /INT1 and PC6. Pin /INT2/PC7 multiplexes /INT2 and PC7.

**/RFSH.** *Refresh (input/output, active Low, tri-state).* Together with /MREQ, /RFSH indicates that the current CPU machine cycle and the contents of the address bus should be used for refresh of dynamic memories. The low order 8 bits of the address bus (A7-A0) contain the refresh address. This signal is analogous to the /REF signal of the Z64180.

## Z180 MPU UART AND SIO SIGNALS

**CKA0, CKA1.** *Asynchronous Clocks 0 and 1 (bi-directional, active High).* These pins are the transmit and receive clocks for the synchronous channels. CKA0 is multiplexed with /DREQ0 on the CKA0//DREQ0 pin. CKA1 is multiplexed with /TEND0 on the CKA1//TEND0 pin.

**CKS.** *Serial Clock (bi-directional, active High).* This line is clock for the CSIO channel and is multiplexed with the ESCC signal (/W//REQB) and the 16550 MIMIC interface signal /HTxRDY on the CKS//W//REQB//HTxRDY pin.

**/DCD0.** *Data Carrier Detect 0 (input, active Low).* This is a programmable modem control signal for ASCI channel 0. /DCD0 is multiplexed with the PB2 (parallel Port B, bit 2) on the /DCD0/PB2 pin.

**/RTS0.** *Request to Send 0 (output, active Low).* This is a programmable modem control signal for ASCI channel 0. This pin is multiplexed with PB0 (parallel Port B, bit 0) on the /RTS0/PB0 pin.

**/CTS0.** *Clear to Send 0 (input, active Low).* This line is a modem control signal for the ASCI channel 0. This pin is multiplexed with PB1 (parallel Port B, bit 1) on the /CTS0 /PB1 pin.

**TxA0.** *Transmit Data 0 (output, active High).* This signal is the transmitted data from the ASCI channel 0. This pin is multiplexed with PB3 (parallel Port B, bit 3) on the TxA0/PB3 pin.

**TxS.** *Clocked Serial Transmit Data (output, active High).* This line is the transmitted data from the CSIO channel. TxS is multiplexed with the ESCC signal (/DTR//REQB) and the 16550 MIMIC interface signal HINTR on the TxS//DTR //REQB//HINTR pin.

**RxA0.** *Receive Data 0 (input, active High).* This signal is the receive data to ASCI channel 0. This pin is multiplexed with PB4 (parallel Port B, bit 4) on the RxA0/PB4.

**RxS.** *Clocked Serial Receive Data (input, active High).* This line is the receive data for the CSIO channel. RxS is multiplexed with the /CTS1 signal for ASCI channel 1 and with PB7 (parallel Port B, bit 7) on the RxS//CTS1/PB7 pin.

**RxA1.** *Received Data ASCI channel 1 (input, active High).* This pin is multiplexed with PB6 (parallel Port B, bit 6) on the RxA1/PB6 pin.

**TxA1.** *Transmitted Data ASCI Channel 1 (output, active High).* This pin is multiplexed with PB5 (parallel Port B, bit 5) on the TxA1/PB5 pin.

## Z180 MPU DMA SIGNALS

**/TEND0.** *Transfer End 0 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND0 is multiplexed with CKA1 on the CKA1//TEND0 pin.

**/TEND1.** *Transfer End 1 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND1 is multiplexed with the ESCC signal /RTSB and the 16550 MIMIC interface signal /HRxRDY on the /TEND1//RTSB//HRxRDY pin.

**/DREQ0.** *DMA request 0 (input, active Low).* /DREQ0 is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. /DREQ0 is multiplexed with CKA0 on the CKA0//DREQ0 pin.

**/DREQ1.** *DMA request 1 (input, active Low).* /DREQ1 is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

## Z180™ MPU TIMER SIGNALS

**$T_{OUT.}$** *Timer Out (output, active High).* $T_{OUT}$ is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/$T_{OUT}$ pin.

## Z85230 ESCC™ SIGNALS

**TxDA.** *Transmit Data (output, active High).* This output signal transmits channel A's serial data at standard TTL levels. This output can be tri-stated during power down modes.

**TxDB.** *Transmit Data (output, active High).* This output signal transmits channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface /HDDIS signal on the TxDB//HDDIS pin.

**RxDA.** *Receive Data (inputs, active High).* These inputs receive channel A's serial data at standard TTL levels.

**RxDB.** *Receive Data (input, active High).* These inputs receive channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB/HA1 pin.

**/TRxCA.** *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel A program control. /TRxCA may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

**/TRxCB.** *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel B program control. /TRxCB may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in output mode. In Z80182/Z8L182 mode 1 /TRxCB is multiplexed with the 16550 MIMIC interface HA0 input on the /TRxCB/HA0 pin.

**/RTxCA.** *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel A program control. In channel A, /RTxCA may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCA pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

**/RTxCB.** *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel B program control. In channel B, /RTxCB may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCB pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182/Z8L182 mode 1 the /RTxCB signal is multiplexed with 16550 MIMIC interface HA2 input on the /RTxCB/HA2 pin.

**/W//REQB.** *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

## 16550 MIMIC INTERFACE SIGNALS

**HD7-HD0.** *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

**/HDDIS.** *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

**HA2-HA0.** *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

**/HCS.** *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

**/HWR.** *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

**/HRD.** *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

**HINTR.** *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

**/HTxRDY.** *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

**/HRxRDY.** *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

## PARALLEL PORTS

**PA7-PA0.** *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

**PB7-PB0.** *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

**PC7-PC0.** *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

**Table 5. Primary, Secondary and Tertiary Pin Functions** (Continued)

| Pin Number VQFP | Pin Number QFP | 1st Function | 2nd Function | 3rd Function | MUX Control |
|---|---|---|---|---|---|
| 71 | 74 | RxDA | | | |
| 72 | 75 | /TRxCA | | | |
| 73 | 76 | TxDA | | | |
| 74 | 77 | /DCDB | /HRD | | SYS CONF REG Bit 1 |
| 75 | 78 | /CTSB | /HWR | | SYS CONF REG Bit 1 |
| 76 | 79 | TxDB | /HDDIS | | SYS CONF REG Bit 1 |
| 77 | 80 | /TRxCB | HA0 | | SYS CONF REG Bit 1 |
| 78 | 81 | RxDB | HA1 | | SYS CONF REG Bit 1 |
| 79 | 82 | /RTxCB | HA2 | | SYS CONF REG Bit 1 |
| 80 | 83 | /SYNCB | /HCS | | SYS CONF REG Bit 1 |
| 81 | 84 | /HALT | | | |
| 82 | 85 | /RFSH | | | |
| 83 | 86 | /IORQ | | | |
| 84 | 87 | /MRD | /MREQ | | INT EDG/PIN REG Bit 3 |
| 85 | 88 | E | | | |
| 86 | 89 | /M1 | | | |
| 87 | 90 | /WR | | | |
| 88 | 91 | /RD | | | |
| 89 | 92 | PHI | | | |
| 90 | 93 | $V_{SS}$ | | | |
| 91 | 94 | XTAL | | | |
| 92 | 95 | EXTAL | | | |
| 93 | 96 | /WAIT | | | |
| 94 | 97 | /BUSACK | | | |
| 95 | 98 | /BUSREQ | | | |
| 96 | 99 | /RESET | | | |
| 97 | 100 | /NMI | | | |
| 98 | 1 | /INT0 | | | |
| 99 | 2 | /INT1 | PC6** | | |
| 100 | 3 | /INT2 | PC7** | | |

**Notes:**
* Also controlled by Interrupt Edge/Pin MUX Register
** PC7 and PC6 are inputs only and can read values of /INT1 and /INT2.

## Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

## Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100% software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

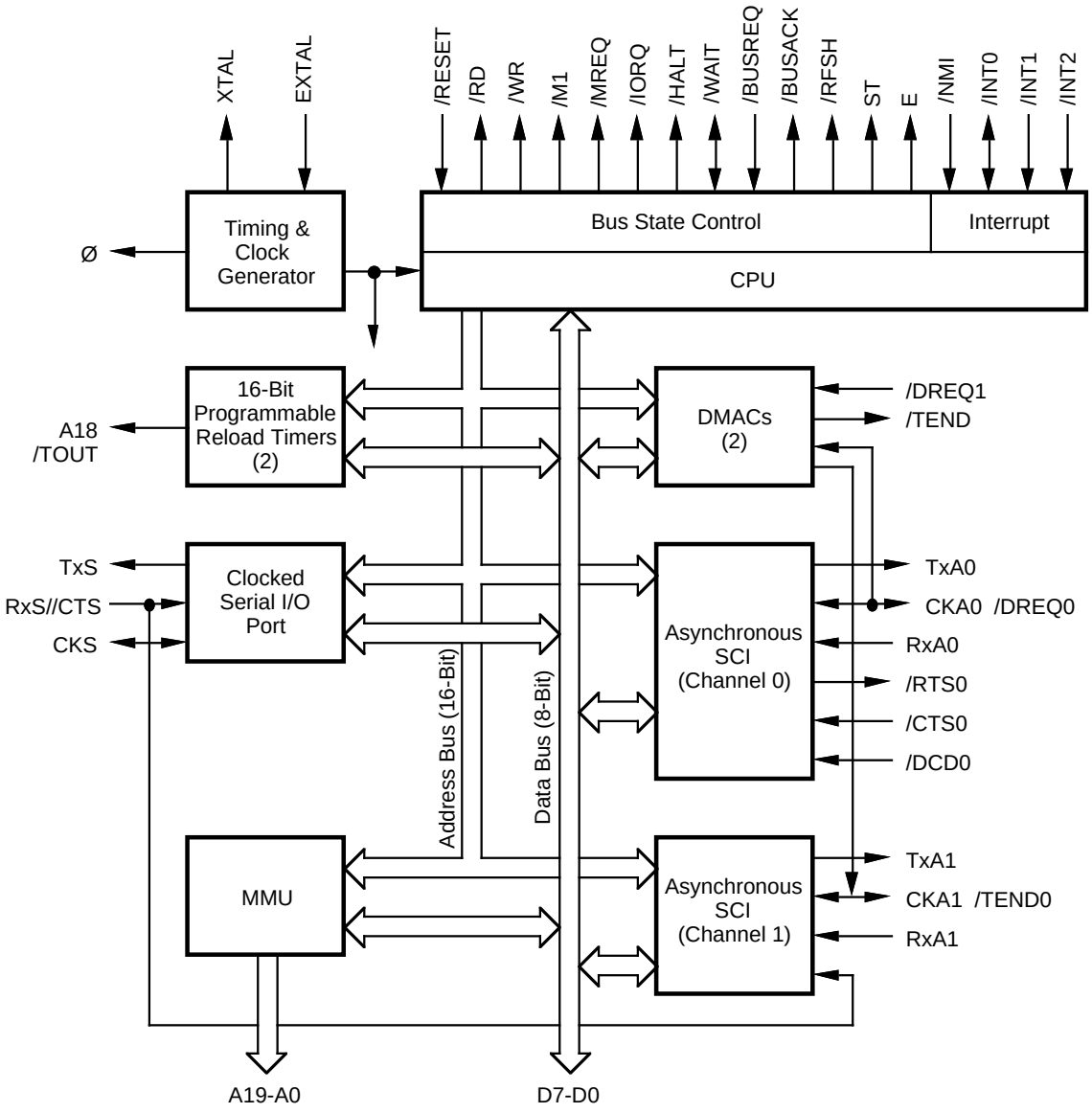



**Figure 4. S180 MPU Block Diagram of Z182**

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

## Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

## PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only). The Ports are controlled through two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

## PROGRAMMING

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for Z182 peripheral access. The full sixteen address lines are decoded for on-chip Z180 MPU access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers through the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated through the System Configuration Register and the Interrupt Edge/Pin MUX Register.

**Table 7. Z80182/Z8L182 MPU Registers**

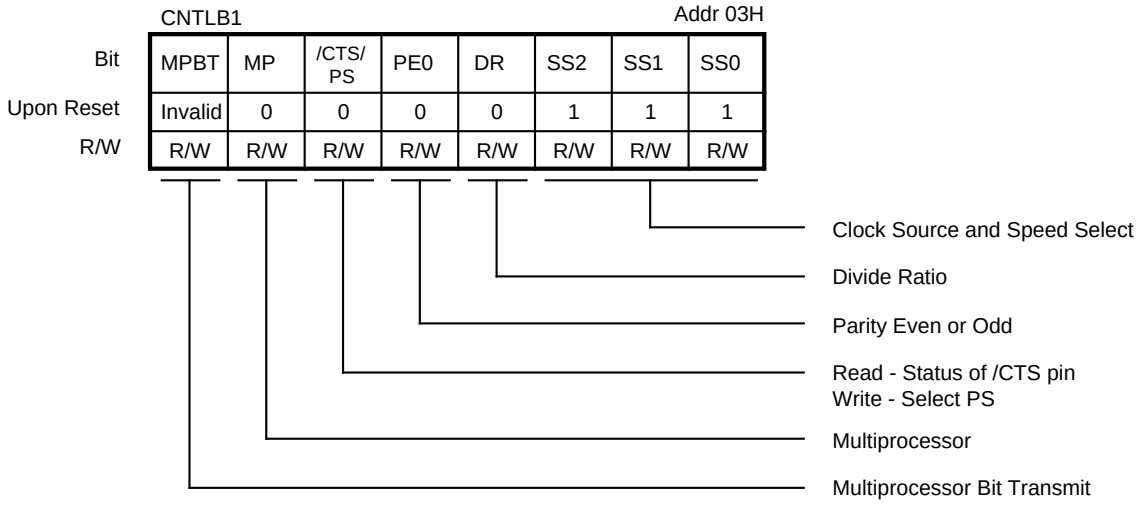
| Register Name | MPU Addr | PC Addr |
|---|---|---|
| Z80182/Z8L182 MPU Control Registers | 0000H to 00x3FH<br>(Relocatable to 0040H to 007FH<br>or 0080H to 00BFH) | None |

**Note:**
"x" indicates don't care condition

**Table 8. Z80182/Z8L182 MIMIC Register MAP**

| Register Name | MPU Addr/Access | | PC Addr/Access | |
|---|---|---|---|---|
| MMC MIMIC Master Control Register | xxFFH | R/W | None | |
| IUS/IP Interrupt Pending | xxFEH | R/Wb7 | None | |
| IE Interrupt Enable | xxFDH | R/W | None | |
| IVEC Interrupt Vector | xxFCH | R/W | None | |
| TTCR Transmit Time Constant | xxFAH | R/W | None | |
| RTCR Receive Time Constant | xxFBH | R/W | None | |
| FSCR FIFO Status and Control | xxECH | R/W7-4 | None | |
| RTTC Receive Timeout Time Constant | xxEAH | R/W | None | |
| TTTC Transmit Timeout Time Constant | xxEBH | R/W | None | |
| RBR Receive Buffer Register | xxF0H | W only | 00H | DLAB=0 R only |
| THR Transmit Holding Register | xxF0H | R only | 00H | DLAB=0 W only |
| IER Interrupt Enable Register | xxF1H | R only | 01H | DLAB=0 R/W |
| IIR Interrupt Identification | None | | 02H | R only |
| FCR FIFO Control Register | xxE9H | R only | 02H | W only |
| MM REGISTER | XXE9H | W only | None | |
| LCR Line Control Register | xxF3H | R only | 03H | R/W |
| MCR Modem Control Register | xxF4H | R only | 04H | R/W |
| LSR Line Status Register | xxF5H | R/Wb6432 | 05H | R only |
| MSR Modem Status Register | xxF6H | R/Wb7-4 | 06H | R only |
| SCR Scratch Register | xxF7H | R only | 07H | R/W |
| DLL Divisor Latch (LSByte) | xxF8H | R only | 00H | DLAB=1 R/W |
| DLM Divisor Latch (MSByte) | xxF9H | R only | 01H | DLAB=1 R/W |

## ASCI CHANNELS CONTROL REGISTERS (Continued)




| General Divide Ratio SS, 2, 1, 0 | PS = 0 (Divide Ratio = 10) DR = 0 (x16) | DR = 1 (x64) | PS = 1 (Divide Ratio = 30) DR = 0 (x16) | DR = 1 (x64) |
|---|---|---|---|---|
| 000 | Ø ÷ 160 | Ø ÷ 640 | Ø ÷ 480 | Ø ÷ 1920 |
| 001 | Ø ÷ 320 | Ø ÷ 1280 | Ø ÷ 960 | Ø ÷ 3840 |
| 010 | Ø ÷ 640 | Ø ÷ 2580 | Ø ÷ 1920 | Ø ÷ 7680 |
| 011 | Ø ÷ 1280 | Ø ÷ 5120 | Ø ÷ 3840 | Ø ÷ 15360 |
| 100 | Ø ÷ 2560 | Ø ÷ 10240 | Ø ÷ 7680 | Ø ÷ 30720 |
| 101 | Ø ÷ 5120 | Ø ÷ 20480 | Ø ÷ 15360 | Ø ÷ 61440 |
| 110 | Ø ÷ 10240 | Ø ÷ 40960 | Ø ÷ 30720 | Ø ÷ 122880 |
| *111 | External Clock (Frequency < Ø ÷ 40) | | | |

**Note:**
* Baud rate is external clock rate ÷ 16; therefore, Ø ÷ (40 x 16) is maximum baud rate using external clocking.

**Figure 12. ASCI Control Register B** (Ch. 1)

## DMA REGISTERS (Continued)

DSTAT — Addr 30H

| Bit | DE1 | DE0 | /DWE1 | /DWE0 | DIE1 | DIE0 | - | DIME |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| R/W | R/W | R/W | W | W | R/W | R/W | | R |

- DIME: DMA Master Enable
- DIE1, DIE0: DMA Interrupt Enable 1, 0
- /DWE1, /DWE0: DMA Enable Bit Write Enable 1, 0
- DE1, DE0: DMA Enable Ch 1, 0

**Figure 40. DMA Status Register**

DMODE — Addr 31H

| Bit | - | - | DM1 | DM0 | SM1 | SM0 | MMOD | - |
|---|---|---|---|---|---|---|---|---|
| Upon Reset | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| R/W | | | R/W | R/W | R/W | R/W | R/W | |

- MMOD: Memory MODE Select
- SM1, SM0: Ch 0 Source Mode 1, 0
- DM1, DM0: Ch 0 Destination Mode 1, 0

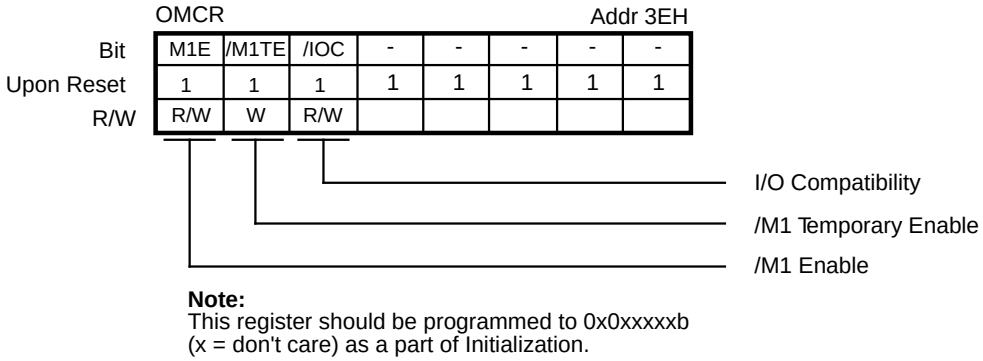
| DM1, 0 | Destination | Address |
|---|---|---|
| 00 | M | DAR0+1 |
| 01 | M | DAR0-1 |
| 10 | M | DAR0 Fixed |
| 11 | I/O | DAR0 Fixed |

| SM1, 0 | Source | Address |
|---|---|---|
| 00 | M | SAR0+1 |
| 01 | M | SAR0-1 |
| 10 | M | SAR0 Fixed |
| 11 | I/O | SAR0 Fixed |

| MMOD | Mode |
|---|---|
| 0 | Cycle Steal Mode |
| 1 | Burst Mode |

**Figure 41. DMA Mode Registers**

## SYSTEM CONTROL REGISTERS (Continued)




**Note:**
This register should be programmed to 0x0xxxxxb (x = don't care) as a part of Initialization.

**Figure 49. Operation Mode Control Register**

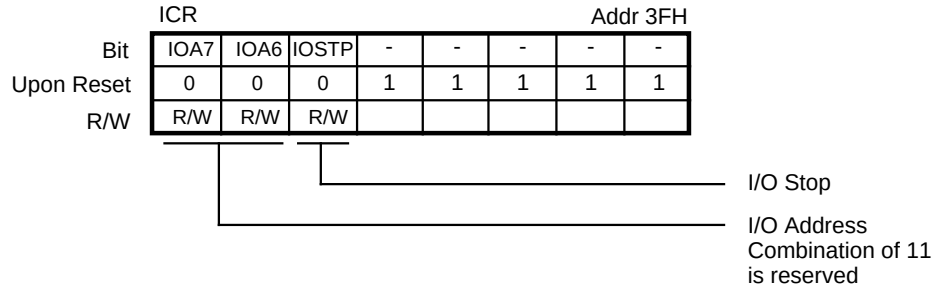



**Figure 50. I/O Control Register**

## ADDITIONAL FEATURES ON THE Z182 MPU

The following is a detailed description of the enhancements to the Z8S180 from the standard Z80180 in the areas of STANDBY, IDLE, and STANDBY-QUICK RECOVERY modes.

### Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce the current consumption. The Z8S180 has added two additional power-down modes, STANDBY and IDLE, to reduce the current consumption even further. The differences among these power-down modes are summarized in Table 10.

**Table 10. Power Down Modes**

| Power-Down Modes | CPU Core | On-Chip I/O | OSC. | CLKOUT | Recovery Source | Recovery Time (Minimum) |
|---|---|---|---|---|---|---|
| SLEEP | Stop | Running | Running | Running | RESET, Interrupts | 1.5 Clock |
| I/O STOP | Running | Stop | Running | Running | By Programming | - |
| SYSTEM STOP | Stop | Stop | Running | Running | RESET, Interrupts | 1.5 Clock |
| IDLE† | Stop | Stop | Running | Stop | RESET, Interrupts, BUSREQ | 8 +1.5 Clock |
| STANDBY† | Stop | Stop | Stop | Stop | RESET, Interrupts, BUSREQ | $2^{17}$ +1.5 Clock (Normal Recovery)<br>$2^{6}$ +1.5 Clock (Quick Recovery) |

**Notes:**
† IDLE and STANDBY modes are only offered in Z8S180. Note that the minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.

### STANDBY Mode

The Z8S180 has been designed to save power. Two low-power programmable power-down modes have been added; STANDBY mode and IDLE mode. The STANDBY/IDLE mode is selected by multiplexing D6 and D3 of the CPU Control Register (CCR, I/O Address = 1FH). To enter STANDBY mode:

1. Set D6 and D3 to 1 and 0, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY mode, it behaves similar to the SYSTEM STOP mode which currently exists on the Z80180, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to typically 50 μA..

Since the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter has been added in the Z8S180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down $2^{17}$ counts before acknowledgment is sent to the interrupt source.

The recovery source needs to remain asserted for duration of the $2^{17}$ count, otherwise standby will be resumed.

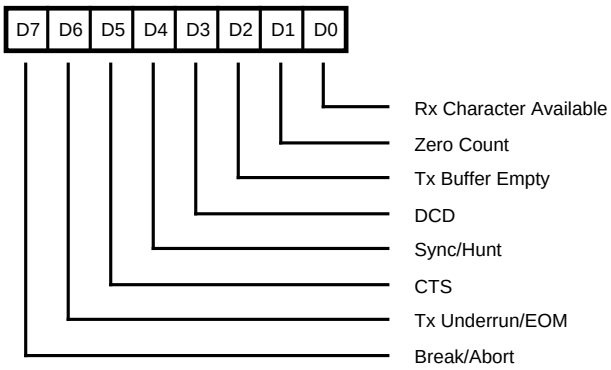
The following is a description of how the part exits STANDBY for different interrupts and modes of operation.

### STANDBY Mode Exit with /RESET

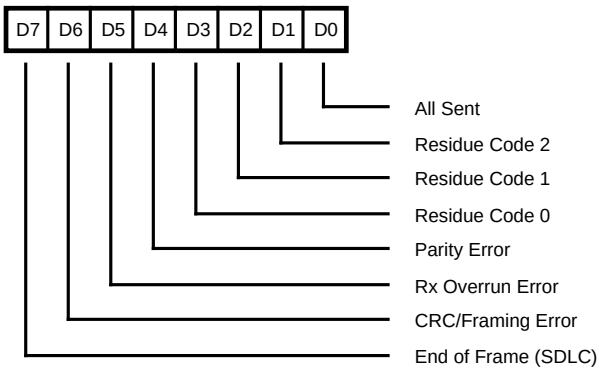
The /RESET input needs to be asserted for a duration long enough for the crystal oscillator to stabilize and then exit from the STANDBY mode. When /RESET is de-asserted, it goes through the normal reset timing to start instruction execution at address (logical and physical) 0000H.

The clocking is resumed within the Z8S180 and at the system clock output after /RESET is asserted when the crystal oscillator is restarted, but not yet stabilized.

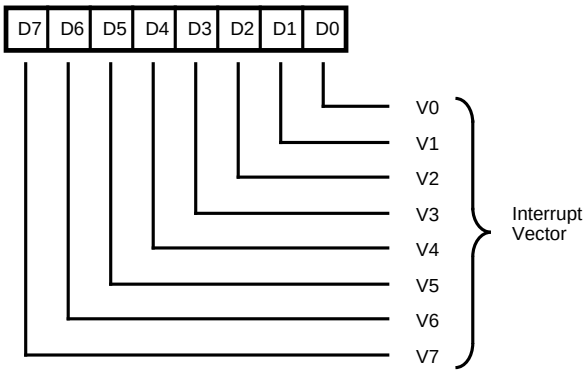
Read Register 0



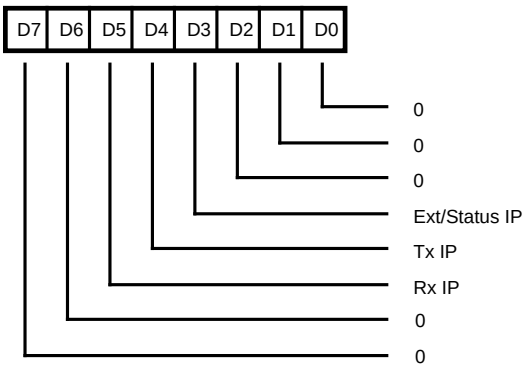

Read Register 1



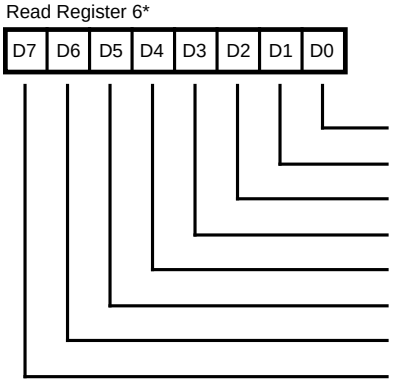

Read Register 2




Read Register 3



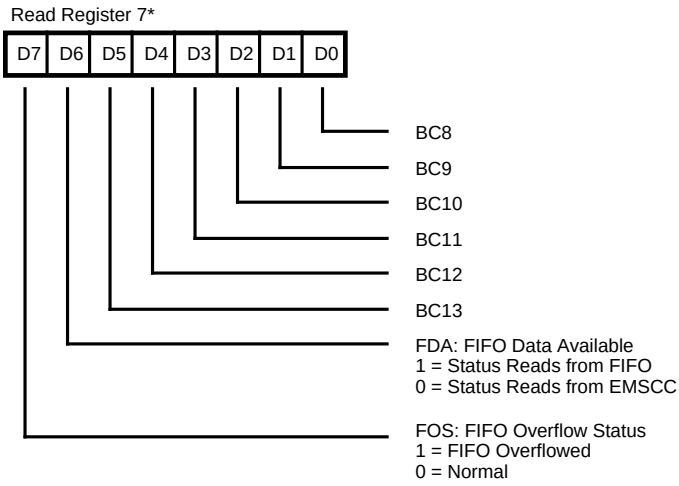

Read Register 6*




*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

**SDLC FIFO Status and Byte Count (LSB)**

Read Register 7*




*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

**SDLC FIFO Status and Byte Count (LSB)**

**Figure 52. Write Register Bit Functions** (Continued)

## CONTROL REGISTERS (Continued)

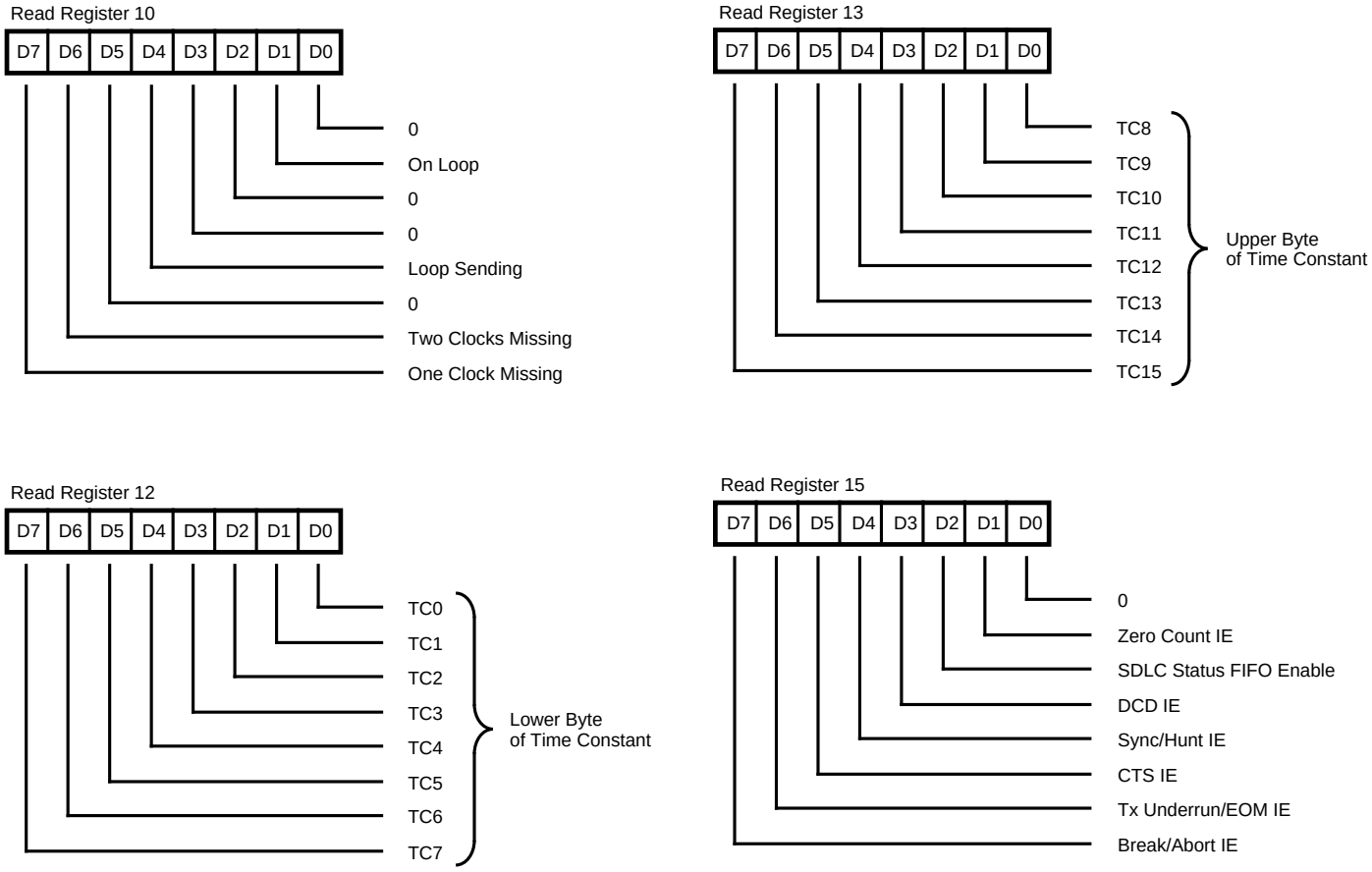



**Figure 53. Read Register Bit Functions**

Although this bit is disabled by default, it is advised that this bit is enabled to prevent interrupt conflict between MIMIC and ESCC interrupts.

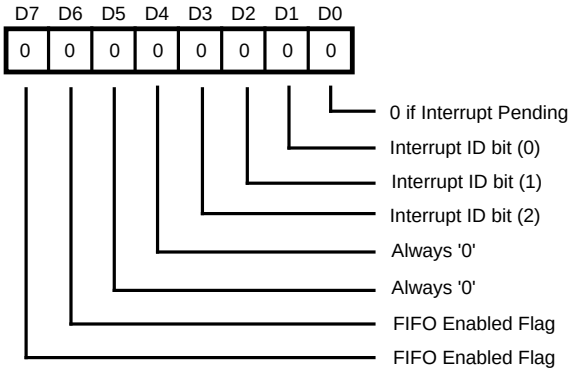



**Figure 73. Interrupt Identification Register**
(PC Read Only, Address 02H)
(Z180 MPU no access)

## Interrupt Identification Register

**Bit 7 and Bit 6 FIFO's Enabled**
These bits will read 1 if the FIFO mode is enabled on the MIMIC.

**Bit 5 and Bit 4 Always Read 0**
Reserved bits.

**Bits 3-1 Interrupt ID Bits**
This 3-bit field is used to determine the highest priority interrupt pending (see Table 19).

**Bit 0 Interrupt Pending**
This bit is logic 0 and interrupt is pending.

When the PC accesses the IIR, the contents of the register and all pending interrupts are frozen. Any new interrupts will be recorded, but not acknowledged, during the IIR access.

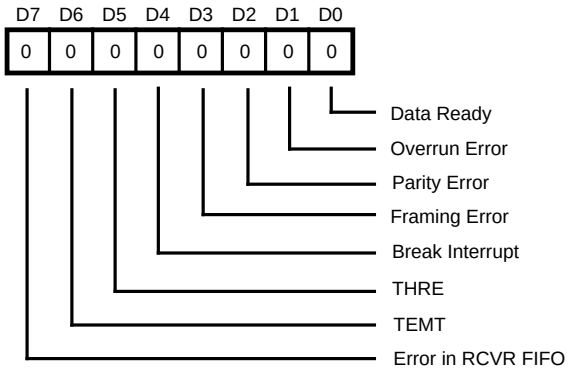



**Figure 74. Line Status Register**
(PC Read Only, Address 05H)
(Z180 MPU Read/Write bits 6, 4, 3, 2, Address xxF5H)

**Table 19. Interrupt Identification Field**

| b3 | b2 | b1 | Priority | Interrupt Source | INT Reset Control |
|---|---|---|---|---|---|
| 0 | 1 | 1 | Highest | Overrun, Parity, Framing error or Break detect bits set by MPU | Read Line Status Register |
| 0 | 1 | 0 | 2nd | Received Data trigger level | RCVR FIFO drops below trigger level |
| 1 | 1 | 0 | 2nd | Receiver Timeout with data in RCVR FIFO. | Read RCVR FIFO |
| 0 | 0 | 1 | 3rd | Transmitter Holding Register Empty. | Writing to the Transmitter Holding Register or reading the Interrupt Identification Register when the THRE is the source of the interrupt. |
| 0 | 0 | 0 | 4th | MODEM status: CTS, DSR, RI or DCD | Reading the MODEM status register. |

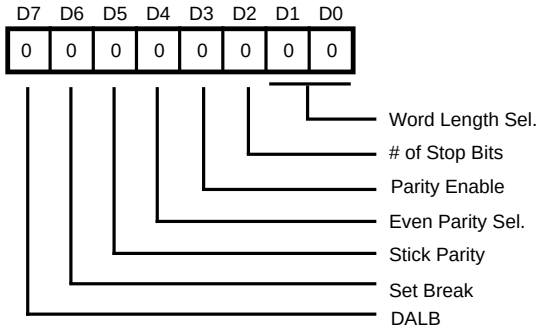



**Figure 76. Line Control Register**
(PC Read/Write, Address 03H)
(Z180 MPU Read Only, Address xxF3H)

## Line Control Register

**Bit 7 Divisor Latch Access Bit (DALB)**
This bit allow access to the divisor latch by the PC/XT/AT. If this bit is set to 1, access to the Transmitter, Receiver and Interrupt Enable Registers is disabled. When an access is made to address 0 the Divisor Latch Least Significant byte is accessed. If an access is made to address 1, the Divisor Latch Most Significant byte is accessed.

**Bit 6 - Bit 0**
These bits do not affect the Z80182/Z8L182 directly, however they can be read by the Z180 MPU and the 16550 MIMIC modes can be emulated by the Z180 MPU.

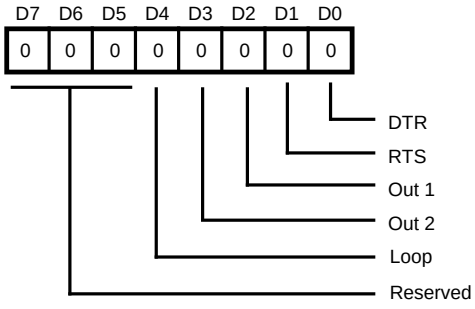



**Figure 77. Modem Control Register**
(PC Read/Write, Address 04H)
(Z180 MPU Read Only, Address xxF4H)

## Modem Control Register

**Bit 7-5 Reserved**
Reserved for future use, always 0.

**Bit 4 Loop**
When this bit is set to 1, D3-D0 field reflects the status of Modem Status Register, as follows:

RI = Out 1
DCD = Out 2
DSR = DTR
CTS = RTS

Emulation of the 16550 UART loop back feature must be done by the Z180 MPU, except in the above conditions.

**Bit 3 Out 2**
This bit controls the tri-state on the HINTR pin if bits 2 and 1 are 10. Otherwise it can be read by the Z180 MPU.

**Bits 2, 1, 0**
These bits have no direct control of the 16550 MIMIC interface and the Z180 MPU must emulate the function if it is to be implemented.

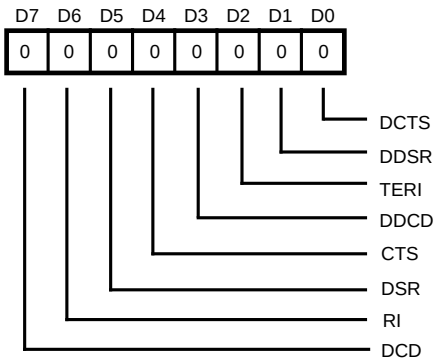



**Figure 78. Modem Status Register**
(PC Read Only, Address 06H)
(Z180 MPU Read/Write bits 7-4, Address xxF6H)

## PARALLEL PORTS REGISTERS

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output. The Ports consist of two registers the Port Direction Control Register and the Port Data Register. The Port and direction register can be accessed in any page of I/O space since only the lowest eight address lines are decoded. Bits PC7 and PC6 are input only bits and have the special function of reading the external value of the /INT2 and /INT1 pins. Writing '1' to these bits will clear the edge detect interrupt logic when operating /INT2 and/or /INT1 in edge detect mode.

When Port B and Port C bits 5-0 are deselected in the System Configuration Register, the Data and Data Direction Registers are still available as read/write scratch registers. If a Port is deselected and if the DDR bit is a '0', then the written value to that bit will be latched and this value can be read back. If a Port is deselected and if the DDR bit is a '1', then you could read only the external pin value; any write to that bit is latched but can be read back only with DDR=0.

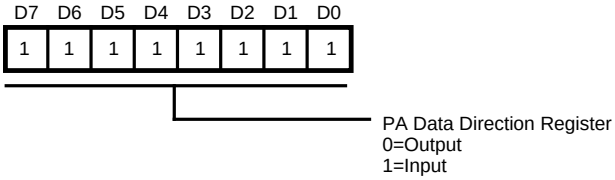



**Figure 83. PA, Port A, Data Direction Register**
(Z180 MPU Read/Write, Address xxEDH)

The data direction register determines which are inputs and outputs in the PA Data Register. When a bit is set to 1 the corresponding bit in the PA Data Register is an input. If the bit is 0, then the corresponding bit is an output.

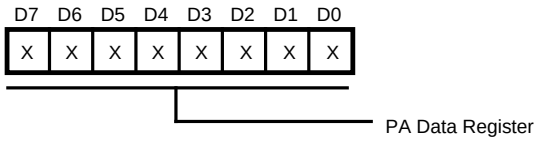



**Figure 84. PA, Port A, Data Register**
(Z180 MPU Read/Write, Address xxEEH)

When the Z180 MPU writes to the PA Data Register the data is stored in the internal buffer. The values of the PA Data Register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PA Data Register the data on the external pins is returned.

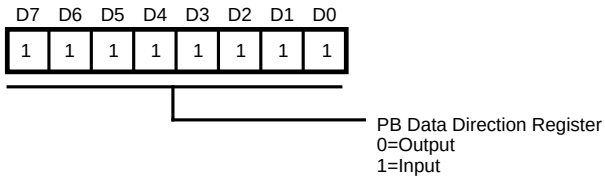



**Figure 85. PB, Port B, Data Direction Register**
(Z180 MPU Read/Write, Address xxE4H)

The data direction register determines which are inputs and outputs in the PB Data Register. When a bit is set to 1 the corresponding bit in the PB Data Register is an input. If the bit is 0 then the corresponding bit is an output.

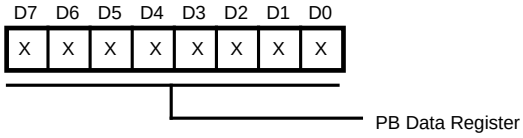



**Figure 86. PB, Port B, Data Register**
(Z180 MPU, Address xxE5H)

When the Z180 MPU writes to the PB Data Register the data is stored in the internal buffer. The values of Port B data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PB Data Register, the data on the external pins is returned.

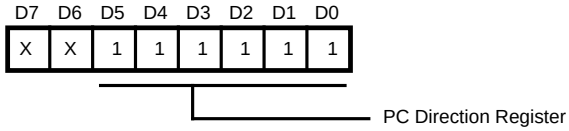



**Figure 87. PC, Port C, Data Direction Register**
(Z180 MPU Read/Write, Address xxDDH)

## Z8S180 AC CHARACTERISTICS

**Table A. Z8L180 and Z8S180 Timings**

| No. | Sym | Parameter | Z8L180 20 MHz Min | Z8L180 20 MHz Max | Z8S180 33 MHz Min | Z8S180 33 MHz Max | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| 1 | tcyc | Clock Cycle Time | 50 | 2000 | 30 | 2000 | ns | [1] |
| 2 | tCHW | Clock Pulse Width (High) | 15 | | 10 | | ns | [1] |
| 3 | tCLW | Clock Pulse Width (Low) | 15 | | 10 | | ns | [1] |
| 4 | tcf | Clock Fall Time | | 10 | | 5 | ns | [1] |
| 5 | tcr | Clock Rise Time | | 10 | | 5 | ns | [1] |
| 6 | tAD | Address Valid from Clock Rise | | 15 | | 15 | ns | |
| 7 | tAS | Address Valid to /MREQ, /IORQ, /MRD Fall | 5 | | 5 | | ns | |
| 8 | tMED1 | Clock Fall to /MREQ Fall Delay | | 15 | | 10 | ns | |
| 9 | tRDD1 | Clock Fall to /RD, /MRD (/IOC=1) | | 25 | | 15 | ns | |
| | | Clock Rise to /RD, /MRD Fall (/IOC=0) | | 35 | | 15 | ns | |
| 10 | tM1D1 | Clock Rise to /M1 Fall delay | | 35 | | 15 | ns | |
| 11 | tAH | Address Hold time (/MREQ, /IORQ, /RD, /WR/MRD) | 5 | | 5 | | ns | |
| 12 | tMED2 | Clock Fall to /MREQ Rise Delay | | 25 | | 15 | ns | |
| 13 | tRDD2 | Clock Fall to /RD, /MRD Rise Delay | | 25 | | 15 | ns | |
| 14 | tM1D2 | Clock Rise to /M1 Rise Delay | | 40 | | 15 | ns | |
| 15 | tDRS | Data Read Setup Time | 15 | | 15 | | ns | |
| 16 | tDRH | Data Read Hold Time | 0 | | 0 | | ns | |
| 17 | tSTD1 | Clock Edge to ST Fall | | 30 | | 15 | ns | |
| 18 | tSTD2 | Clock Edge to ST Rise | | 30 | | 15 | ns | |
| 19 | tWS | /WAIT Setup Time to Clock Fall | 15 | | 10 | | ns | [2] |
| 20 | tWH | /WAIT Hold Time from Clock Fall | 10 | | 5 | | ns | |
| 21 | tWDZ | Clock Rise to Data Float Delay | | 35 | | 20 | ns | |
| 22 | tWRD1 | Clock Rise to /WR,/MWR Fall Delay | | 25 | | 15 | ns | |
| 23 | tWDD | Clock Fall to Write Data Delay | | 25 | | 15 | ns | |
| 24 | tWDS | Write Data Setup Time to /WR,/MWR Fall | 10 | | 10 | | ns | |
| 25 | tWRD2 | Clock Fall to /WR Rise | | 25 | | 15 | ns | |
| 26 | tWRP | /WR Pulse Width (Memory Write Cycles) | 75 | | 45 | | ns | |
| 26a | | /WR Pulse Width (I/O Write Cycles) | 130 | | 70 | | ns | |
| 27 | tWDH | Write Data Hold Time from /WR Rise | 10 | | 5 | | ns | |
| 28 | tIOD1 | Clock Fall to /IORQ Fall Delay (/IOC=1) | | 25 | | 15 | ns | |
| | | Clock Rise to /IORQ Fall Delay (/IOC=0) | | 25 | | 15 | ns | |
| 29 | tIOD2 | Clock Fall /IOQR Rise Delay | | 25 | | 15 | ns | |
| 30 | tIOD3 | /M1 Fall to /IORQ Fall Delay | 100 | | 80 | | ns | |
| 31 | tINTS | /INT Setup Time to Clock Fall | 20 | | 15 | | ns | |
| 32 | tINTH | /INT Hold Time from Clock Fall | 10 | | 10 | | ns | |
| 33 | tNMIW | /NMI Pulse Width | 35 | | 25 | | ns | |
| 34 | tBRS | /BUSREQ Setup Time to Clock Fall | 10 | | 10 | | ns | |
| 35 | tBRH | /BUSREQ Hold Time from Clock Fall | 10 | | 10 | | ns | |
| 36 | tBAD1 | Clock Rise to /BUSACK Fall Delay | | 25 | | 15 | ns | |
| 37 | tBAD2 | Clock Fall to /BUSACK Rise Delay | | 25 | | 15 | ns | |
| 38 | tBZD | Clock Rise to Bus Floating Delay Time | | 40 | | 30 | ns | |
| 39 | tMEWH | /MREQ Pulse Width (High) | 35 | | 25 | | ns | |
| 40 | tMEWL | /MREQ Pulse Width (Low) | 35 | | 25 | | ns | |

## General-Purpose I/O Port Timing

This figure shows the timing for the Ports A, B and C. Parameters referred to in this figure appear in Tables D and E.

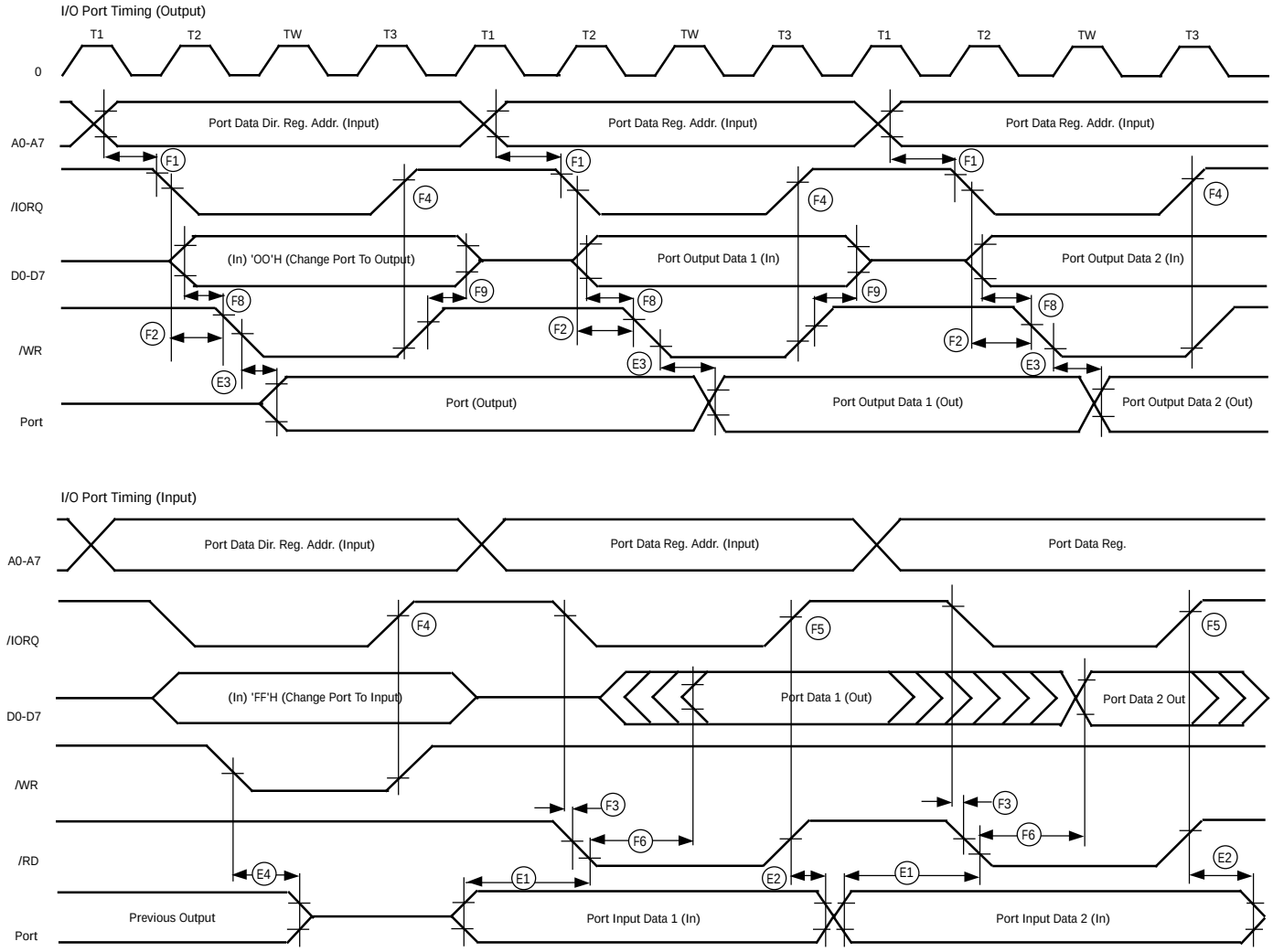



**Figure 107. PORT Timing**

## Read Write External Bus Master Timing

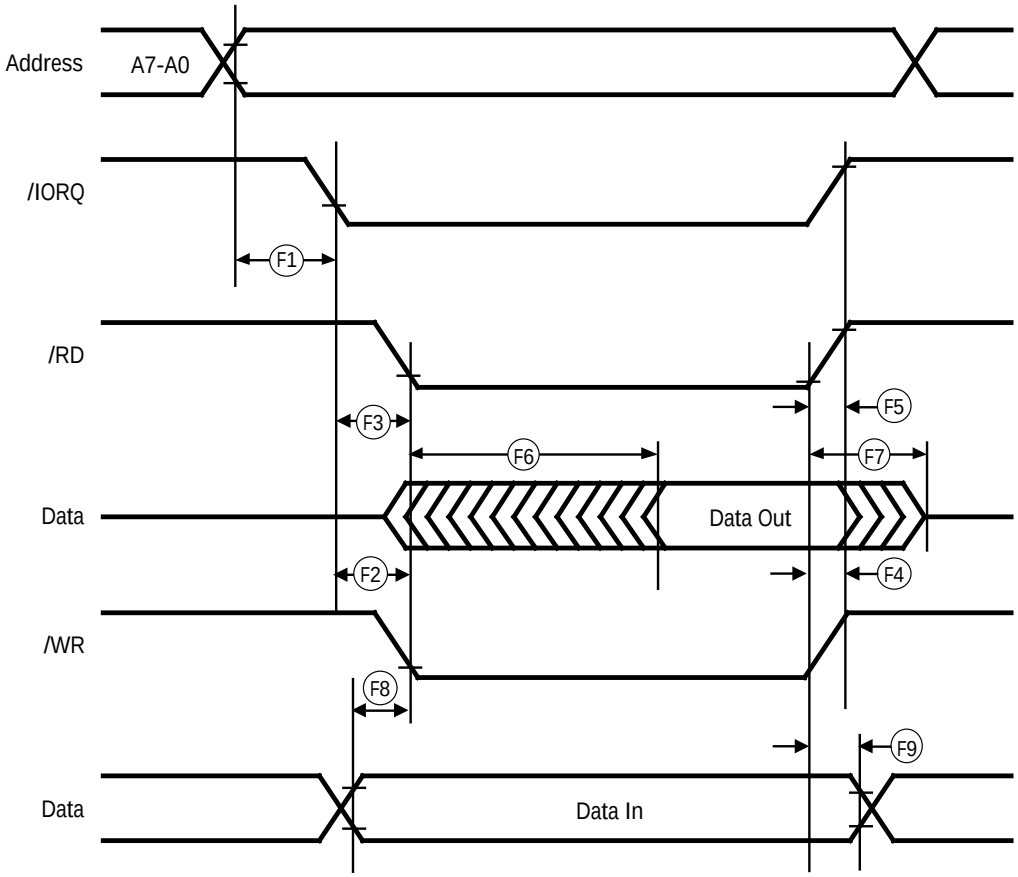



**Figure 108. Read/Write External Bus Master Timing**

## 16550 MIMIC TIMING

Refer to Figures 106 thru 112 for MIMIC AC Timing.

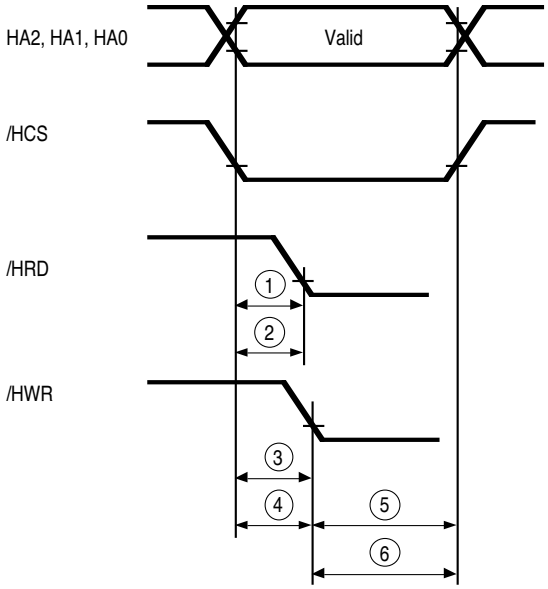



**Figure 110. PC Host /RD /WR Timing**

**Table H. PC Host /RD /WR Timing**

| No | Symbol | Parameter | Z8L182 20 MHz Min | Z8L182 20 MHz Max | Z80182 33 MHz Min | Z80182 33 MHz Max | Units |
|---|---|---|---|---|---|---|---|
| 1 | tAR | /HRD Delay from Address | 30 | | 30 | | ns |
| 2 | tCSR | /HRD Delay from /HCS | 30 | | 30 | | ns |
| 3 | tAW | /HWR Delay from Address | 30 | | 30 | | ns |
| 4 | tCSW | /HWR Delay from /HCS | 30 | | 30 | | ns |
| 5 | tAh | Address Hold Time | 20 | | 20 | | ns |
| 6 | tCSh | /HCS Hold Time | 20 | | 20 | | ns |

**Note:**
These AC parameter values are preliminary and are subject to change without notice.