Zilog - Z8018233FSC00TR Datasheet

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018233fsc00tr

GENERAL DESCRIPTION (Continued)

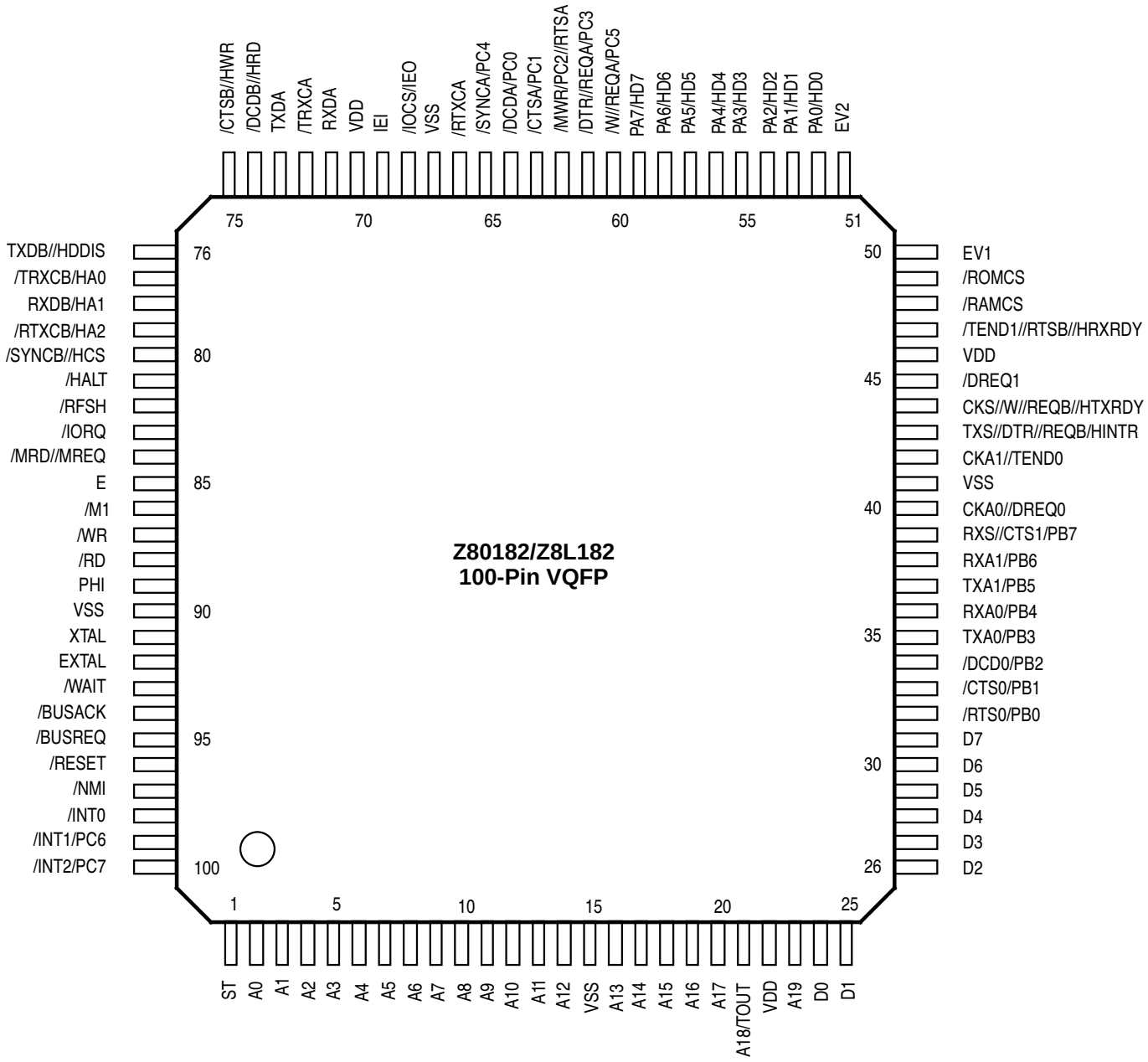


Figure 3. Z80182/Z8L182 100-Pin VQFP Pin Configuration

Z180 MPU DMA SIGNALS

/TEND0. *Transfer End 0 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND0 is multiplexed with CKA1 on the CKA1//TEND0 pin.

/TEND1. *Transfer End 1 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND1 is multiplexed with the ESCC signal /RTSB and the 16550 MIMIC interface signal /HRxRDY on the /TEND1//RTSB//HRxRDY pin.

/DREQ0. *DMA request 0 (input, active Low).* /DREQ0 is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. /DREQ0 is multiplexed with CKA0 on the CKA0//DREQ0 pin.

/DREQ1. *DMA request 1 (input, active Low).* /DREQ1 is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

Z180™ MPU TIMER SIGNALS

$T_{OUT.}$ *Timer Out (output, active High).* T_{OUT} is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/T_{OUT} pin.

Z85230 ESCC™ SIGNALS

TxDA. *Transmit Data (output, active High).* This output signal transmits channel A's serial data at standard TTL levels. This output can be tri-stated during power down modes.

TxDB. *Transmit Data (output, active High).* This output signal transmits channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface /HDDIS signal on the TxDB//HDDIS pin.

RxDA. *Receive Data (inputs, active High).* These inputs receive channel A's serial data at standard TTL levels.

RxDB. *Receive Data (input, active High).* These inputs receive channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB/HA1 pin.

/TRxCA. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel A program control. /TRxCA may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/TRxCB. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel B program control. /TRxCB may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in output mode. In Z80182/Z8L182 mode 1 /TRxCB is multiplexed with the 16550 MIMIC interface HA0 input on the /TRxCB/HA0 pin.

/RTxCA. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel A program control. In channel A, /RTxCA may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCA pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

/RTxCB. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel B program control. In channel B, /RTxCB may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCB pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182/Z8L182 mode 1 the /RTxCB signal is multiplexed with 16550 MIMIC interface HA2 input on the /RTxCB/HA2 pin.

/W//REQB. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

16550 MIMIC INTERFACE SIGNALS

HD7-HD0. *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

/HDDIS. *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

HA2-HA0. *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

/HCS. *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

/HWR. *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

/HRD. *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

HINTR. *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

/HTxRDY. *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

/HRxRDY. *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

PARALLEL PORTS

PA7-PA0. *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

PC7-PC0. *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

MULTIPLEXED PIN DESCRIPTIONS (Continued)

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
41	44	V_{SS}			
42	45	CKA1//TEND0			
43	46	TxS	/DTR//REQB	HINTR	SYS CONF REG Bit 1,2
44	47	CKS	/W//REQB	/HTxRDY	SYS CONF REG Bit 1,2
45	48	/DREQ1			
46	49	V_{DD}			
47	50	/TEND1	/RTSB	/HRxRDY	SYS CONF REG Bit 1,2
48	51	/RAMCS			
49	52	/ROMCS			
50	53	EV1			
51	54	EV2			
52	55	PA0	HD0		SYS CONF REG Bit 1
53	56	PA1	HD1		SYS CONF REG Bit 1
54	57	PA2	HD2		SYS CONF REG Bit 1
55	58	PA3	HD3		SYS CONF REG Bit 1
56	59	PA4	HD4		SYS CONF REG Bit 1
57	60	PA5	HD5		SYS CONF REG Bit 1
58	61	PA6	HD6		SYS CONF REG Bit 1
59	62	PA7	HD7		SYS CONF REG Bit 1
60	63	/W//REQA	PC5		SYS CONF REG Bit 7
61	64	/DTR//REQA	PC3		SYS CONF REG Bit 7
62	65	/MWR	PC2	RTSA	SYS CONF REG Bit 7 *
63	66	/CTSA	PC1		SYS CONF REG Bit 7
64	67	/DCDA	PC0		SYS CONF REG Bit 7
65	68	/SYNCA	PC4		SYS CONF REG Bit 7
66	69	/RTxCA			
67	70	V_{SS}			
68	71	/IOCS	IEO		INT EDG/PIN REG Bit 2
69	72	IEI			
70	73	V_{DD}			

Z182 MPU CONTROL REGISTERS

Figures 10 through 50 refer to the Z80182/Z8L182 MPU Control registers. For additional information, refer to the Z8S180 Product Specification and Technical Manual.

ASCI CHANNELS CONTROL REGISTERS

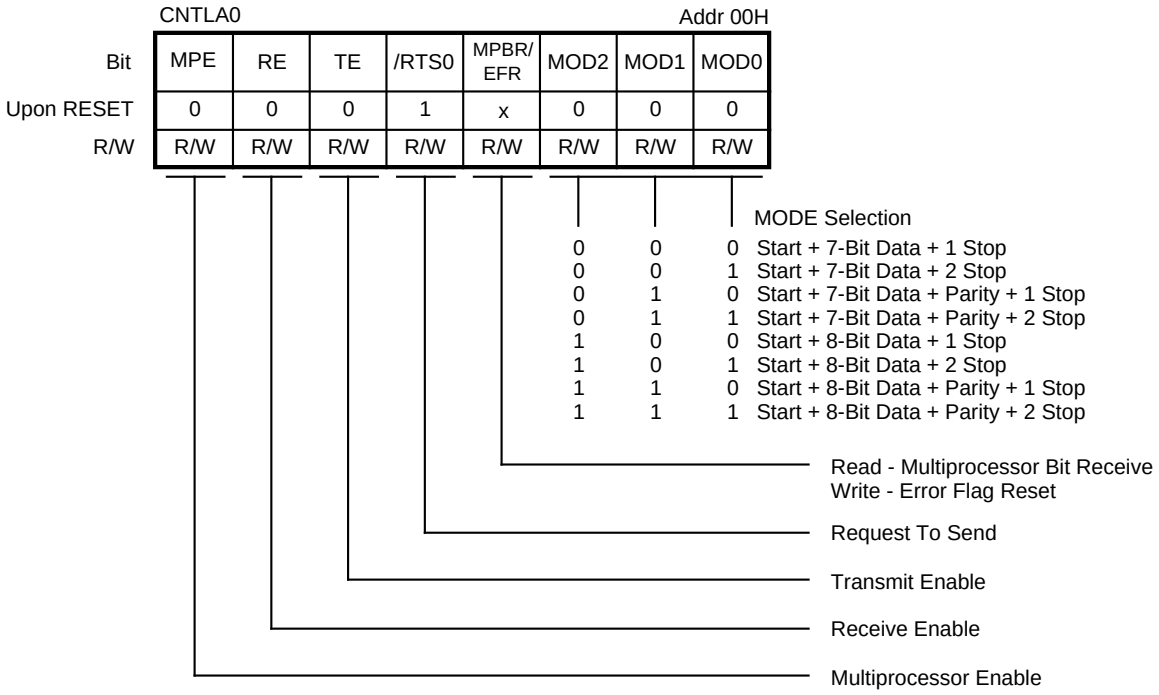


Figure 10a. ASCI Control Register A (Ch. 0)

ASCI CHANNELS CONTROL REGISTERS (Continued)

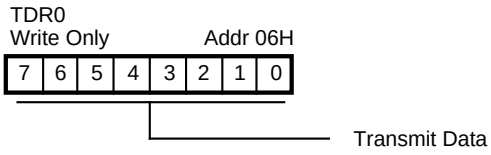


Figure 15. ASCI Transmit Data Register (Ch. 0)

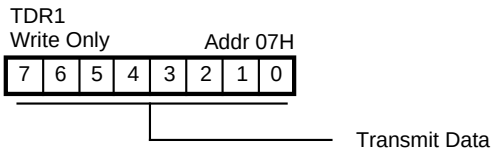


Figure 16. ASCI Transmit Data Register (Ch. 1)

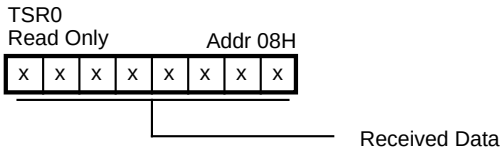


Figure 17. ASCI Receive Data Register (Ch. 0)

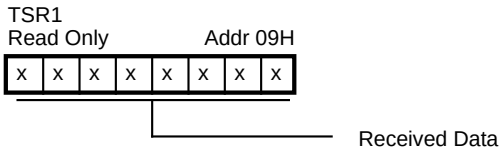


Figure 18. ASCI Receive Data Register (Ch. 1)

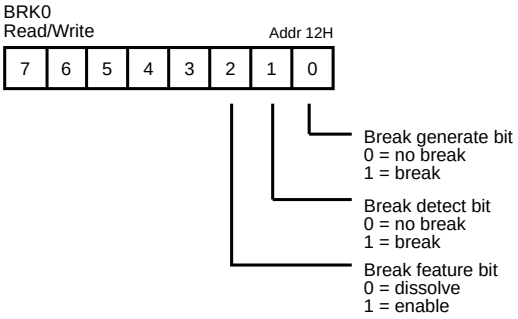


Figure 19. ASCI Break Control Register (Ch. 0)

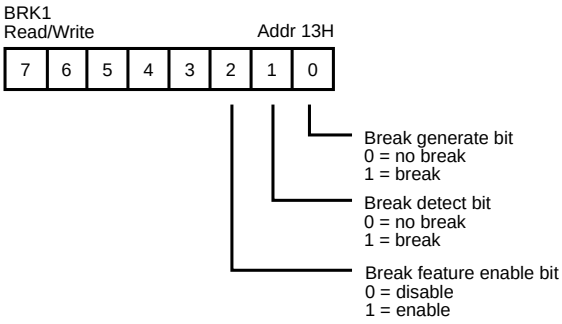
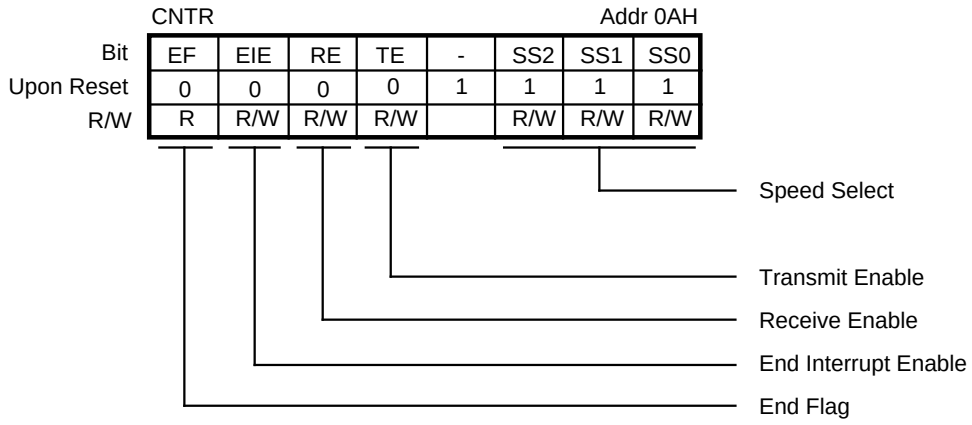


Figure 20. ASCI Break Control Register (Ch. 1)

CSI/O REGISTERS



SS2, 1, 0	Baud Rate
000	Ø ÷ 20
001	Ø ÷ 40
010	Ø ÷ 80
011	Ø ÷ 100

SS2, 1, 0	Baud Rate
100	Ø ÷ 320
101	Ø ÷ 640
110	Ø ÷ 1280
111	External Clock (Frequency < Ø ÷ 20)

Figure 21. CSI/O Control Register

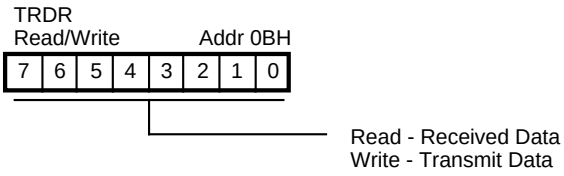


Figure 22. CSI/O Transmit/Receive Data Register

FREE RUNNING COUNTER

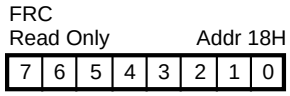


Figure 32. Free Running Counter

CPU CONTROL REGISTER

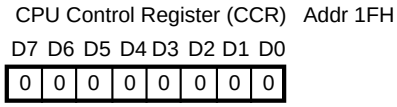
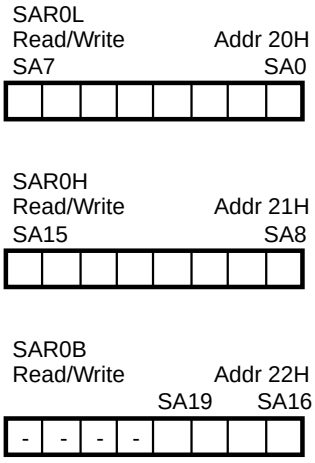


Figure 33. CPU

Note: See Figure 49 for full description.

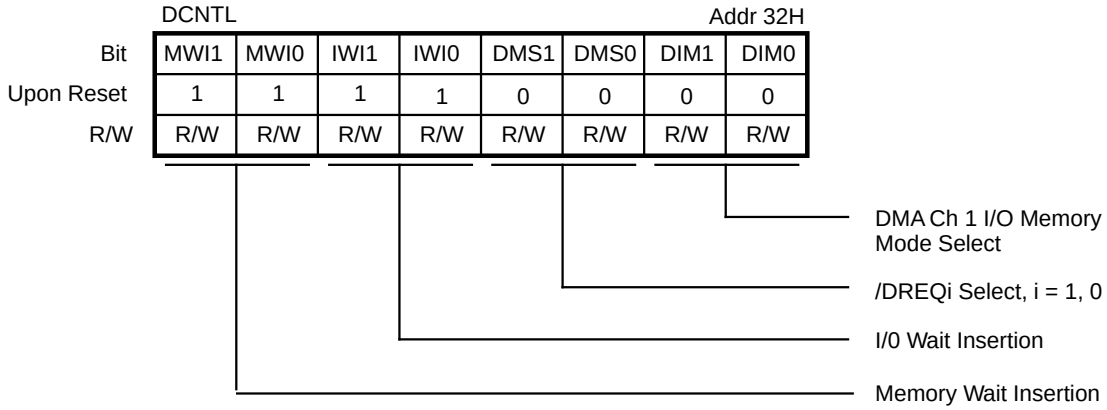
DMA REGISTERS



Bits 0-2 (3) are used for SAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	RDR1 (ASCI1)
x	x	1	1	Not Used

Figure 34. DMA 0 Source Address Registers



*

MWI1, 0	No. of Wait States
00	0
01	1
10	2
11	3

IWI1, 0	No. of Wait States
00	1
01	2
10	3
11	4

DMSi	Sense
1	Edge Sense
0	Level Sense

DM1, 0	Transfer Mode	Address Increment/Decrement	
00	M - I/O	MAR1+1	IAR1 Fixed
01	M - I/O	MAR1-1	IAR1 Fixed
10	I/O - M	IAR1 Fixed	MAR1+1
11	I/O - M	IAR1 Fixed	MAR1-1

Note:
* If using ROM/RAM Chip Select wait state generators, the Z180 wait state generator should be set to 0.

Figure 42. DMA/WAIT Control Register

ADDITIONAL FEATURES ON THE Z182 MPU

The following is a detailed description of the enhancements to the Z8S180 from the standard Z80180 in the areas of STANDBY, IDLE, and STANDBY-QUICK RECOVERY modes.

Add-On Features

There are five different power-down modes. SLEEP and SYSTEM STOP are inherited from the Z80180. In SLEEP mode, the CPU is in a stopped state while the on-chip I/Os are still operating. In I/O STOP mode, the on-chip I/Os are in a stopped state while leaving the CPU running. In SYSTEM STOP mode, both the CPU and the on-chip I/Os are in the stopped state to reduce the current consumption. The Z8S180 has added two additional power-down modes, STANDBY and IDLE, to reduce the current consumption even further. The differences among these power-down modes are summarized in Table 10.

Table 10. Power Down Modes

Power-Down Modes	CPU Core	On-Chip I/O	OSC.	CLKOUT	Recovery Source	Recovery Time (Minimum)
SLEEP	Stop	Running	Running	Running	RESET, Interrupts	1.5 Clock
I/O STOP	Running	Stop	Running	Running	By Programming	-
SYSTEM STOP	Stop	Stop	Running	Running	RESET, Interrupts	1.5 Clock
IDLE†	Stop	Stop	Running	Stop	RESET, Interrupts, BUSREQ	8 +1.5 Clock
STANDBY†	Stop	Stop	Stop	Stop	RESET, Interrupts, BUSREQ	2^{17} +1.5 Clock (Normal Recovery) 2^{6} +1.5 Clock (Quick Recovery)

Notes:
† IDLE and STANDBY modes are only offered in Z8S180. Note that the minimum recovery time can be achieved if INTERRUPT is used as the Recovery Source.

STANDBY Mode

The Z8S180 has been designed to save power. Two low-power programmable power-down modes have been added; STANDBY mode and IDLE mode. The STANDBY/IDLE mode is selected by multiplexing D6 and D3 of the CPU Control Register (CCR, I/O Address = 1FH). To enter STANDBY mode:

1. Set D6 and D3 to 1 and 0, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY mode, it behaves similar to the SYSTEM STOP mode which currently exists on the Z80180, except that the STANDBY mode stops the external oscillator, internal clocks and reduces power consumption to typically 50 μA..

Since the clock oscillator has been stopped, a restart of the oscillator requires a period of time for stabilization. An 18-bit counter has been added in the Z8S180 to allow for oscillator stabilization. When the part receives an external IRQ or BUSREQ during STANDBY mode, the oscillator is restarted and the timer counts down 2^{17} counts before acknowledgment is sent to the interrupt source.

The recovery source needs to remain asserted for duration of the 2^{17} count, otherwise standby will be resumed.

The following is a description of how the part exits STANDBY for different interrupts and modes of operation.

STANDBY Mode Exit with /RESET

The /RESET input needs to be asserted for a duration long enough for the crystal oscillator to stabilize and then exit from the STANDBY mode. When /RESET is de-asserted, it goes through the normal reset timing to start instruction execution at address (logical and physical) 0000H.

The clocking is resumed within the Z8S180 and at the system clock output after /RESET is asserted when the crystal oscillator is restarted, but not yet stabilized.

Z85230 ESCC™ CONTROL REGISTERS

See Figures 52 and 53 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification /Technical Manual.

The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. ***It is recommended that /TRxCB be programmed as an output with proper baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.***

Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

PROGRAMMING THE ESCC™

The ESCC contains write registers in each channel that are programmed by the system separately to configure the functional uniqueness of the channels.

In the ESCC, the data registers are directly addressed by selecting a High on the D//C pin. With all other registers (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers, both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected read register accessed. All of the ESCC registers, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

With the Z80182/Z8L182, a new feature is implemented in the ESCC. The Transmitter and Receiver is now capable of sending and comparing a 32-bit CRC-32 (Ethernet Polynomial):

$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

This feature is enabled by access to WR7' Bit 7, which selects the 32-bit CRC polynomial for the transmitter and receiver and overrides any selection of SDLC/CRC-16 CRCs. When the 32-bit CRC override feature is enabled, the transmitter will only send 32-bit CRC when CRC is to be sent. On the receive side, the CRC comparison/calculation will be done only on 32-bit CRC values. The result of the 32-bit CRC comparison will be maintained in RR1 bit D6 in place of the 16-bit CRC comparison result. The 32-bit CRC compare result will also be maintained in the 10x19 FIFO for frames in which 32-bit CRC is enabled. The CRC still can be preset to all 0s or all 1s. 32-bit CRC is disabled upon power-up or reset.

Note: The ESCC cannot do simultaneous calculation/ comparison using both 16-bit and 32-bit CRC.

Also, for the Z80182/Z8L182 only, the clock provided to the ESCC core is equal to the system clock divided by 1 or 2. The divider is programmed in the Z80182 Enhancement Register bit 3.

Divide-by-two should be programmed when running the Z182 beyond:

- 20 MHz, 5V
- 10 MHz, 3V

Note: Upon power-up or reset the system clock is equal to the ESCC clock.

Initialization. The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, in the Asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity should be set first. Then the interrupt mode is set, and finally, the receiver and transmitter are enabled.

Write Registers. The ESCC contains 16 write registers (17 counting the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. There are two registers (WR2 and WR9) shared by the two channels that are accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits and reset commands. A new register, WR7', was added to the ESCC and may be written to if WR15, D0 is set. Figure 50 shows the format of each write register.

Read Registers. The ESCC contains ten read registers (eleven, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) are read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (channel A) or the vector modified by status information (channel B). RR3 contains the Interrupt Pending (IP) bits (channel A only). RR6 and RR7 contain the information in the SDLC Frame Status FIFO, but is only read when WR15, D2 is set. If WR7' D6 is set, Write Registers WR3, WR4, WR5, WR7, and WR10 can be read as RR9, RR4, RR5, and RR14, respectively. Figure 51 shows the format of each Read register.

IUS/IP Register

The IUS/IP Register is used by the Z180™ MPU to determine the source of the interrupt. This register will have the appropriate bit set when an interrupt occurs.

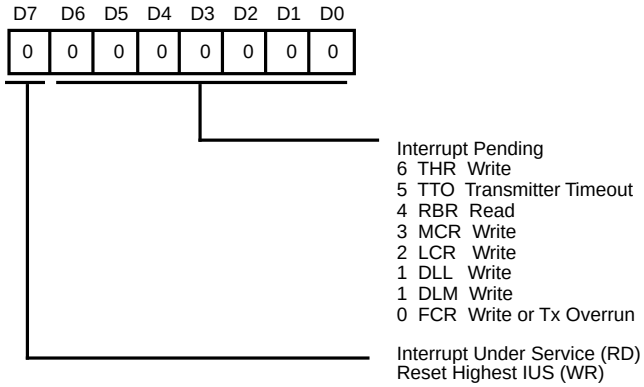


Figure 61. IUS/IP Register
(Z180 MPU, Address xxFEH)

Bit 7 Interrupt Under Service (Read/Write)
This bit represents a logical OR of each individual IUS bit for the internal MIMIC interrupt daisy chain. An IUS bit is set when an interrupt is registered (IP set) and enabled (IE set), the incoming IEI daisy chain is active (chain enabled) and an interrupt acknowledge cycle is entered. By writing a 1 to this bit the highest priority IUS bit that is set will be reset. Writing a 0 to this bit has no effect.

This should be done at the end of every MIMIC Interrupt Service routine.

Bit 6 Transmit Holding Register Written (Read Only)
This bit is set when the PC/XT/AT writes to the Transmit Holding Register. It is reset when the Z180 MPU reads the Transmit Holding Register. In FIFO mode, this bit is set when the trigger level is reached (4,8,14 bytes available). **Note:** The THR bit is set (interrupts) when the transmitter FIFO reaches the data available trigger level set in the MPU FCR control register. The bit and interrupt source is cleared when the number of data bytes falls below the set trigger level.

Bit 5 Transmitter Timeout with Data in FIFO (Read Only)
This bit is set when the transmitter FIFO has been idle (no read or write and timer decrements to zero) with data bytes below the trigger level. It is cleared when the FIFO is read or written.

Bit 4 Receive Buffer Read (Read Only)
This bit is set when the PC/XT/AT reads the Receive Buffer Register. It is reset when the Z180 MPU writes to the Receive Buffer Register. In FIFO mode, this bit is set upon the PC reading all the data in the receive FIFO. **Note:** RBR is set and interrupts when the receive FIFO has been emptied by the PC. This bit and interrupt are cleared when one or more bytes are written into the receive FIFO by the MPU.

Bit 3 Modem Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the Modem Control Register. It is reset when the Z180™ MPU reads the Modem Control Register.

Bit 2 Line Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the Line Control Register. It is reset when the Z180 MPU reads the Line Control Register.

Bit 1 Divisor Latch LS/MS Write (Read Only)
This bit is set when the PC/XT/AT writes to the Divisor Latch Least Significant or Most Significant bytes. It is reset when the PC reads the LS/MS register(s). To determine which byte(s) have been written, the Z180 must read either LS or MS locations and then repoll this bit. If only one location is interrupting, the interrupt is cleared when that location is read by the Z180.

Bit 0 FIFO Control Register Write (Read Only)
This bit is set when the PC/XT/AT writes to the FCR. This bit is also set when Transmit occurs. It is reset when the Z180 MPU reads this register.

16550 MIMIC REGISTERS (Continued)

Line Status Register

Bit 7 Error in RCVR FIFO
In 16450 mode, this bit will read logic 0. In 16550 mode this bit is set if at least one data byte is available in the FIFO with one of its associated error bits set. This bit will clear when there are no more errors (or break detects) in the FIFO.

Bit 6 Transmitter Empty
This bit must be set or reset by the MPU by a write to this register bit. If Double Buffer Mode is enabled, the TEMT bit is set/reset automatically. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 5 Transmit Holding Register Empty, THRE
This bit is set to 1 when either the THR has been read (emptied) by the MPU (16450 mode) or the XMIT FIFO is empty (16550 mode). This bit is set to 0 when either the THR or XMIT FIFO become non-empty. A shadow bit exists so that the register bit setting to 1 is delayed by the Transmitter Timer if enabled. The MPU when reading this bit will not see the delay. Both shadow and register bits are cleared when the PC writes to the THR of XMIT FIFO. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 2, 3, 4 Parity Error, Framing Error, Break Detect
These bits are written, indirectly, by the MPU as follows: The bits are first written to shadow bit locations when the MPU write accesses the LSR. When the next character is written to the Receive Buffer or RCVR FIFO, the data in the shadow bits is then copied to the LSR (16450 mode) or FIFO RAM (16550 mode). In FIFO mode bits become available to the PC when the data byte associated with the bits is next to be read (top of FIFO). In FIFO mode, with successive reads of the receiver, the status bits will be set if an error occurs on any byte. Once the MPU writes to the Receive Buffer or RCVR FIFO, the shadow bits are auto cleared. The register bits are cleared upon the PC reading the LSR. In FIFO mode these bits will be set if any byte has the respective error bit set while the PC reads multiple characters from the FIFO.

Bit 1 Overrun Error
This bit is set if the Z180 MPU makes a second write to the Receive Buffer before the PC reads the data in the Buffer (16450 mode) or with a full RCVR FIFO (16550 mode.) No data will be transferred to the RCVR FIFO under these circumstances. This bit is reset when the PC reads the Line Status Register.

Bit 0 Data Ready
This bit is set to 1 when received data is available, either in the RCVR FIFO (16550 mode) or Receive Buffer Register (16450 mode). This bit is set immediately upon the MPU writing data to the Receive Buffer or FIFO if the Receive Timer is not enabled but is delayed by the timer interval if the Receive Timer is enabled. For MPU read access a shadow bit exists so that the MPU does not see the delay the PC does. Both bits are cleared to logic zero immediately upon reading all the data in either the Receive Buffer or FIFO.

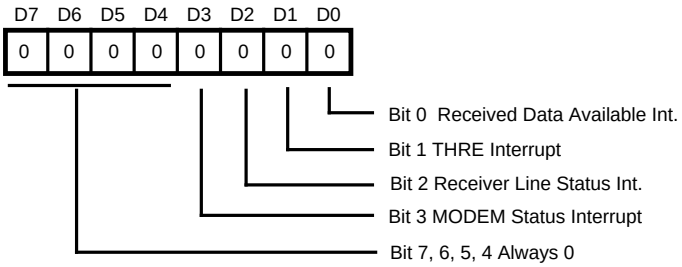


Figure 75. Interrupt Enable Register
(PC Read/Write, Address 01H)
(Z180 MPU Read Only, Address xxF1H)

Interrupt Enable Register

Bits 7, 6, 5, 4 Reserved
These bits will always read 0 (PC and MPU).

Bit 3 Modem Status IRQ
If bits 0, 1, 2 or 3 of the Modem Status Register are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 2 Receive Line Status IRQ
If bits 1, 2, 3 or 4 of the LSR are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 1 Transmit Holding Register Empty IRQ
If bit 5 of the LSR is set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 0 Received Data Available IRQ
If bit 0 of the LSR is set or a Receive Timeout occurs and this enable bit is a logic 1, then an interrupt to the PC is generated.

EMULATION MODES (Continued)

Table 21. Emulation Mode 1

Signal	Normal Mode 0	Emulation Adaptor Mode 1
PHI	Output	Input
/M1	Output	Input
/MREQ,/MRD	Output	Input
/IORQ	Output	Input
/RD	Output	Input
/WR	Output	Input
/RFSH	Output	Input
/HALT	Output	Input
ST	Output	Input
E	Output	Tri-state
/BUSACK	Output	Input
/WAIT	Input	Output
A19,A18/T_{OUT}	Output	Input
A17-A0	Output	Input
D7-D0	Input/Output	Input/Output
TxA0	Output	Tri-state
/RTS0	Output	Tri-state
TxA1	Output	Tri-state
/INT0	Input	Output, Open-Drain

Mode 2 Emulation Probe Mode
In the Emulator Probe Mode all of the Z182 output signals are tri-state. This scheme allows a Z182 emulator probe to grab on to the Z182 package leads on the target system.

Mode 3 RESERVED (for test purposes only)
This mode is reserved for test purpose only, do not use.

Notes:
Z182 has two branches of reset. /RESET controls the Z182 overall configuration, RAM and ROM boundaries, plus the ESCC, Port and the 16550 MIMIC interface. In Normal Mode, a "one shot" circuit samples the input of the /RESET pin to assert the internal reset to its proper duration. In Adapter Mode, this "one shot" circuit is bypassed. Note also that the Z180's crystal oscillator is disabled in Mode 1 and Mode 2.

In Mode 1 the emulator must provide /MREQ on the (/MREQ,/MRD) Z80182/Z8L182 pin (not /MRD); and A18 (not T_{OUT}) on the A18/T_{OUT} pin.

SLEEP, HALT EFFECT ON MIMIC AND 182 SIGNALS

The following Z80182/Z8L182 signals are driven High when Z180™ MPU enters a SLEEP or HALT state:

- /MRD when selected in the Interrupt Edge/Pin MUX Register.
- /MWR when selected in the Interrupt Edge/Pin MUX Register.
- /ROMCS,/RAMCS always High in SLEEP or HALT.

The following signals are High-Z during SLEEP and HALT:

- /IOCS when so selected in the Interrupt Edge/Pin MUX Register.
- /RD and /WR.

A0-A19 (A18 if selected) always High-Z in power down.

D0-D7 always High-Z in power down modes.

The MIMIC logic of the 182 is disabled during power down modes of the Z180.

TIMING DIAGRAMS

Z180 MPU Timing

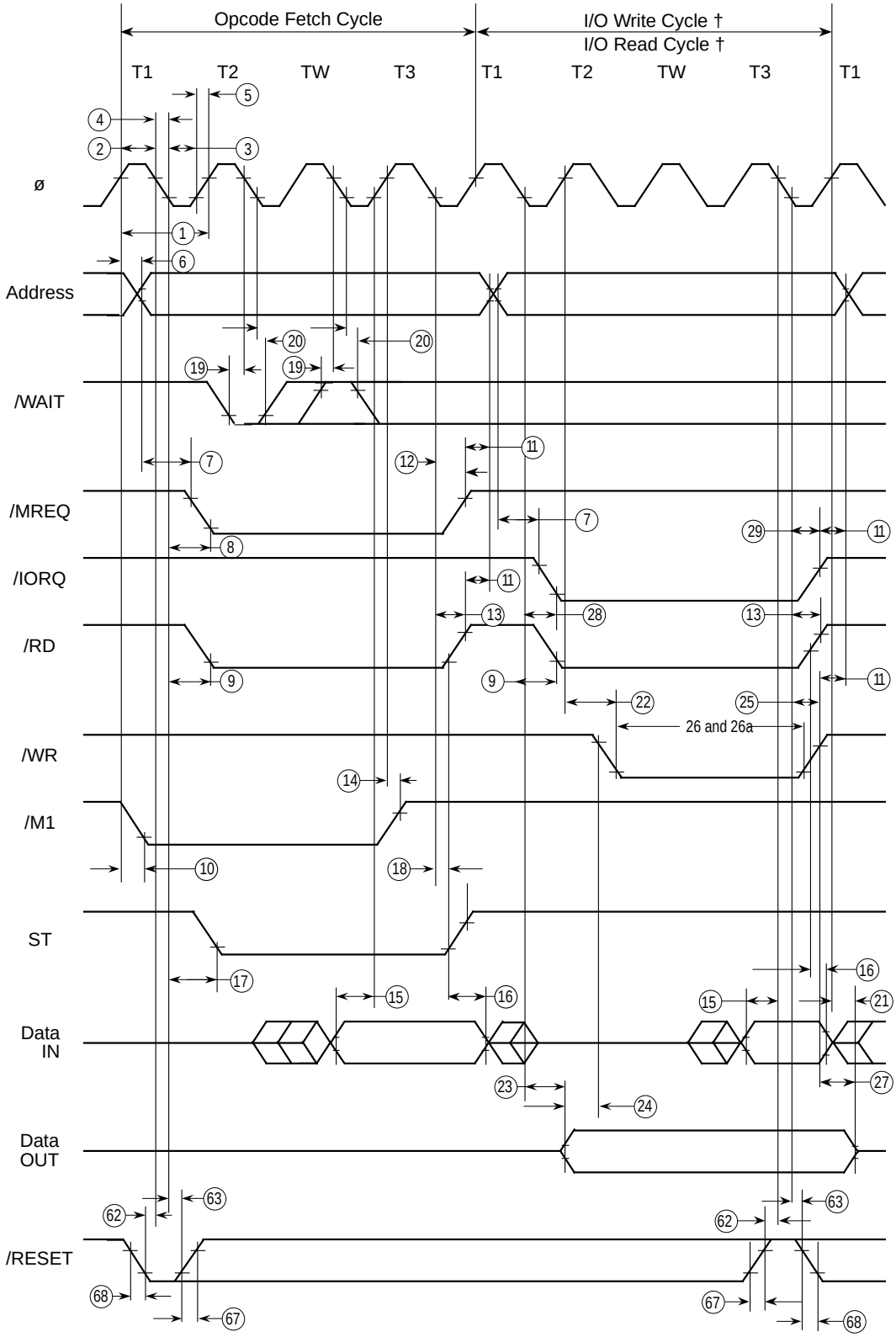


Figure 90. CPU Timing
(Opcode Fetch Cycle, Memory Read/Write Cycle
I/O Read/Write Cycle)

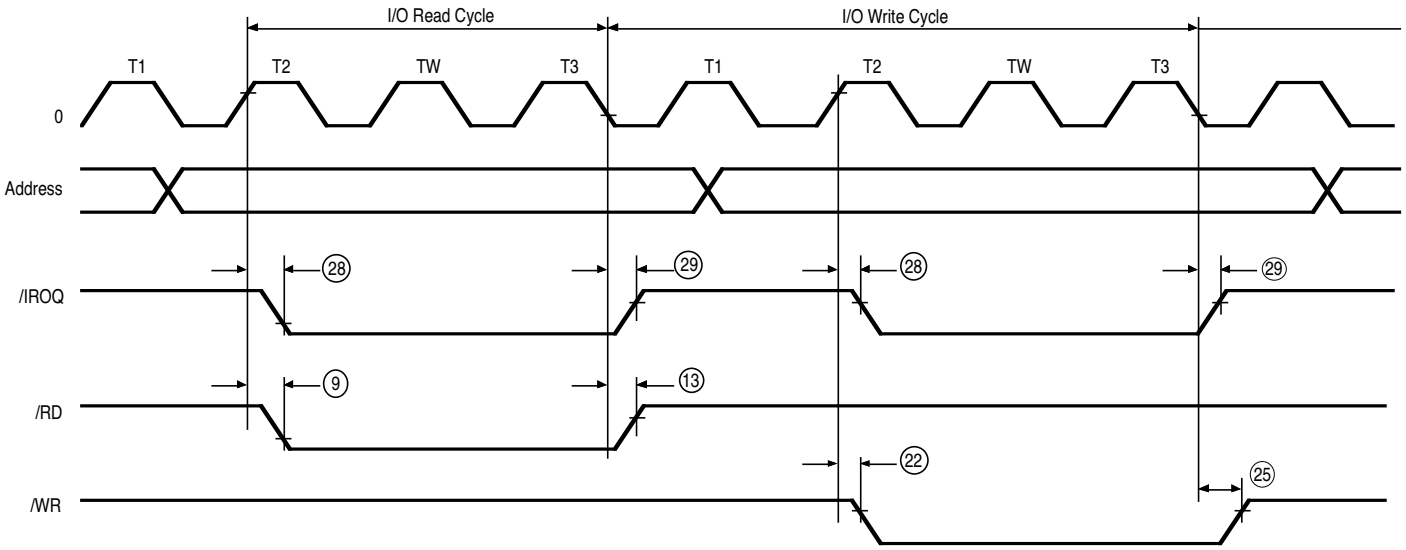
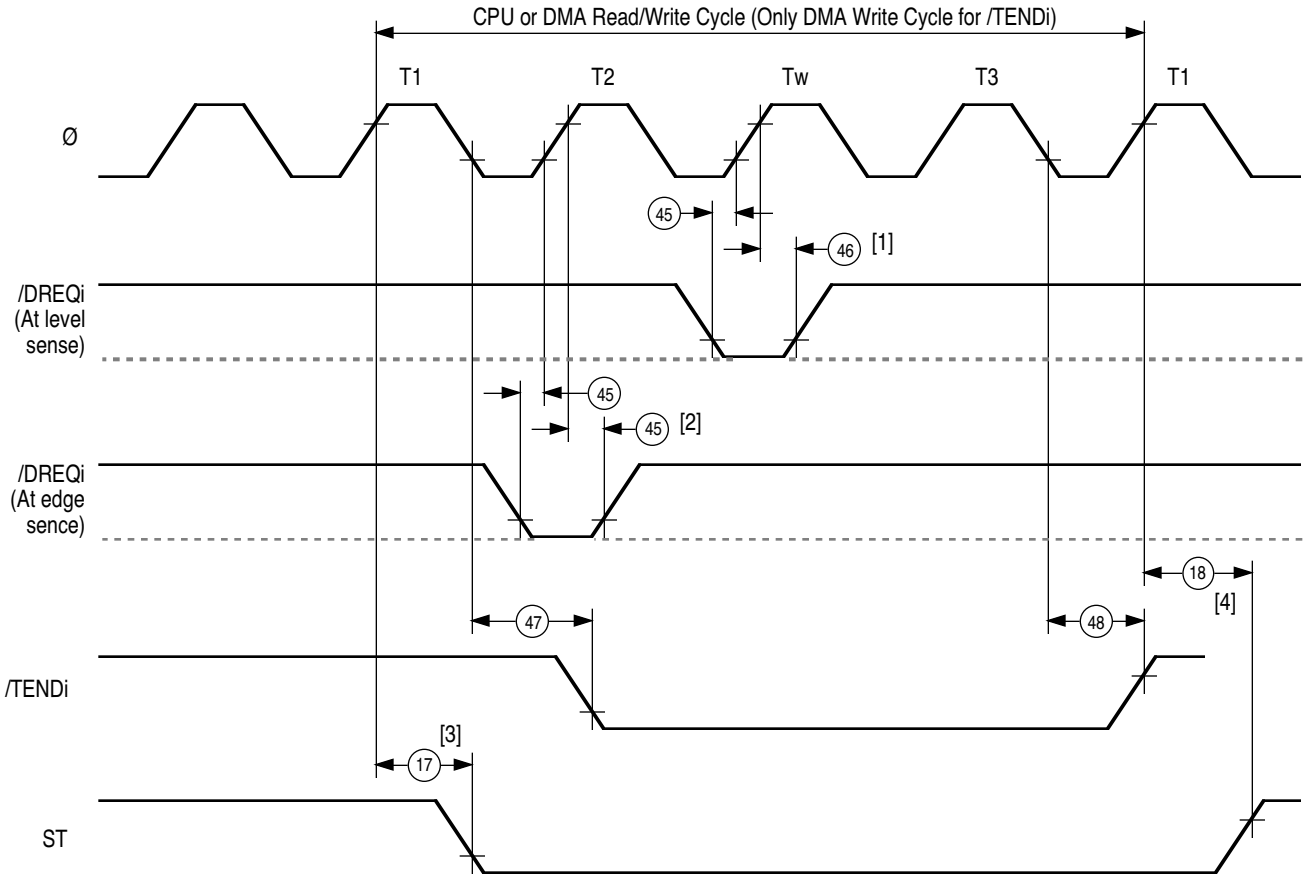


Figure 92. CPU Timing



DMA Control Signals
[1] tDRQS and tDRQH are specified for the rising edge of clock followed by T3.
[2] tDRQS and tDRQH are specified for the rising edge of clock.
[3] DMA cycle starts.
[4] CPU cycle starts.

Figure 93. DMA Control Signals

Z8S180 AC CHARACTERISTICS

Table A. Z8L180 and Z8S180 Timings

No.	Sym	Parameter	Z8L180 20 MHz Min	Z8L180 20 MHz Max	Z8S180 33 MHz Min	Z8S180 33 MHz Max	Unit	Note
1	tcyc	Clock Cycle Time	50	2000	30	2000	ns	[1]
2	tCHW	Clock Pulse Width (High)	15		10		ns	[1]
3	tCLW	Clock Pulse Width (Low)	15		10		ns	[1]
4	tcf	Clock Fall Time		10		5	ns	[1]
5	tcr	Clock Rise Time		10		5	ns	[1]
6	tAD	Address Valid from Clock Rise		15		15	ns	
7	tAS	Address Valid to /MREQ, /IORQ, /MRD Fall	5		5		ns	
8	tMED1	Clock Fall to /MREQ Fall Delay		15		10	ns	
9	tRDD1	Clock Fall to /RD, /MRD (/IOC=1)		25		15	ns	
		Clock Rise to /RD, /MRD Fall (/IOC=0)		35		15	ns	
10	tM1D1	Clock Rise to /M1 Fall delay		35		15	ns	
11	tAH	Address Hold time (/MREQ, /IORQ, /RD, /WR/MRD)	5		5		ns	
12	tMED2	Clock Fall to /MREQ Rise Delay		25		15	ns	
13	tRDD2	Clock Fall to /RD, /MRD Rise Delay		25		15	ns	
14	tM1D2	Clock Rise to /M1 Rise Delay		40		15	ns	
15	tDRS	Data Read Setup Time	15		15		ns	
16	tDRH	Data Read Hold Time	0		0		ns	
17	tSTD1	Clock Edge to ST Fall		30		15	ns	
18	tSTD2	Clock Edge to ST Rise		30		15	ns	
19	tWS	/WAIT Setup Time to Clock Fall	15		10		ns	[2]
20	tWH	/WAIT Hold Time from Clock Fall	10		5		ns	
21	tWDZ	Clock Rise to Data Float Delay		35		20	ns	
22	tWRD1	Clock Rise to /WR,/MWR Fall Delay		25		15	ns	
23	tWDD	Clock Fall to Write Data Delay		25		15	ns	
24	tWDS	Write Data Setup Time to /WR,/MWR Fall	10		10		ns	
25	tWRD2	Clock Fall to /WR Rise		25		15	ns	
26	tWRP	/WR Pulse Width (Memory Write Cycles)	75		45		ns	
26a		/WR Pulse Width (I/O Write Cycles)	130		70		ns	
27	tWDH	Write Data Hold Time from /WR Rise	10		5		ns	
28	tIOD1	Clock Fall to /IORQ Fall Delay (/IOC=1)		25		15	ns	
		Clock Rise to /IORQ Fall Delay (/IOC=0)		25		15	ns	
29	tIOD2	Clock Fall /IOQR Rise Delay		25		15	ns	
30	tIOD3	/M1 Fall to /IORQ Fall Delay	100		80		ns	
31	tINTS	/INT Setup Time to Clock Fall	20		15		ns	
32	tINTH	/INT Hold Time from Clock Fall	10		10		ns	
33	tNMIW	/NMI Pulse Width	35		25		ns	
34	tBRS	/BUSREQ Setup Time to Clock Fall	10		10		ns	
35	tBRH	/BUSREQ Hold Time from Clock Fall	10		10		ns	
36	tBAD1	Clock Rise to /BUSACK Fall Delay		25		15	ns	
37	tBAD2	Clock Fall to /BUSACK Rise Delay		25		15	ns	
38	tBZD	Clock Rise to Bus Floating Delay Time		40		30	ns	
39	tMEWH	/MREQ Pulse Width (High)	35		25		ns	
40	tMEWL	/MREQ Pulse Width (Low)	35		25		ns	

ESCC Timing

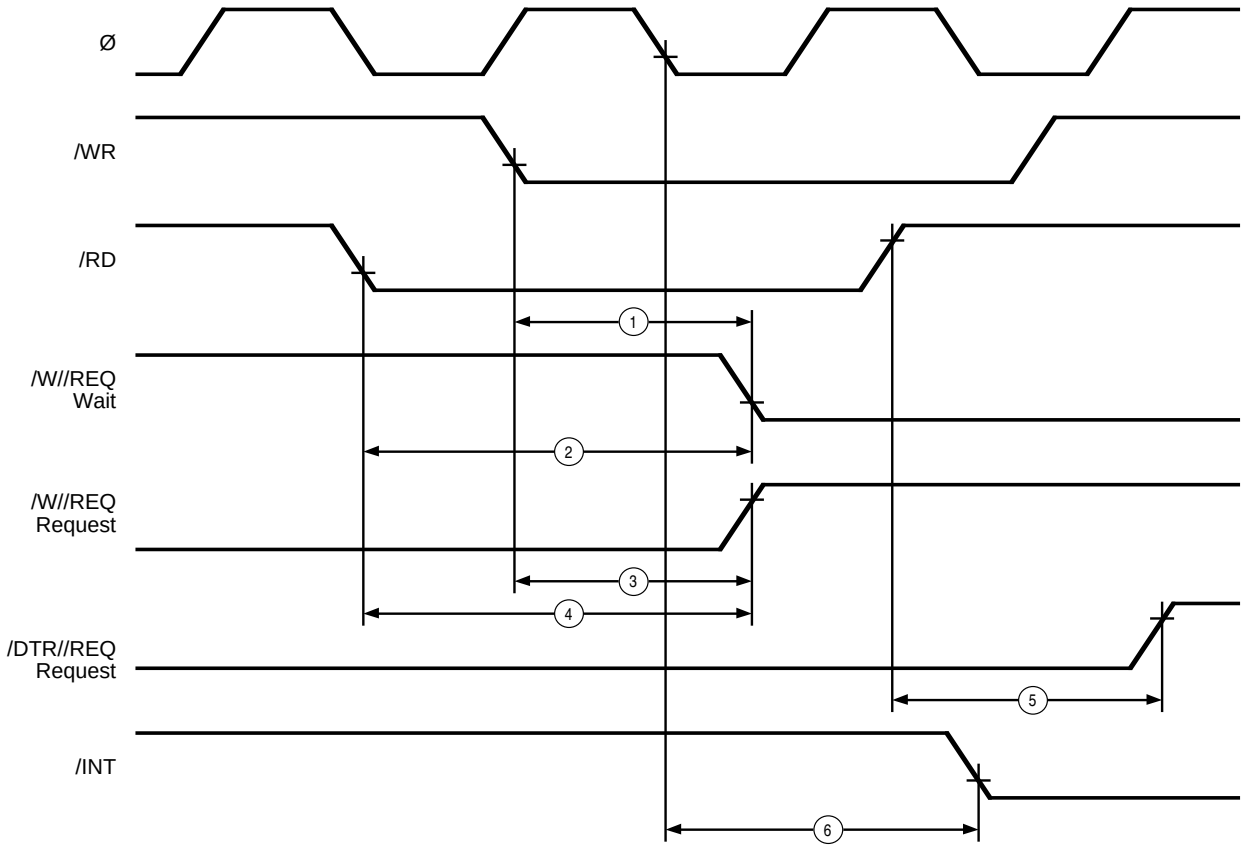


Figure 104. ESCC AC Parameter

Table B. ESCC Timing Parameters

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Unit
1	TdWR(W)	/WR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50	
3	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		65	
4	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		65	
5	TdRdr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay		TBD	
6	TdPC(INT)	Clock to /INT Valid Delay		160	

Table L. Interrupt Timing Transmitter FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
16	tHR	Delay from /WR (WR THR) to Reset Interrupt		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles
17	TSTI	Delay from Stop to Interrupt (THRE)	2 MPU Clock Cycles		2 MPU Clock Cycles	
18	TIR	Delay from /RD (RD IIR) to Reset Interrupt (THRIE)		75		75

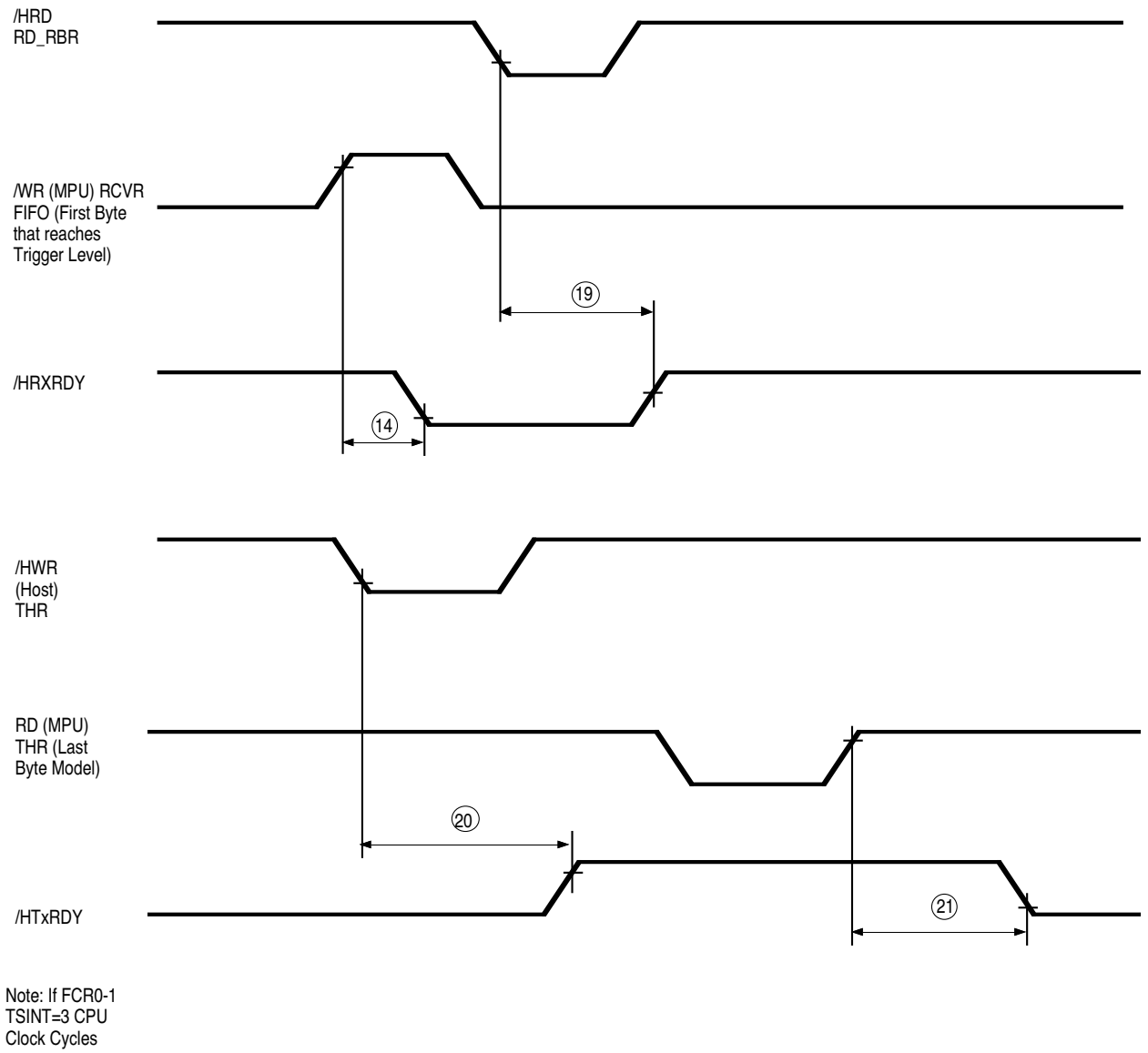


Figure 116 RCVR FIFO Bytes Other Than First