Zilog - Z8018233FSC1838 Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018233fsc1838

/W//REQB. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

16550 MIMIC INTERFACE SIGNALS

HD7-HD0. *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

/HDDIS. *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

HA2-HA0. *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

/HCS. *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

/HWR. *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

/HRD. *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

HINTR. *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

/HTxRDY. *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

/HRxRDY. *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

PARALLEL PORTS

PA7-PA0. *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

PC7-PC0. *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100% software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

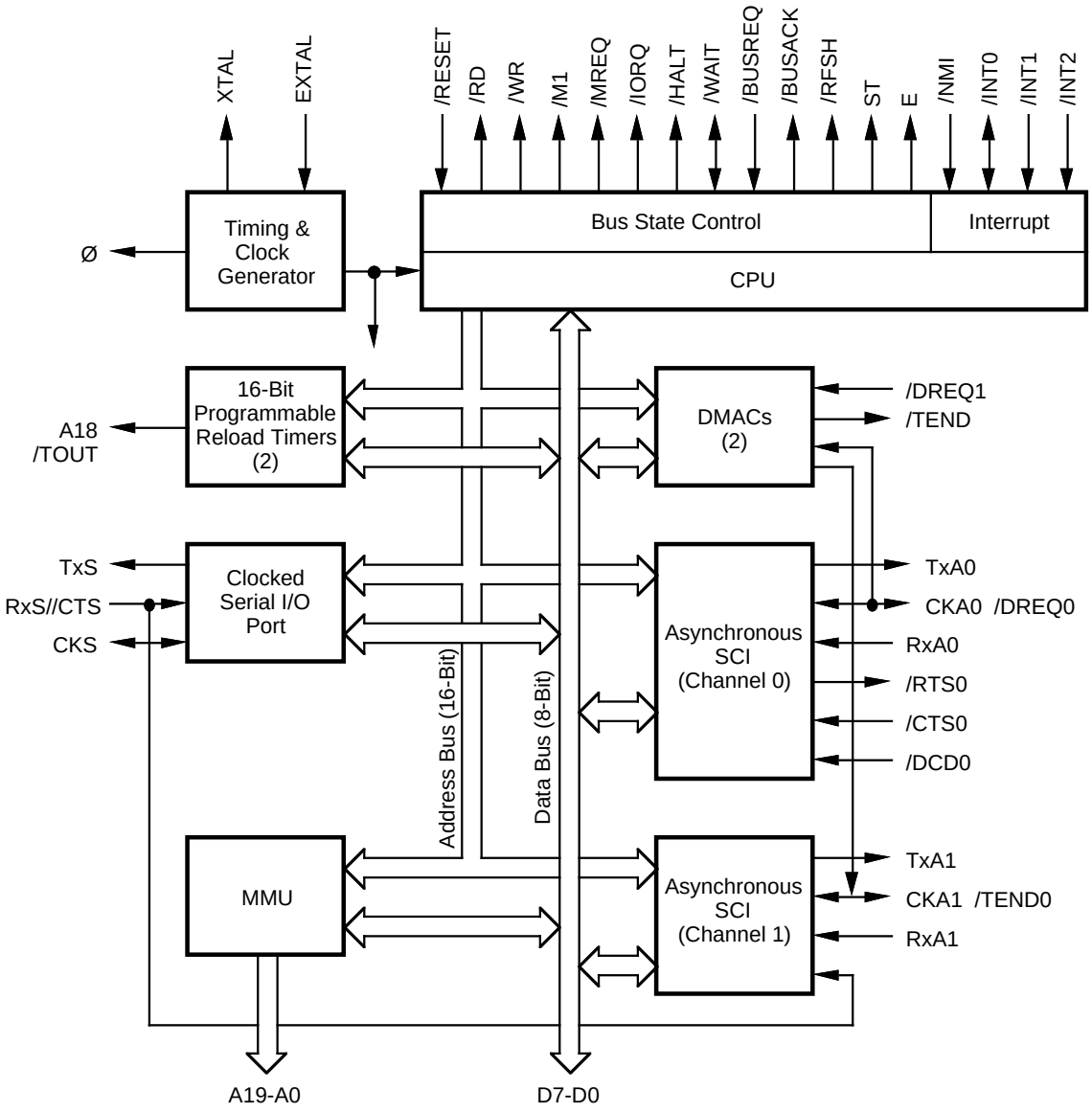


Figure 4. S180 MPU Block Diagram of Z182

Z80182 MIMIC DOUBLE BUFFERING FOR THE TRANSMITTER

The Z80182 Rev DA implements double buffering for the transmitter in 16450 mode and sets the TEMT bit in the LSR Register automatically.

When this feature is enabled and character delay emulation is being used (see Figure 9):

1. The PC THRE bit in the LSR Register is set when the THR Register is empty;
2. PC Host writes to the 16450 THR Register;
3. Whenever the Z80182 TSR buffer is empty and one character delay timer is in a timed-out state, the byte from the THR Register is transferred to the TSR buffer; the timer is in timed-out state after FIFO Reset or after Host TEMT is set. This allows a dual write to THR when Host TEMT is set.
4. Restart character delay timer (timer reloads and counts down) with byte transfer from THR Register to the TSR buffer;
5. Whenever the TSR buffer is full, the TEMT bit in MPU LSR Register is reset with no delay;
6. MPU reads TSR buffer;
7. TEMT bit in LSR Register for MPU is set with no delay whenever the TSR buffer is empty;
8. When the TSR buffer is read by MPU and THR Register is empty and one character delay timer reaches zero, the TEMT bit in the LSR Register for Host is set from 0 to 1.

The PC THRE bit in the LSR Register is reset whenever the THR Register is full and set whenever THR Register is empty.

MPU IREQ and DMA Request for the transmit data is trigger whenever TSR buffer is full and cleared whenever TSR buffer is empty.

If character delay emulation is not used the TEMT bit in the LSR Register is set whenever both the THR Register and the TSR buffer are both empty. The Host TEMT bit is clear if there is data in either the TSR buffer of THR Register.

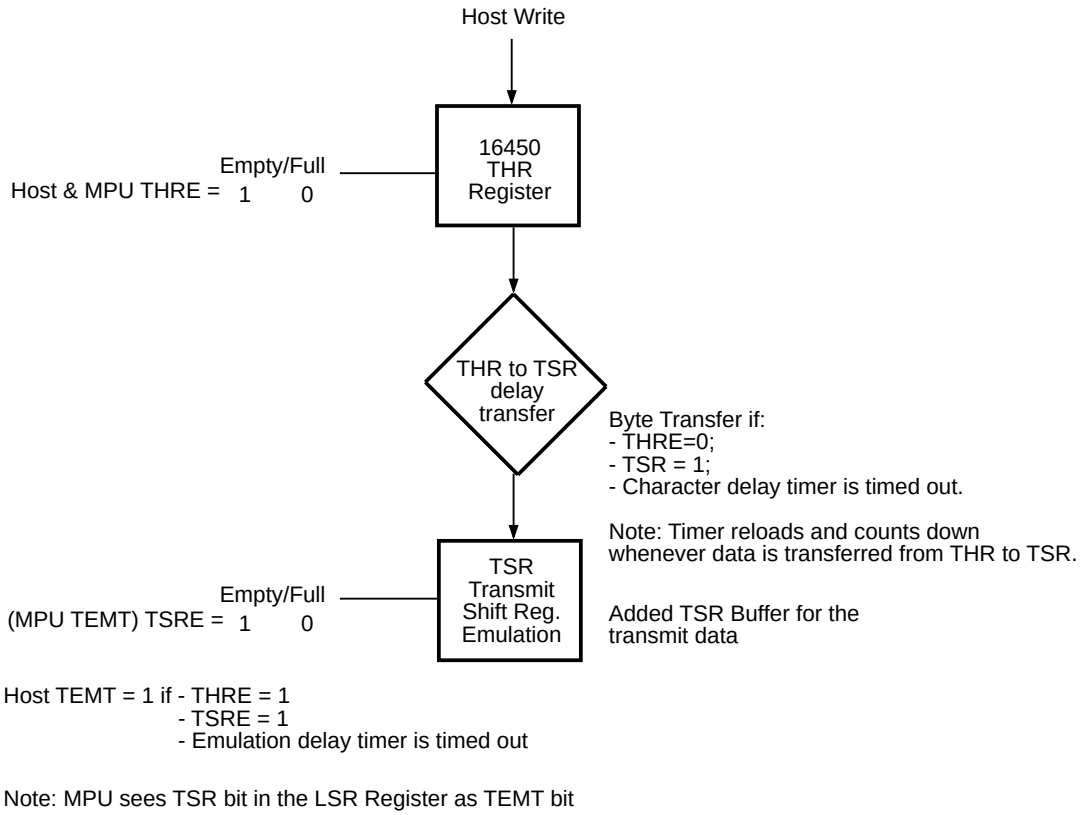
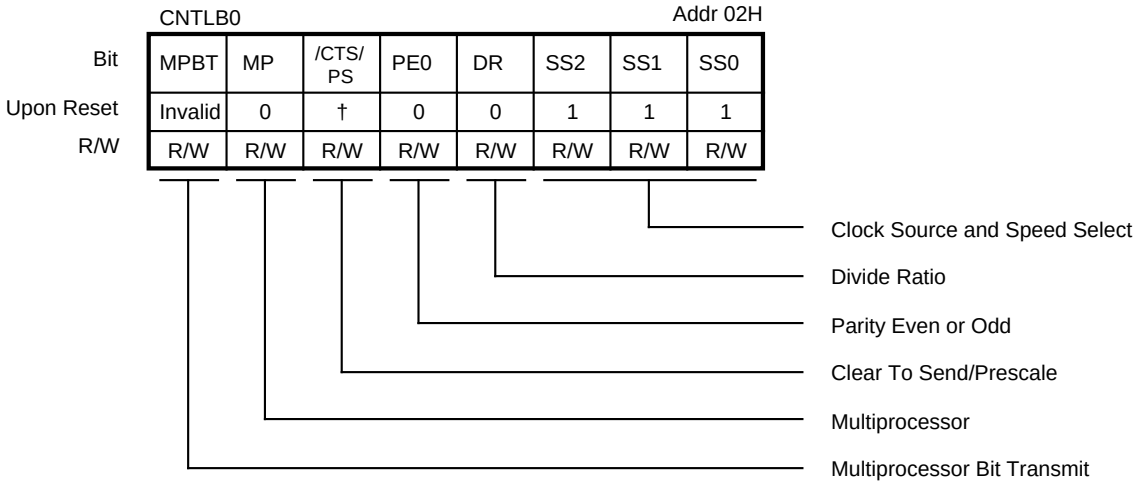


Figure 9. TEMT Emulation Logic Implementation



† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

General Divide Ratio	PS = 0 (Divide Ratio = 10)		PS = 1 (Divide Ratio = 30)	
SS, 2, 1, 0	**DR = 0 (x16)**	**DR = 1 (x64)**	**DR = 0 (x16)**	**DR = 1 (x64)**
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

Figure 11. ASCI Control Register B (Ch. 0)

TIMER DATA REGISTERS

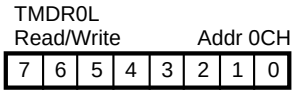


Figure 23. Timer 0 Data Register L

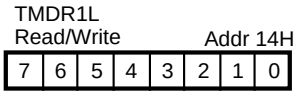
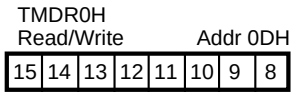
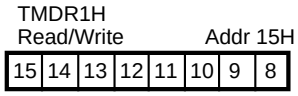


Figure 24. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 25. Timer 0 Data Register H



When Read, read Data Register L before reading Data Register H.

Figure 26. Timer 1 Data Register H

TIMER RELOAD REGISTERS

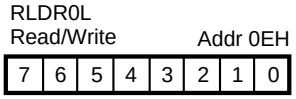


Figure 27. Timer 0 Reload Register L

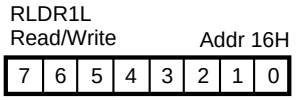


Figure 28. Timer 1 Reload Register L

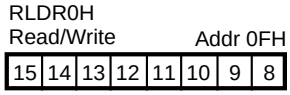


Figure 29. Timer 0 Reload Register H

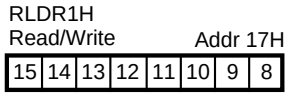


Figure 30. Timer 1 Reload Register H

FREE RUNNING COUNTER

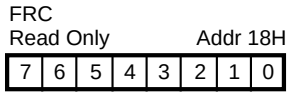


Figure 32. Free Running Counter

CPU CONTROL REGISTER

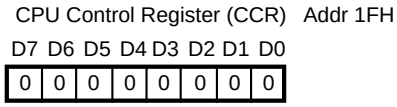
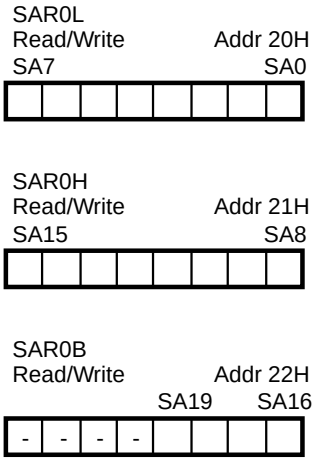


Figure 33. CPU

Note: See Figure 49 for full description.

DMA REGISTERS



Bits 0-2 (3) are used for SAR0B

A19,	A18,	A17,	A16	DMA Transfer Request
x	x	0	0	/DREQ0 (external)
x	x	0	1	RDR0 (ASCI0)
x	x	1	0	RDR1 (ASCI1)
x	x	1	1	Not Used

Figure 34. DMA 0 Source Address Registers

SYSTEM CONTROL REGISTERS

IL — Addr 33H

Bit	IL7	IL6	IL5	-	-	-	-	-
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W					

Interrupt Vector Low

Figure 46. Interrupt Vector Low Register

ITC — Addr 34H

Bit	TRAP	UFO	-	-	-	ITE2	ITE1	ITE0
Upon Reset	0	0	1	1	1	0	0	1
R/W	R/W	R				R/W	R/W	R/W

/INT Enable 2, 1, 0
Undefined Fetch Object
TRAP

Figure 47. INT/TRAP Control Register

RCR — Addr 36H

Bit	REFE	REFW	-	-	-	-	CYC1	CYC0
Upon Reset	1	1	1	1	1	1	0	0
R/W	R/W	R/W					R/W	R/W

Cycle Select
Refresh Wait State
Refresh Enable

CYC1, 0	Interval of Refresh Cycle
00	10 states
01	20 states
10	40 states
11	80 states

Figure 48. Refresh Control Register

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is stopped completely. IDLE mode is exited in a similar way as STANDBY mode, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS, except that the 2^{17} bit wake-up timer is bypassed; all control signals are asserted eight clock cycles after the exit conditions are gathered.

STANDBY-QUICK RECOVERY Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from 2^{17} clock cycles (6.5 ms at 20 MHz) to 2^{6} clock cycles (3.2 µs at 20 MHz). This feature can only be used when providing an oscillator as clock source.

To enter STANDBY-QUICK RECOVERY mode:

1. Set D6 and D3 to 1 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS; the clock and other control signals are recovered sooner than the STANDBY mode.

Note: If STANDBY-QUICK RECOVERY is enabled, the user must make sure stable oscillation is obtained within 64 clock cycles.

CPU Control Register

The Z8S180 has an additional register which allows the programmer to select options that directly affect the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU Control Register (CCR) allows the programmer to change the divide-by-two internal clock to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 can reduce the output drivers on selected groups of pins to 25% of normal pad driver capability which minimizes the EMI noise generated by the part.

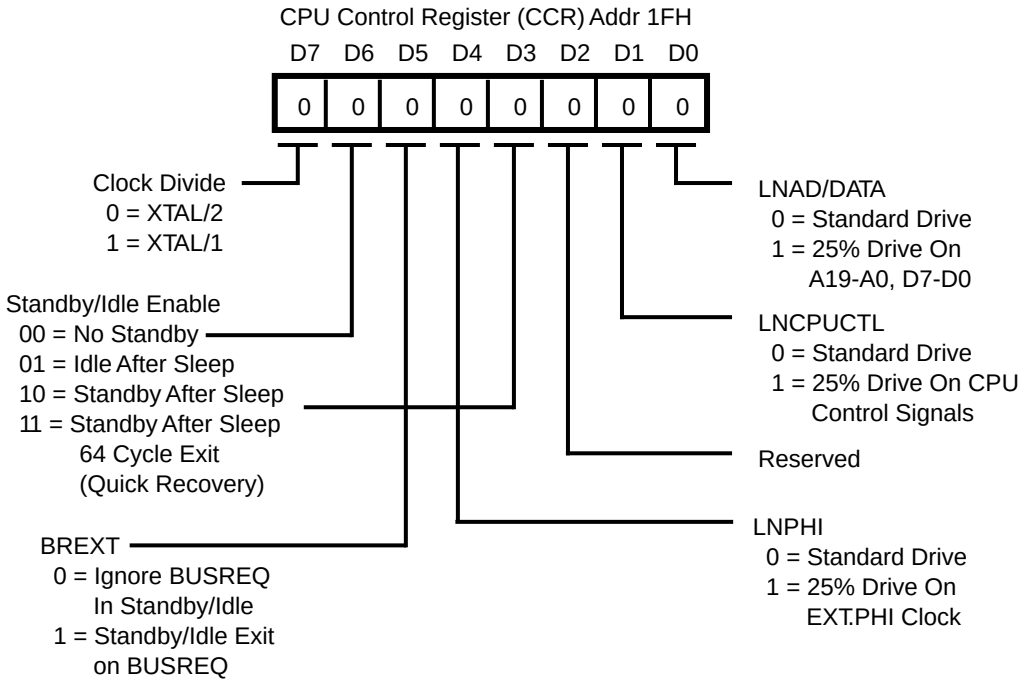


Figure 51. CPU Control Register

PROGRAMMING THE ESCC™

The ESCC contains write registers in each channel that are programmed by the system separately to configure the functional uniqueness of the channels.

In the ESCC, the data registers are directly addressed by selecting a High on the D//C pin. With all other registers (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers, both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected read register accessed. All of the ESCC registers, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

With the Z80182/Z8L182, a new feature is implemented in the ESCC. The Transmitter and Receiver is now capable of sending and comparing a 32-bit CRC-32 (Ethernet Polynomial):

$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

This feature is enabled by access to WR7' Bit 7, which selects the 32-bit CRC polynomial for the transmitter and receiver and overrides any selection of SDLC/CRC-16 CRCs. When the 32-bit CRC override feature is enabled, the transmitter will only send 32-bit CRC when CRC is to be sent. On the receive side, the CRC comparison/calculation will be done only on 32-bit CRC values. The result of the 32-bit CRC comparison will be maintained in RR1 bit D6 in place of the 16-bit CRC comparison result. The 32-bit CRC compare result will also be maintained in the 10x19 FIFO for frames in which 32-bit CRC is enabled. The CRC still can be preset to all 0s or all 1s. 32-bit CRC is disabled upon power-up or reset.

Note: The ESCC cannot do simultaneous calculation/ comparison using both 16-bit and 32-bit CRC.

Also, for the Z80182/Z8L182 only, the clock provided to the ESCC core is equal to the system clock divided by 1 or 2. The divider is programmed in the Z80182 Enhancement Register bit 3.

Divide-by-two should be programmed when running the Z182 beyond:

- 20 MHz, 5V
- 10 MHz, 3V

Note: Upon power-up or reset the system clock is equal to the ESCC clock.

Initialization. The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, in the Asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity should be set first. Then the interrupt mode is set, and finally, the receiver and transmitter are enabled.

Write Registers. The ESCC contains 16 write registers (17 counting the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. There are two registers (WR2 and WR9) shared by the two channels that are accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits and reset commands. A new register, WR7', was added to the ESCC and may be written to if WR15, D0 is set. Figure 50 shows the format of each write register.

Read Registers. The ESCC contains ten read registers (eleven, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) are read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (channel A) or the vector modified by status information (channel B). RR3 contains the Interrupt Pending (IP) bits (channel A only). RR6 and RR7 contain the information in the SDLC Frame Status FIFO, but is only read when WR15, D2 is set. If WR7' D6 is set, Write Registers WR3, WR4, WR5, WR7, and WR10 can be read as RR9, RR4, RR5, and RR14, respectively. Figure 51 shows the format of each Read register.

CONTROL REGISTERS (Continued)

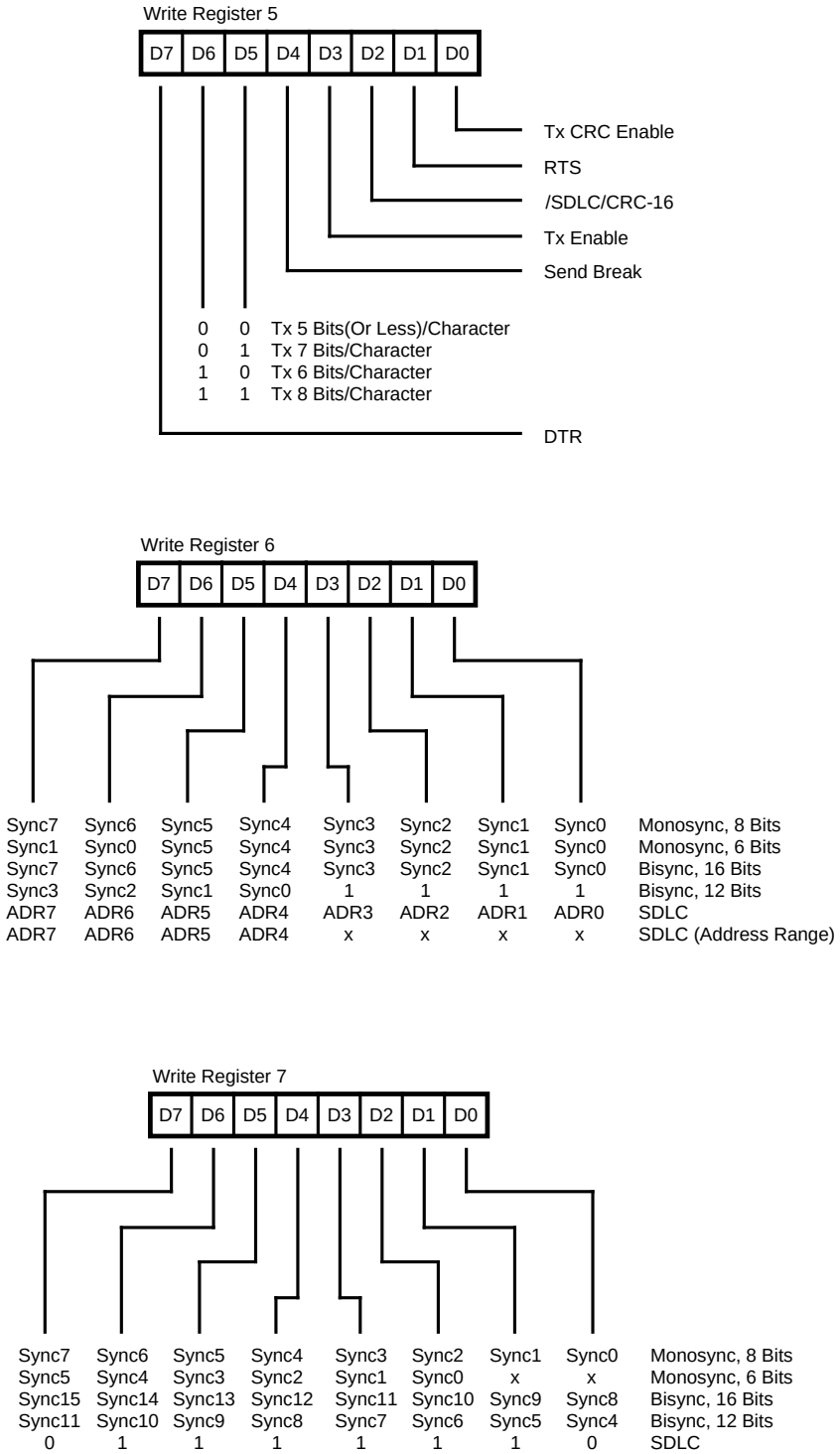


Figure 52. Write Register Bit Functions (Continued)

16550 MIMIC REGISTERS (Continued)

FIFO Control Register

Bit 6 and Bit 7 RCVR trigger LSB and MSB bits
This 2-bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs (see Table 18).

Bit 4 and Bit 5
Reserved for future use (PC side). Note: From the MPU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side will clear a previously set bit 4 or bit 5.

Bit 3 DMA mode select
Setting this bit to 1 will cause the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A 1 in this bit enables multi-byte DMA).

Bit 2 XMIT FIFO Reset
Setting this bit to 1 will cause the transmitter FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 1 RCVR FIFO Reset
Setting this bit to 1 will cause the receiver FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 0 FIFO Enable
The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be 1 when writing to the other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared. This feature can be forced in a disabled state by the MPU.

Table 18. Receive Trigger Level

b7	b6	Trigger Level, Number of Bytes
0	0	1
0	1	4
1	0	8
1	1	14

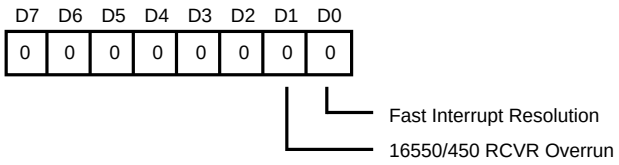


Figure 72. MIMIC Modification Register
(Z180 MPU Write only, Address xxE9h)

Bit 7-2 Reserved. Program to zero.

Bit 1 RCVR Overrun Modification
The actual 16450/16550 device allows the last position in FIFO to be overwritten by DCE during receiver overrun condition. When this bit is enabled (programmed to 1) the last position in FIFO can be overwritten by Z180 during receiver overrun. This feature is disabled by default. When this modification is not enabled, the MIMIC will ignore any write to RBR during an overrun condition.

Bit 0 Fast MIMIC-ESCC Interrupt Resolution
When enabling this modification, the internal MIMIC IEO signal into the ESCC IEI input is forced Low when the MIMIC Interrupt line becomes active. This is required to prevent the ESCC from putting it's vector on the databus during an INTACK cycle (given that the MIMIC is programmed to have higher interrupt priority).

When disabled, the internal MIMIC IEO becomes deasserted only after an interrupt acknowledge cycle. In this case, it is possible for the ESCC to force it's interrupt vector onto the data bus even when the MIMIC has a pending interrupt and is higher in priority.

16550 MIMIC REGISTERS (Continued)

Line Status Register

Bit 7 Error in RCVR FIFO
In 16450 mode, this bit will read logic 0. In 16550 mode this bit is set if at least one data byte is available in the FIFO with one of its associated error bits set. This bit will clear when there are no more errors (or break detects) in the FIFO.

Bit 6 Transmitter Empty
This bit must be set or reset by the MPU by a write to this register bit. If Double Buffer Mode is enabled, the TEMT bit is set/reset automatically. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 5 Transmit Holding Register Empty, THRE
This bit is set to 1 when either the THR has been read (emptied) by the MPU (16450 mode) or the XMIT FIFO is empty (16550 mode). This bit is set to 0 when either the THR or XMIT FIFO become non-empty. A shadow bit exists so that the register bit setting to 1 is delayed by the Transmitter Timer if enabled. The MPU when reading this bit will not see the delay. Both shadow and register bits are cleared when the PC writes to the THR of XMIT FIFO. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 2, 3, 4 Parity Error, Framing Error, Break Detect
These bits are written, indirectly, by the MPU as follows: The bits are first written to shadow bit locations when the MPU write accesses the LSR. When the next character is written to the Receive Buffer or RCVR FIFO, the data in the shadow bits is then copied to the LSR (16450 mode) or FIFO RAM (16550 mode). In FIFO mode bits become available to the PC when the data byte associated with the bits is next to be read (top of FIFO). In FIFO mode, with successive reads of the receiver, the status bits will be set if an error occurs on any byte. Once the MPU writes to the Receive Buffer or RCVR FIFO, the shadow bits are auto cleared. The register bits are cleared upon the PC reading the LSR. In FIFO mode these bits will be set if any byte has the respective error bit set while the PC reads multiple characters from the FIFO.

Bit 1 Overrun Error
This bit is set if the Z180 MPU makes a second write to the Receive Buffer before the PC reads the data in the Buffer (16450 mode) or with a full RCVR FIFO (16550 mode.) No data will be transferred to the RCVR FIFO under these circumstances. This bit is reset when the PC reads the Line Status Register.

Bit 0 Data Ready
This bit is set to 1 when received data is available, either in the RCVR FIFO (16550 mode) or Receive Buffer Register (16450 mode). This bit is set immediately upon the MPU writing data to the Receive Buffer or FIFO if the Receive Timer is not enabled but is delayed by the timer interval if the Receive Timer is enabled. For MPU read access a shadow bit exists so that the MPU does not see the delay the PC does. Both bits are cleared to logic zero immediately upon reading all the data in either the Receive Buffer or FIFO.

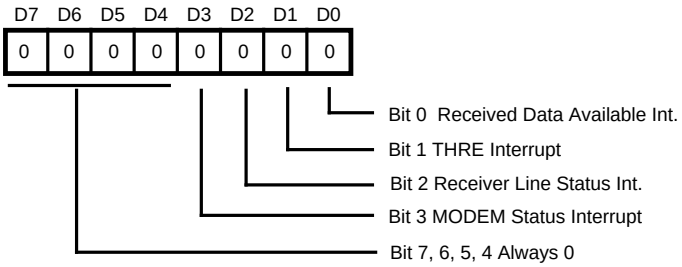


Figure 75. Interrupt Enable Register
(PC Read/Write, Address 01H)
(Z180 MPU Read Only, Address xxF1H)

Interrupt Enable Register

Bits 7, 6, 5, 4 Reserved
These bits will always read 0 (PC and MPU).

Bit 3 Modem Status IRQ
If bits 0, 1, 2 or 3 of the Modem Status Register are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 2 Receive Line Status IRQ
If bits 1, 2, 3 or 4 of the LSR are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 1 Transmit Holding Register Empty IRQ
If bit 5 of the LSR is set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 0 Received Data Available IRQ
If bit 0 of the LSR is set or a Receive Timeout occurs and this enable bit is a logic 1, then an interrupt to the PC is generated.

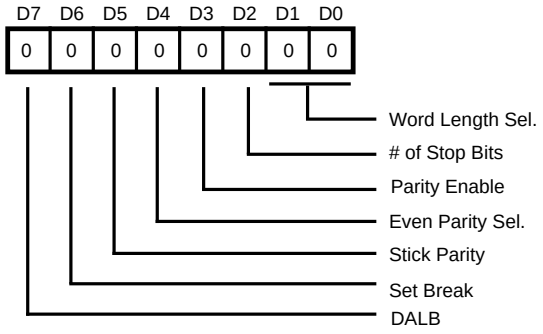


Figure 76. Line Control Register
(PC Read/Write, Address 03H)
(Z180 MPU Read Only, Address xxF3H)

Line Control Register

Bit 7 Divisor Latch Access Bit (DALB)
This bit allow access to the divisor latch by the PC/XT/AT. If this bit is set to 1, access to the Transmitter, Receiver and Interrupt Enable Registers is disabled. When an access is made to address 0 the Divisor Latch Least Significant byte is accessed. If an access is made to address 1, the Divisor Latch Most Significant byte is accessed.

Bit 6 - Bit 0
These bits do not affect the Z80182/Z8L182 directly, however they can be read by the Z180 MPU and the 16550 MIMIC modes can be emulated by the Z180 MPU.

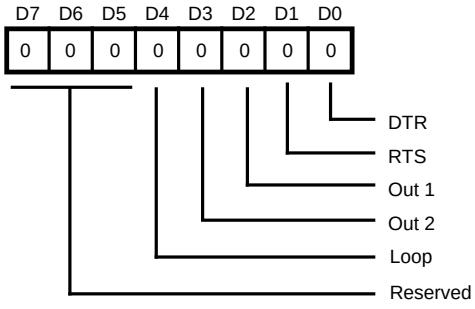


Figure 77. Modem Control Register
(PC Read/Write, Address 04H)
(Z180 MPU Read Only, Address xxF4H)

Modem Control Register

Bit 7-5 Reserved
Reserved for future use, always 0.

Bit 4 Loop
When this bit is set to 1, D3-D0 field reflects the status of Modem Status Register, as follows:

RI = Out 1
DCD = Out 2
DSR = DTR
CTS = RTS

Emulation of the 16550 UART loop back feature must be done by the Z180 MPU, except in the above conditions.

Bit 3 Out 2
This bit controls the tri-state on the HINTR pin if bits 2 and 1 are 10. Otherwise it can be read by the Z180 MPU.

Bits 2, 1, 0
These bits have no direct control of the 16550 MIMIC interface and the Z180 MPU must emulate the function if it is to be implemented.

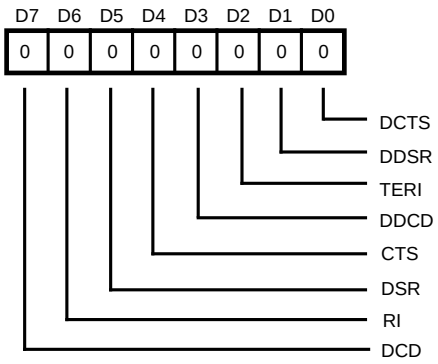


Figure 78. Modem Status Register
(PC Read Only, Address 06H)
(Z180 MPU Read/Write bits 7-4, Address xxF6H)

Z80182 ENHANCEMENTS REGISTER

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode
If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit is used to allow DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TxDA Tri-state
The TxDA pin can be tri-stated on assertion of the /HALT pin. This prevents the TxDA from driving and external device when /HALT output is used to force other devices into power-down modes. This feature is disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider
The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock will be Z180's PHI clock divided by two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5V or 10 MHz/3V, this bit should be set for ESCC divide-by-two mode.

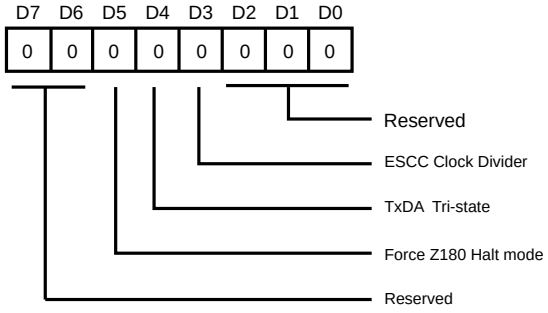


Figure 82. Z80182 Enhancements Register
(Z180 MPU Read/Write, Address xxD9H)

PARALLEL PORTS REGISTERS

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output. The Ports consist of two registers the Port Direction Control Register and the Port Data Register. The Port and direction register can be accessed in any page of I/O space since only the lowest eight address lines are decoded. Bits PC7 and PC6 are input only bits and have the special function of reading the external value of the /INT2 and /INT1 pins. Writing '1' to these bits will clear the edge detect interrupt logic when operating /INT2 and/or /INT1 in edge detect mode.

When Port B and Port C bits 5-0 are deselected in the System Configuration Register, the Data and Data Direction Registers are still available as read/write scratch registers. If a Port is deselected and if the DDR bit is a '0', then the written value to that bit will be latched and this value can be read back. If a Port is deselected and if the DDR bit is a '1', then you could read only the external pin value; any write to that bit is latched but can be read back only with DDR=0.

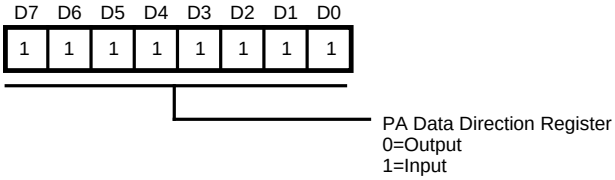


Figure 83. PA, Port A, Data Direction Register
(Z180 MPU Read/Write, Address xxEDH)

The data direction register determines which are inputs and outputs in the PA Data Register. When a bit is set to 1 the corresponding bit in the PA Data Register is an input. If the bit is 0, then the corresponding bit is an output.

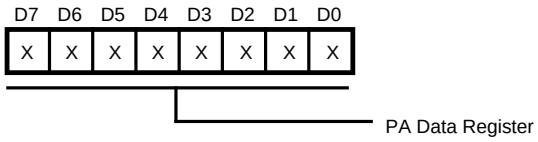


Figure 84. PA, Port A, Data Register
(Z180 MPU Read/Write, Address xxEEH)

When the Z180 MPU writes to the PA Data Register the data is stored in the internal buffer. The values of the PA Data Register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PA Data Register the data on the external pins is returned.

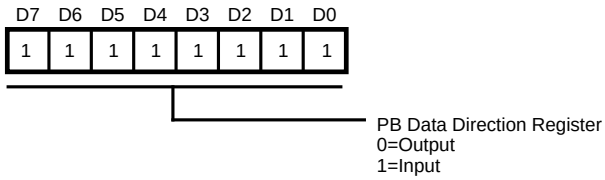


Figure 85. PB, Port B, Data Direction Register
(Z180 MPU Read/Write, Address xxE4H)

The data direction register determines which are inputs and outputs in the PB Data Register. When a bit is set to 1 the corresponding bit in the PB Data Register is an input. If the bit is 0 then the corresponding bit is an output.

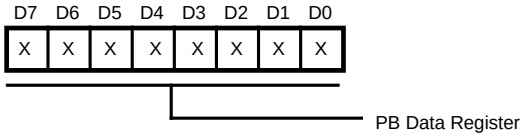


Figure 86. PB, Port B, Data Register
(Z180 MPU, Address xxE5H)

When the Z180 MPU writes to the PB Data Register the data is stored in the internal buffer. The values of Port B data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PB Data Register, the data on the external pins is returned.

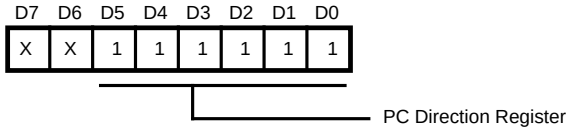


Figure 87. PC, Port C, Data Direction Register
(Z180 MPU Read/Write, Address xxDDH)

Z80182/Z8L182 MIMIC DMA CONSIDERATIONS

For the PC Interface, the 16550 device has two modes of operation that need to be supported by the MIMIC. In single transfer mode, the DMA request line for the receiver goes active whenever there is at least one character in the RCVR FIFO. For the transmitter, the DMA request line is active on an empty XMIT FIFO and inactive on non-empty.

In multi-transfer mode, the RCVR DMA goes active at the trigger level and inactive on RCVR FIFO empty. The XMIT DMA is active on non-full XMIT FIFO and inactive on a full XMIT FIFO.

Bit 3 in the FCR controls the DMA mode for the PC interface. If a 1 is programmed into this bit, multi-byte DMA is enabled. A 0 in this bit (default) enables single byte DMA.

As specified, the 16550 does not have any means of handling the error status bits in the FIFO in this multi-transfer mode. Such DMA transfers would require blocks with some checksum or other error checking scheme.

For the MPU interface, the DMA is controlled by a non-empty transmit FIFO and by a non-full receive FIFO conditions (THRE and the DR bits in the LSR). If the delay timers are enabled, the respective shadow bits are used for DMA control. The effect of the DMA logic is to request DMA service when at least one byte of data is available to be read or written to the FIFO's by the Z180. The Z180's DMA channel can be programmed to trigger on edge or on level.

EMULATION MODES

The Z80182/Z8L182 provides four modes of operation. The modes are selected by the EV1 and EV2 pins. These four modes allow the system development and commercial production to be done with the same device. The four emulation modes are shown in Table 20.

Table 20. EV2 and EV1, Emulation Mode Control

	EV2	EV1	EV Description
Mode 0	0	0	Normal Mode, on-chip Z180 bus master
Mode 1	0	1	Emulation Adapter Mode
Mode 2	1	0	Emulator Probe Mode
Mode 3	1	1	RESERVED, for Test Use Only

Mode 0 Normal Mode

This is the normal operating mode for the Z80182/Z8L182.

Mode 1 Emulation Adapter Mode

The Emulation Adaptor Mode enables system development for the Z182 with a readily available Z180 emulator. The Emulator provides the Z180™ MPU and Z180 peripheral functions to the target system, with their signals passing through the emulation adapter. In Emulation Adaptor Mode the Z182s, Z180 MPU and Z180 peripheral signals are tri-state or physically disconnected. The Z182 continues to provide its ESCC, MIMIC, chip select, and Port functions and signals to the target system. The Mode 1 effects on the Z182 are shown in Table 21. Note that INT1-2 Edge Detect Logic cannot be used in Emulation Adaptor EV Mode 2.

DC CHARACTERISTICS

Z80182/Z8L182

(V_{CC} = 5V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL, NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL, NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL, NMI	–0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL, NMI	–0.3		0.8	V	
V_{OH1}	Output H Voltage	2.4			V	I_{OH} = –200 µA
	All outputs	V_{CC} –1.2				I_{OH} = –200 µA
V_{OH2}	Output H PHI	V_{CC} –0.6			V	I_{OH}= –200 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.2 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{TL}	Tri-state Leakage Current			1.0	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{CC}*	Power Dissipation*		60	120	mA	f = 20 MHz
	(Normal Operation)		100	200	mA	f = 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(SLEEP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		TBD	TBD	mA	f= 20 MHz
	(I/O STOP)		TBD	TBD	mA	f= 33 MHz
	Power Dissipation*		5	10	mA	f = 20 MHz
	(SYSTEM STOP mode)		9	17	mA	f = 33 MHz
	IDLE Mode		TBD	TBD	mA	f = 20 MHz
			TBD	TBD	mA	f = 33 MHz
	STANDBY Mode		50		µA	f = 0 MHz †
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:

These I_{CC} values are preliminary and subject to change without notice.

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
V_{CC} = 5.0V; (I_{OH} Low EMI) = -50 µA, I_{OL} (Low EMI) = 500 µA

† Device may take up to two seconds before stabilizing to steady state standby current.

DC CHARACTERISTICS

Z80182/Z8L182

(V_{CC} = 3.3V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL, NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL, NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL, NMI	–0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL, NMI	–0.3		0.8	V	
V_{OH1}	Output H Voltage All outputs	2.15			V	I_{OH} = –200 µA
V_{OH2}	Output H PHI	V_{CC} –0.6			V	I_{OH}= –200 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.2 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			10	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{TL}	Tri-state Leakage Current			10	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{CC}*	Power Dissipation* (Normal Operation)		40	80	mA	f = 20 MHz
	Power Dissipation* (SLEEP)		TBD	TBD	mA	f= 20 MHz
	Power Dissipation* (I/O STOP)		TBD	TBD	mA	f= 20 MHz
	Power Dissipation* (SYSTEM STOP mode)		4	8	mA	f = 20 MHz
	IDLE Mode		TBD	TBD	mA	f = 20 MHz
	STANDBY Mode		50		µA	f = 0 MHz †
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:

These I_{CC} values are preliminary and subject to change without notice.

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
V_{CC} = 3.3V

† Device may take up to two seconds before stabilizing to steady state current.

ESCC Timing

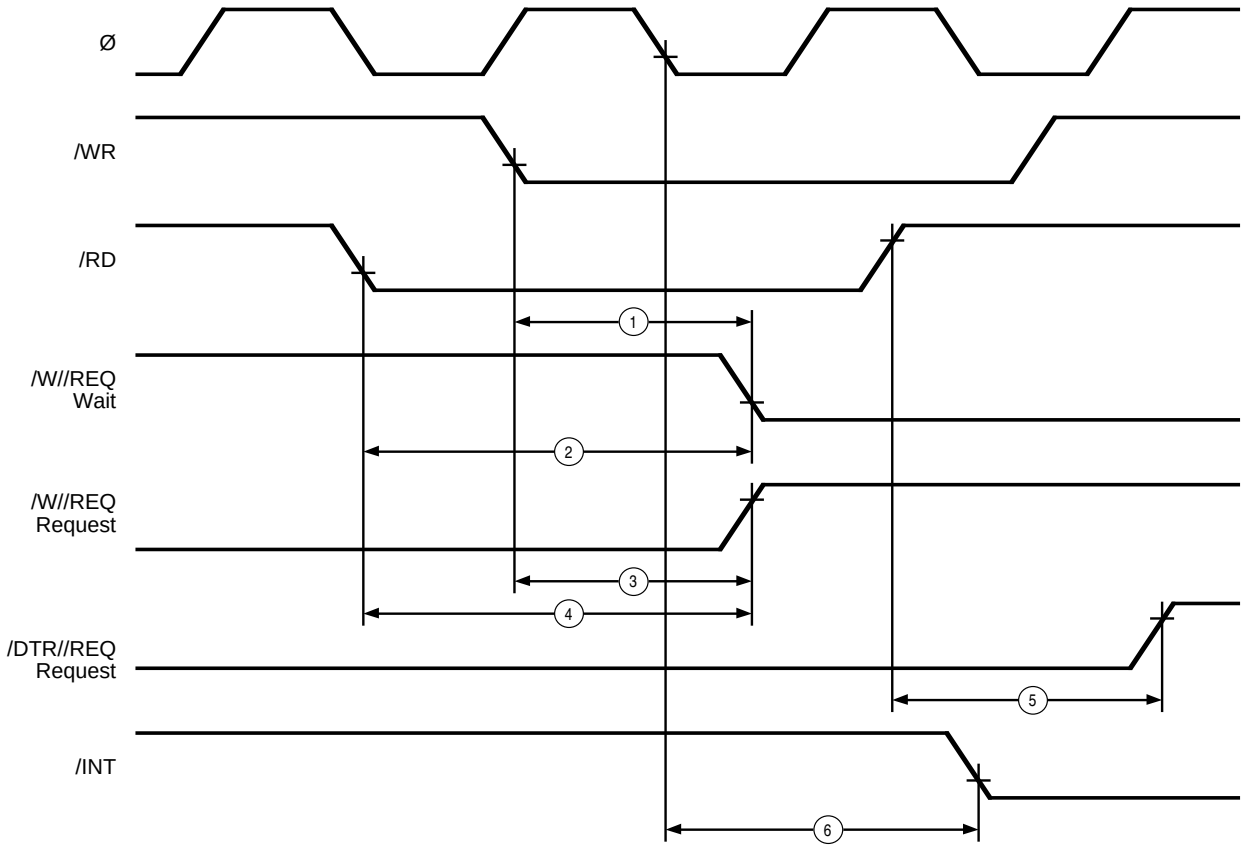


Figure 104. ESCC AC Parameter

Table B. ESCC Timing Parameters

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Unit
1	TdWR(W)	/WR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50	
3	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		65	
4	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		65	
5	TdRdr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay		TBD	
6	TdPC(INT)	Clock to /INT Valid Delay		160	

ORDERING INFORMATION

Z8L182	Z80182
20 MHz	**33 MHz**
Z8L18220ASC	Z8018233ASC
Z8L18220FSC	Z8018233FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

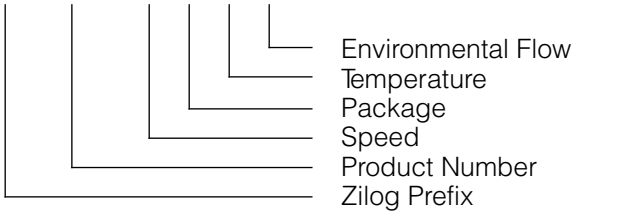
Preferred Package
A = VQFP (Very Small QFP)
F = Plastic Quad Flatpack

Preferred Temperature
S = 0°C to +70°C

Speeds
20 = 20 MHz
33 = 33 MHZ

Environmental
C = Plastic Standard
D = Plastic Stressed
E = Hermetric Standard

Example:
Z 80182 20 F S C is a Z80182, 20 MHz, QFP, 0°C to +70°C, Plastic Standard Flow



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