Zilog - Z8018233FSG1838 Datasheet

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Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z80180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	33MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	5.0V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8018233fsg1838

Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100% software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

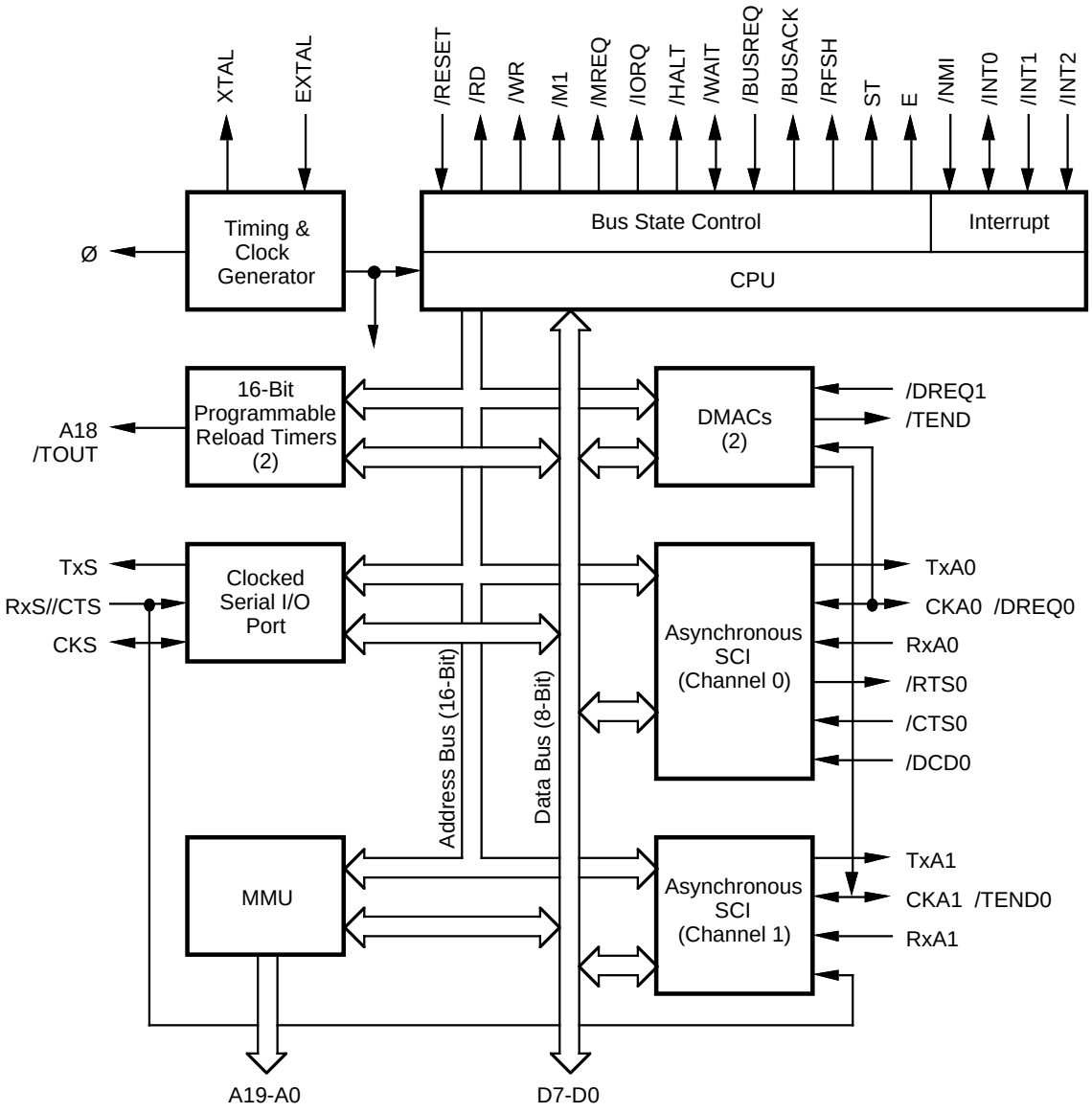


Figure 4. S180 MPU Block Diagram of Z182

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

PROGRAMMING (Continued)

Table 9. Z80182/Z8L182 ESCC, PIA and MISC Registers

Register Name	MPU Addr/Access		PC Addr/Access
WSG Chip Select Register	xxD8H	R/W	None
Z80182 Enhancements Register	xxD9H	R/W	None
PC Data Direction Register	xxDDH	R/W	None
PC Data Register	xxDEH	R/W	None
Interrupt Edge/Pin MUX Control	xxDFH	R/W	None
ESCC Chan A Control Register	xxE0H	R/W	None
ESCC Chan A Data Register	xxE1H	R/W	None
ESCC Chan B Control Register	xxE2H	R/W	None
ESCC Chan B Data Register	xxE3H	R/W	None
PB Data Direction Register	xxE4H	R/W	None
PB Data Register	xxE5H	R/W	None
RAMUBR RAM Upper Boundary Register	xxE6H	R/W	None
RAMLBR RAM Lower Boundary Register	xxE7H	R/W	None
ROM Address Boundary Register	xxE8H	R/W	None
PA Data Direction Register	xxEDH	R/W	None
PA Data Register	xxEEH	R/W	None
System Configuration Register	xxEFH	R/W	None

ASCI CHANNELS CONTROL REGISTERS (Continued)

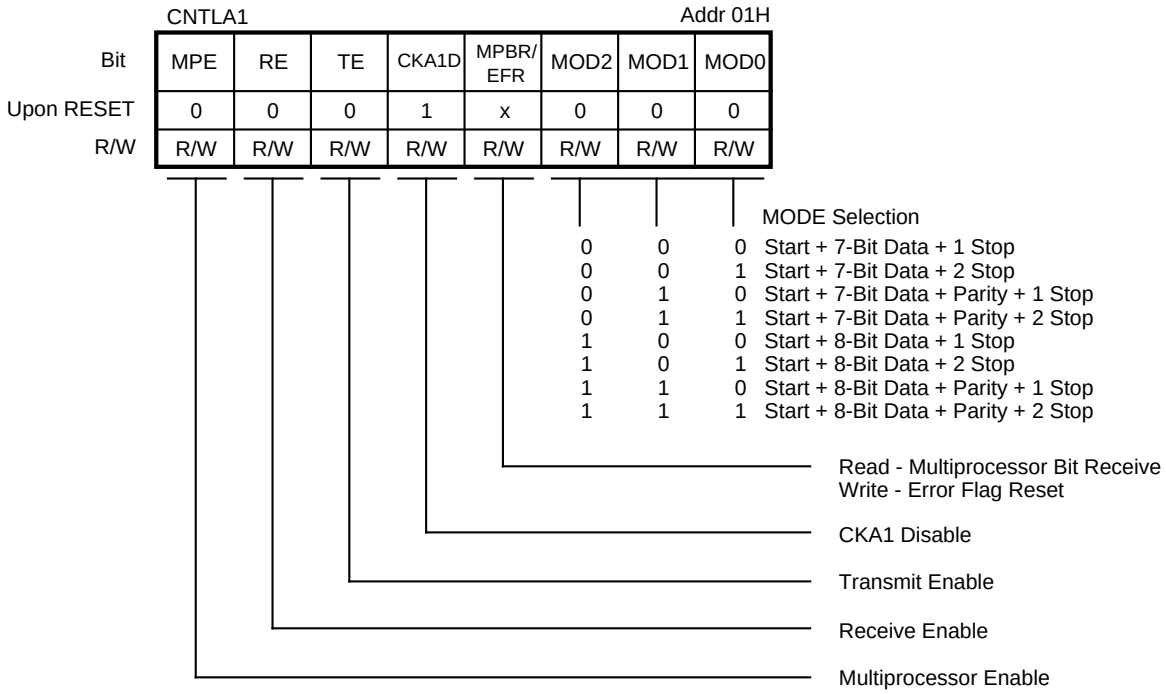
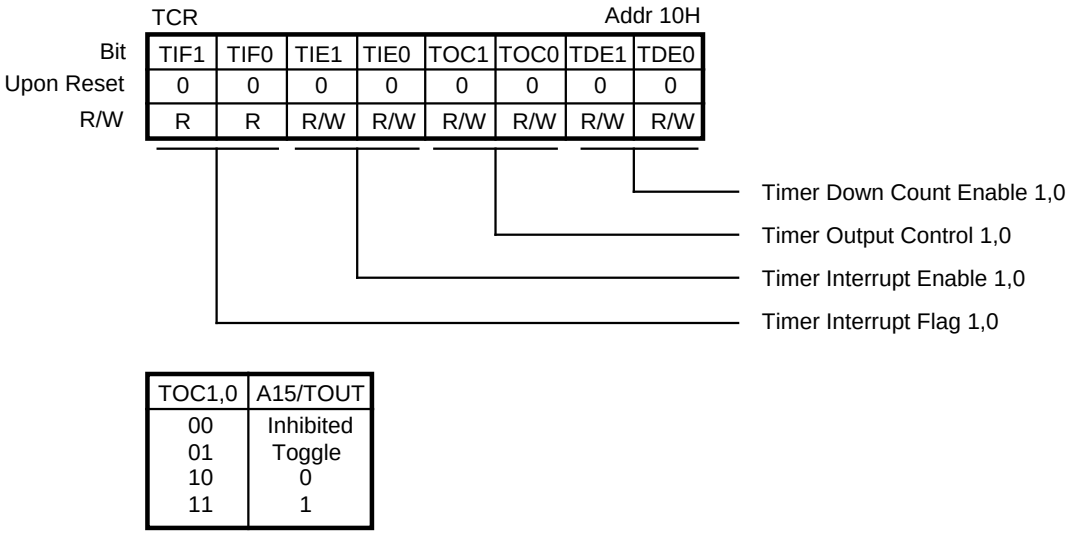


Figure 10b. ASCI Control Register A (Ch. 1)

TIMER CONTROL REGISTER



TOC1,0	A15/TOUT
00	Inhibited
01	Toggle
10	0
11	1

Figure 31. Timer Control Register

MMU REGISTERS

CBR — Addr 38H

Bit	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Common Base Register

Figure 43. MMU Common Base Register

BBR — Addr 39H

Bit	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Bank Base Register

Figure 44. MMU Bank Base Register

CBAR — Addr 3AH

Bit	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
Upon Reset	1	1	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Bank Area Register

MMU Common Area Register

Figure 45. MMU Common/Bank Area Register

SYSTEM CONTROL REGISTERS

IL — Addr 33H

Bit	IL7	IL6	IL5	-	-	-	-	-
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W					

Interrupt Vector Low

Figure 46. Interrupt Vector Low Register

ITC — Addr 34H

Bit	TRAP	UFO	-	-	-	ITE2	ITE1	ITE0
Upon Reset	0	0	1	1	1	0	0	1
R/W	R/W	R				R/W	R/W	R/W

/INT Enable 2, 1, 0
Undefined Fetch Object
TRAP

Figure 47. INT/TRAP Control Register

RCR — Addr 36H

Bit	REFE	REFW	-	-	-	-	CYC1	CYC0
Upon Reset	1	1	1	1	1	1	0	0
R/W	R/W	R/W					R/W	R/W

Cycle Select
Refresh Wait State
Refresh Enable

CYC1, 0	Interval of Refresh Cycle
00	10 states
01	20 states
10	40 states
11	80 states

Figure 48. Refresh Control Register

CONTROL REGISTERS

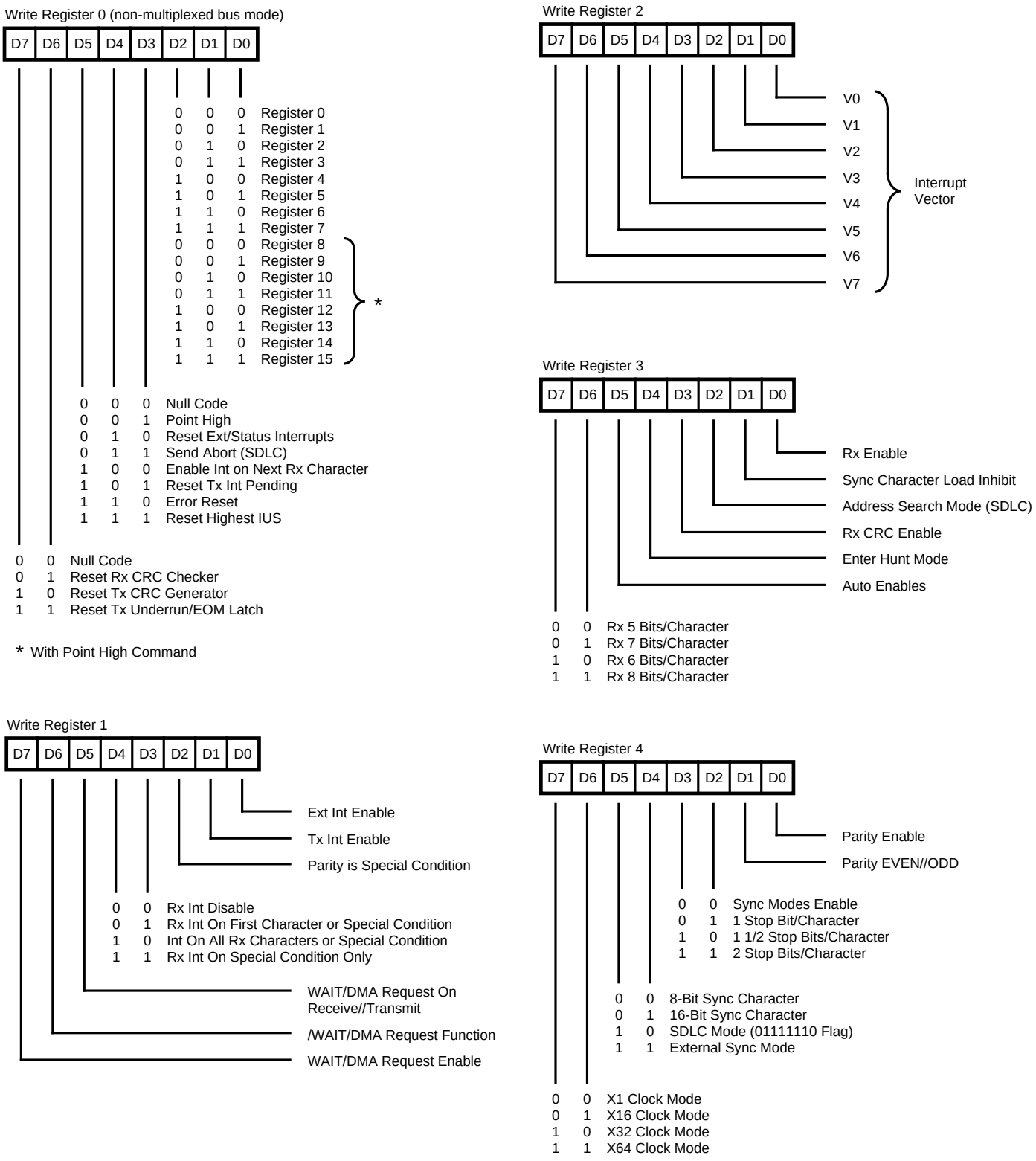


Figure 52. Write Register Bit Functions

CONTROL REGISTERS (Continued)

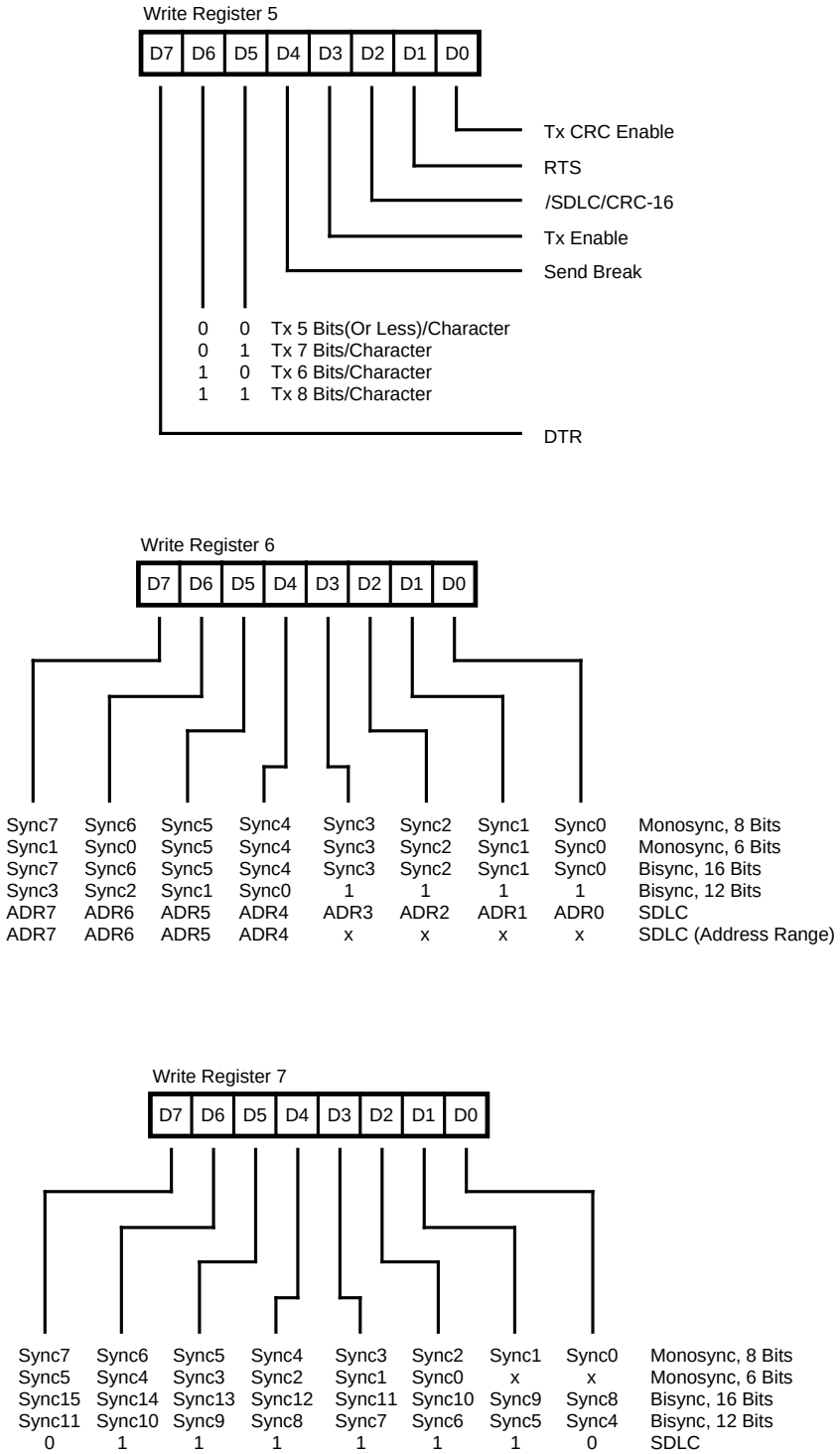


Figure 52. Write Register Bit Functions (Continued)

CONTROL REGISTERS (Continued)

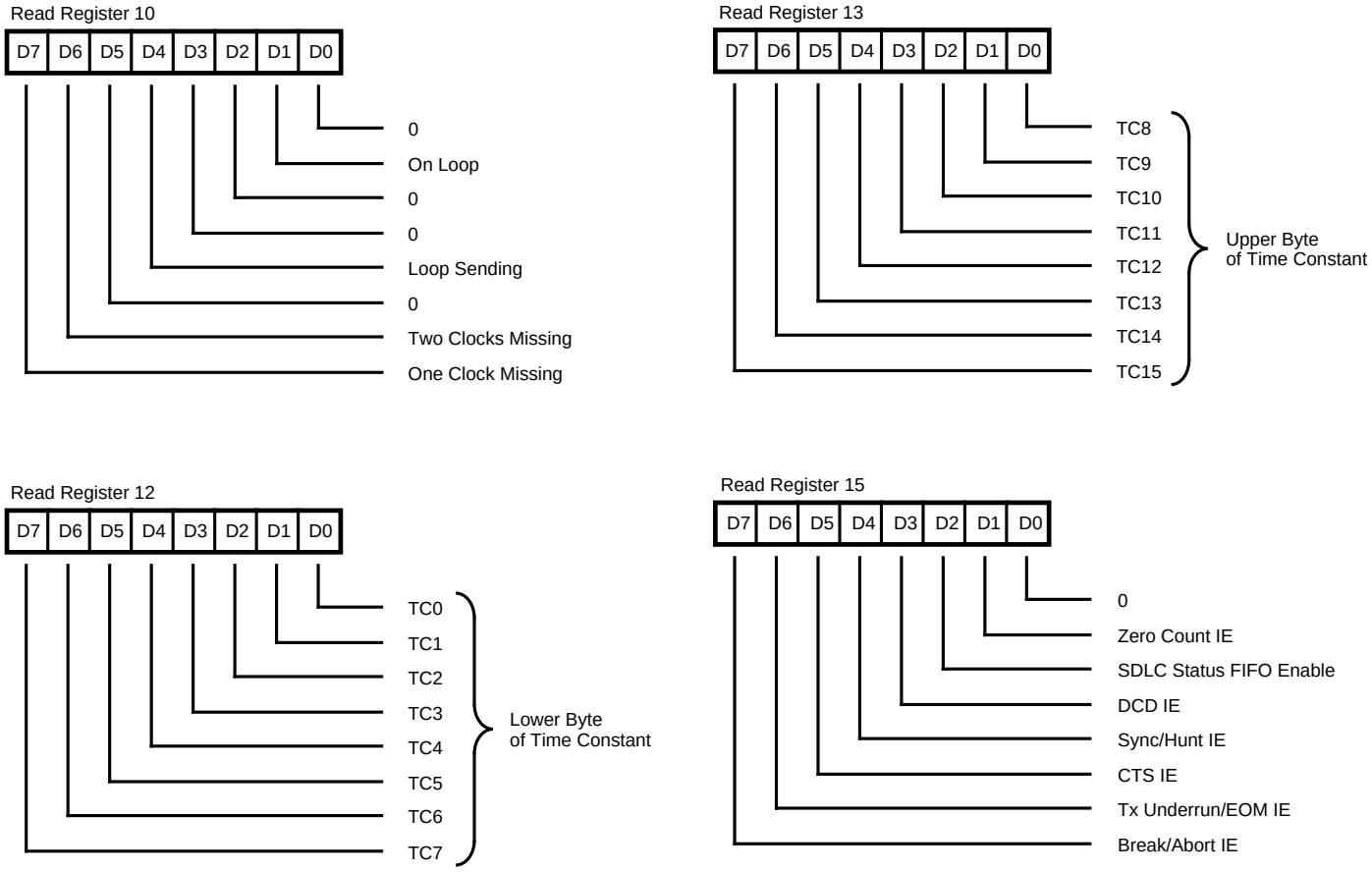


Figure 53. Read Register Bit Functions

Interrupt Vector Register (Continued)

Table 16. Interrupt Status Bits

Bits 3, 2, 1	Interrupt Request
000	NO IRQ
001	FCR or Tx OVRN IRQ
010	DLL/DLM IRQ
011	LCR IRQ*
100	MCR IRQ*
101	RBR IRQ
110	TTO IRQ
111	THR IRQ

Note: * The order of LCR and MCR does not follow that of the IE Register.

Bit 0 0/Opcode (Read/Write)
This bit is always 0 when the VIS bit is 1. If the VIS bit is 0, this bit reads back what was last written to it.

The Interrupt Vector Register serves both interrupt modes. When the VIS bit is 0, the last value written to the register can be read back. If the VIS bit is 1, and an interrupt is pending, the value read is the last value written to the upper nibble plus the status for the interrupt that is pending. If no interrupt is pending, then the last value written to the upper nibble plus the lower nibble is read from the register.

If the vector includes the status, then the lower four bits of the vector change asynchronously depending on the interrupting source. Since this vector changes asynchronously, then the interrupt service routine to read the IVEC register might read the source of the most recent IRQ/INTACK cycle if that IRQ does not have its IUS set.

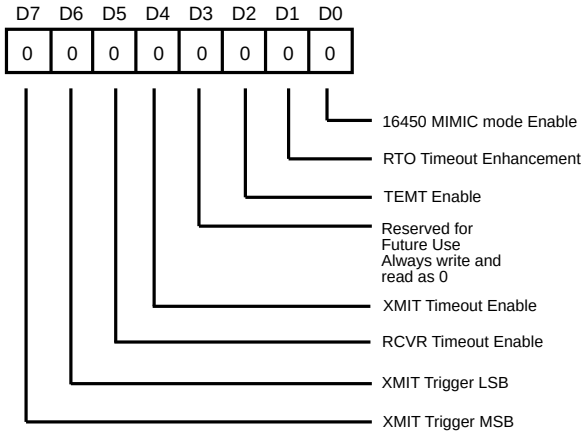


Figure 64. FIFO Status and Control Register
(Z180 MPU Read/Write, Address xxECH)

Bit 7 and Bit 6 XMIT Trigger MSB,LSB
This field determines the number of bytes available to read in the transmitter FIFO before an interrupt occurs to the MPU (Table 17).

Table 17. Transmitter Trigger Level

b7	b6	Level (# bytes)
0	0	1
0	1	4
1	0	8
1	1	14

Bit 5 Receive Timeout Enable
This bit enables the Z80182/Z8L182 Receive Timeout Timer that is used to emulate the four character timeout delay that is specified by the 16550. If no read or write to the RCVR FIFO has taken place and data bytes are available, but are below the PC trigger level. If this timer reaches zero, an interrupt is sent to the PC.

Bit 4 Transmitter Timeout Enable
This bit enables the Z80182/Z8L182 timer that is used to interrupt the Z180 MPU if characters are available, but are below the trigger level. The timer is enabled to count down if this bit is 1 and the number of bytes is below the set transmitter trigger level. The timer will timeout and interrupt the MPU if no read or write to the XMIT FIFO takes place within the timer interval.

Bit 3 Reserved. Program to zero.

Bit 2 (Reset value = 0) TEMT/Double Buffer
When enabled the Tx buffer can hold one extra byte (2 bytes total in 16450 mode). **(Do not enable in 16550 mode.)**

TEMT Emulation
If character delay emulation is not used the TEMT bit is automated. (Refer to page 26 for TEMT/Double Buffer information.)

Bit 1 RTO Timeout Enhancement
(Reset value = 0) Setting this bit will enable the RTO timeout to emulate the 16550 device. When enabling this feature, the receive timeout timer will not begin counting down until the character emulation timer for each byte of data in the Rx FIFO has expired.

Bit 0 16450 MIMIC Mode Enable
(Reset value=0) This bit = 1 will force the mimic into 16450 mode. Bit 0 in the FCR reg is forced to zero as well as the mimic internal FIFO enable. When used, this bit should be programmed at MIMIC initialization and not modified afterwards.

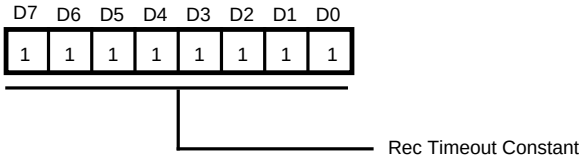


Figure 65. Receive Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEAH)

This register contains an 8-bit constant for emulation of the 16550 four character timeout feature. Software must determine the value to load into this register based on the bit rate and word length specified by the MIMIC interface with the PC. This timer receives its input from the /TRxCB Clock of the ESCC. This timer is enabled to down count when the enable bit in the FSR register is set and the trigger level interrupt has not been activated on the RCVR FIFO. The counter reloads and counts down each time there is a read or write to the RCVR FIFO.

The receive timeout timer is enhanced to emulate the actual 16550 when bit 1 of the FIFO status and control register is enabled. Under most circumstances, this register should be programmed for four character timers (40d, 8-N-1).

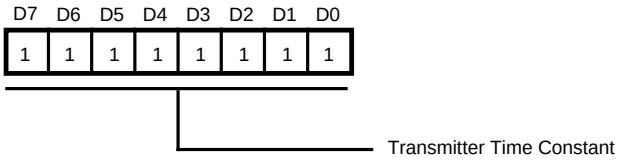


Figure 66. Transmit Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEBH)

This register contains an 8-bit constant for determining the interval for the Transmit Timeout Timer. If allowed to decrement to zero, this timer interrupts the MPU by setting the THR bit in the IUS/IP register. This timer receives its input from the /TRxCB Clock of the SCC. The timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the XMIT FIFO. The counter reloads each time there is a read or write to the XMIT FIFO.

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z180™ MPU and the PC/XT/AT, two timers have been added to alleviate any software problems that a high speed parallel data transfer might cause. These timers allow the programmer to slow down the data transfer just as if the 16550 MIMIC interface had to shift the data in and out serially. The Timers receive their input from the /TRxCB Clock since, in 16550 MIMIC mode, the ESCC channel B is disabled. For example, the clock source for the 8-bit registers: RTTC (Receive Timeout Time Constant, xxEAH), TTTC (Transmit Timeout Time Constant, xxEBH), TTCR (Transmit Time Constant Register, xxFAH) and RTCR (Receive Time Constant Register, xxFBH) uses the /TRxCB Clock output. The /TRxCB Clock output needs to be generated by the ESCC's channel B's 16-bit BRG as its clock source, thus allowing the programmer to access a total of 24 bits as a timer to slow down the data transfer.

In most cases, ESCC Ch. B BRG should be programmed to output at a frequency equivalent to the desired serial transfer rate. The output of the BRG should be routed to the /TRxCB pin.

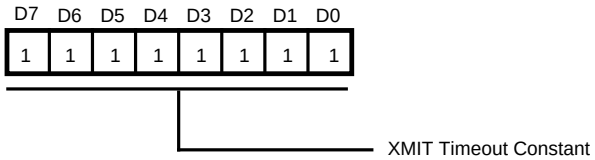


Figure 67. Transmitter Time Constant Register
(Z180 MPU Read/Write, Address xxFAH)

16550 MIMIC REGISTERS (Continued)

FIFO Control Register

Bit 6 and Bit 7 RCVR trigger LSB and MSB bits
This 2-bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs (see Table 18).

Bit 4 and Bit 5
Reserved for future use (PC side). Note: From the MPU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side will clear a previously set bit 4 or bit 5.

Bit 3 DMA mode select
Setting this bit to 1 will cause the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A 1 in this bit enables multi-byte DMA).

Bit 2 XMIT FIFO Reset
Setting this bit to 1 will cause the transmitter FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 1 RCVR FIFO Reset
Setting this bit to 1 will cause the receiver FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 0 FIFO Enable
The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be 1 when writing to the other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared. This feature can be forced in a disabled state by the MPU.

Table 18. Receive Trigger Level

b7	b6	Trigger Level, Number of Bytes
0	0	1
0	1	4
1	0	8
1	1	14

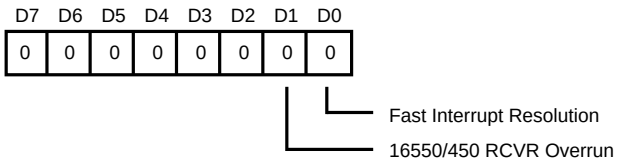


Figure 72. MIMIC Modification Register
(Z180 MPU Write only, Address xxE9h)

Bit 7-2 Reserved. Program to zero.

Bit 1 RCVR Overrun Modification
The actual 16450/16550 device allows the last position in FIFO to be overwritten by DCE during receiver overrun condition. When this bit is enabled (programmed to 1) the last position in FIFO can be overwritten by Z180 during receiver overrun. This feature is disabled by default. When this modification is not enabled, the MIMIC will ignore any write to RBR during an overrun condition.

Bit 0 Fast MIMIC-ESCC Interrupt Resolution
When enabling this modification, the internal MIMIC IEO signal into the ESCC IEI input is forced Low when the MIMIC Interrupt line becomes active. This is required to prevent the ESCC from putting it's vector on the databus during an INTACK cycle (given that the MIMIC is programmed to have higher interrupt priority).

When disabled, the internal MIMIC IEO becomes deasserted only after an interrupt acknowledge cycle. In this case, it is possible for the ESCC to force it's interrupt vector onto the data bus even when the MIMIC has a pending interrupt and is higher in priority.

Although this bit is disabled by default, it is advised that this bit is enabled to prevent interrupt conflict between MIMIC and ESCC interrupts.

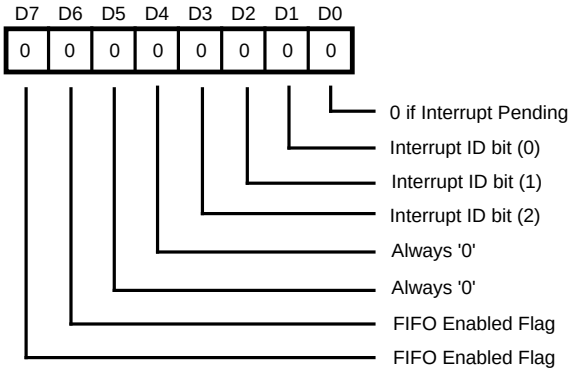


Figure 73. Interrupt Identification Register
(PC Read Only, Address 02H)
(Z180 MPU no access)

Interrupt Identification Register

Bit 7 and Bit 6 FIFO's Enabled
These bits will read 1 if the FIFO mode is enabled on the MIMIC.

Bit 5 and Bit 4 Always Read 0
Reserved bits.

Bits 3-1 Interrupt ID Bits
This 3-bit field is used to determine the highest priority interrupt pending (see Table 19).

Bit 0 Interrupt Pending
This bit is logic 0 and interrupt is pending.

When the PC accesses the IIR, the contents of the register and all pending interrupts are frozen. Any new interrupts will be recorded, but not acknowledged, during the IIR access.

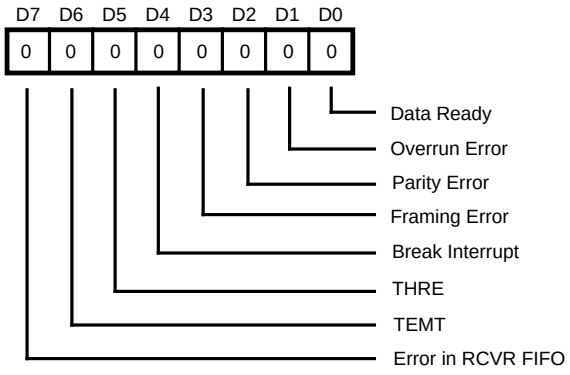


Figure 74. Line Status Register
(PC Read Only, Address 05H)
(Z180 MPU Read/Write bits 6, 4, 3, 2, Address xxF5H)

Table 19. Interrupt Identification Field

b3	b2	b1	Priority	Interrupt Source	INT Reset Control
0	1	1	Highest	Overrun, Parity, Framing error or Break detect bits set by MPU	Read Line Status Register
0	1	0	2nd	Received Data trigger level	RCVR FIFO drops below trigger level
1	1	0	2nd	Receiver Timeout with data in RCVR FIFO.	Read RCVR FIFO
0	0	1	3rd	Transmitter Holding Register Empty.	Writing to the Transmitter Holding Register or reading the Interrupt Identification Register when the THRE is the source of the interrupt.
0	0	0	4th	MODEM status: CTS, DSR, RI or DCD	Reading the MODEM status register.

Z80182 ENHANCEMENTS REGISTER

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode
If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit is used to allow DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TxDA Tri-state
The TxDA pin can be tri-stated on assertion of the /HALT pin. This prevents the TxDA from driving and external device when /HALT output is used to force other devices into power-down modes. This feature is disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider
The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock will be Z180's PHI clock divided by two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5V or 10 MHz/3V, this bit should be set for ESCC divide-by-two mode.

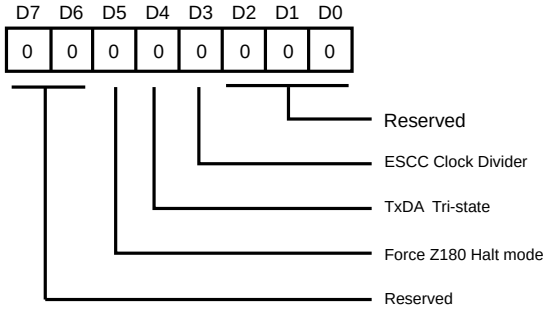
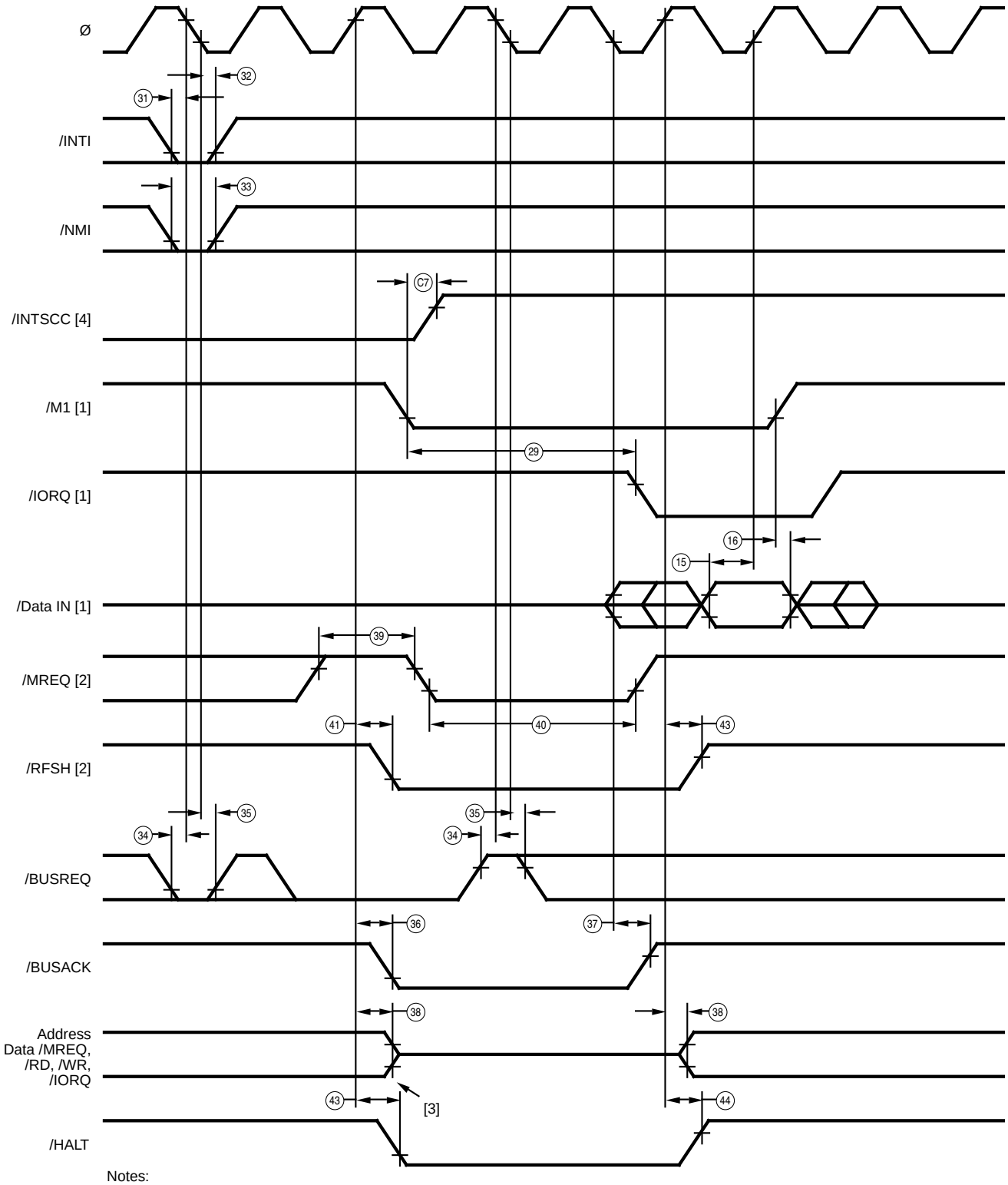


Figure 82. Z80182 Enhancements Register
(Z180 MPU Read/Write, Address xxD9H)

TIMING DIAGRAMS (Continued)



Notes:
[1] During /INT0 acknowledge cycle
[2] During refresh cycle
[3] Output buffer is off at this point
[4] Refer to Table C, parameter 7

Figure 91. CPU Timing
(/INT0 Acknowledge Cycle, Refresh Cycle, BUS RELEASE Mode
HALT Mode, SLEEP Mode, SYSTEM STOP Mode)

TIMING DIAGRAMS (Continued)

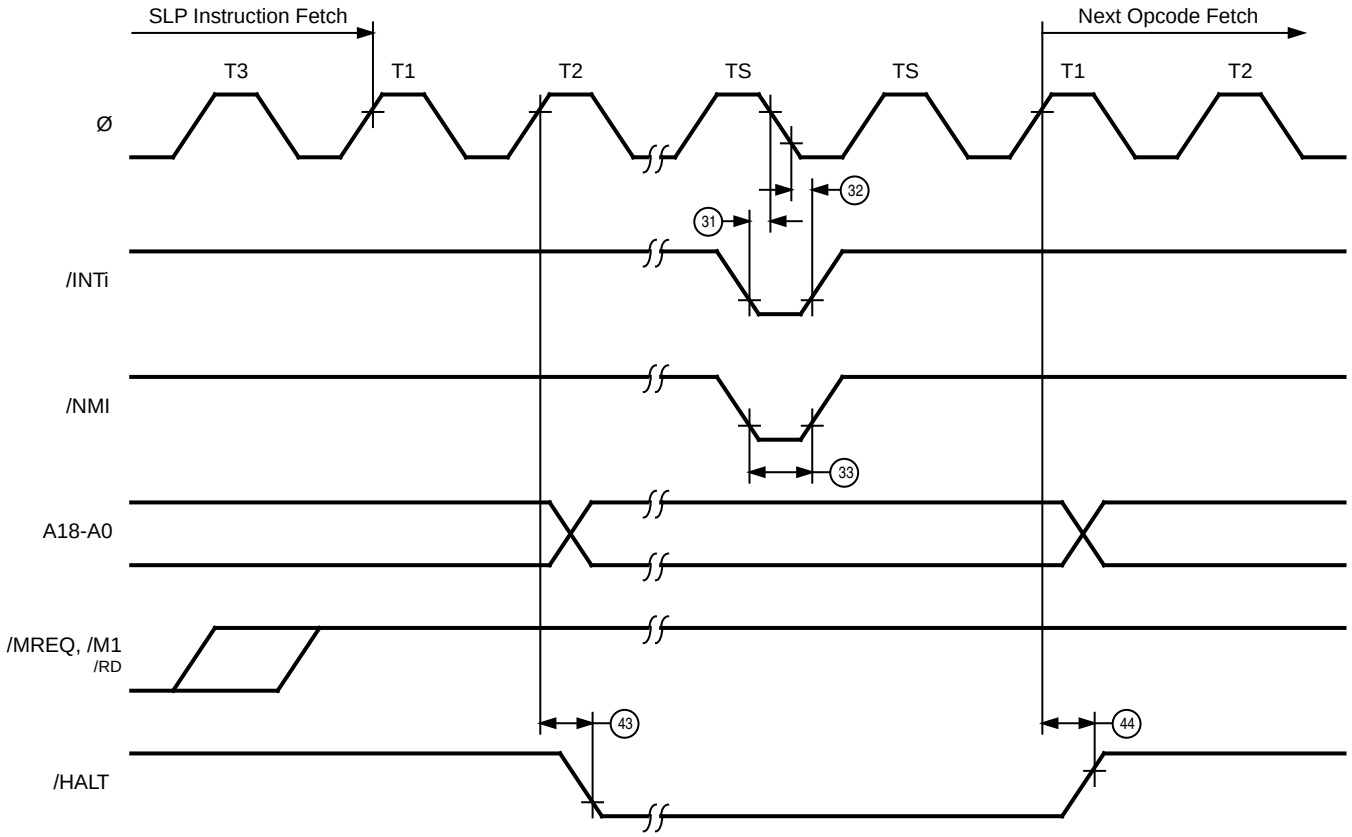


Figure 98. SLEEP Execution Cycle

Table D. Z85230 System Timing Table

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Notes [4]
1	TdRxC(REQ)	/RxC to /W//REQ Valid	13	18	[2]
2	TdRxC(W)	/RxC to /Wait Inactive	13	18	[1,2]
3	TdRxC(SY)	/RxC to /SYNC Valid	9	13	[2]
4	TdRxC(INT)	/RxC to /INT Valid	15	22	[1,2]
5	TdTxC(REQ)	/TxC to /W//REQ Valid	8	12	[3]
6	TdTxC(W)	/TxC to /Wait Inactive	8	15	[1,3]
7	TdTxC(DRQ)	/TxC to /DTR//REQ Valid	7	11	[3]
8	TdTxC(INT)	/TxC to /INT Valid	9	14	[1,3]
9	TdSY(INT)	/SYNC to /INT Valid	2	6	[1]
10	TdExT(INT)	/DCD or /CTS to /INT Valid	3	9	[1]

Notes:
These AC parameters values are preliminary and subject to change without notice.
[1] Open-drain output, measured with open-drain test load.
[2] /RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[3] /TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[4] Units equal to TcPc

Table E. I/O Port Timing

No.	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
1	TsPIA(RD)	Port Data Input Setup to /RD Fall	20		20	
2	ThPIA(RD)	Port Data Input Hold From /RD Rise	0		0	
3	$TdWR_F$(PIA)	Port Data Output Delay From /WR Fall		60		60
4	T_FWR_F(PIA)	Port Data Output Float From /WR Fall	0		0	

Table F. External Bus Master Timing

No.	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
1	TsA(IORQf)	Address to /IORQ Fall Setup	10		5	
2	TsIOf(WRf)	/IORQ Fall to /WR Fall Setup	0		0	
3	TsIOf(RDf)	/IORQ Fall to /RD Fall Setup	0		0	
4	ThIOR(WR_R)	/IORQ Rise From /WR Rise Hold	0		0	
5	ThIOR(RD_R)	/IORQ Rise From /RD Rise Hold	0		0	
6	TdRDf(DO)	/RD Fall to Data Out Valid Delay		50		45
7	T_HRD_R(DO)	/RD Rise to Data Out Valid Hold		0		0
8	$T_SD(WR_R)$	Data In to /WR Fall Setup	50		50	
9	THD(WR_R)	Data In From /WR Rise Hold	10	8	10	

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Refer to Figures 106 thru 112 for MIMIC AC Timing.

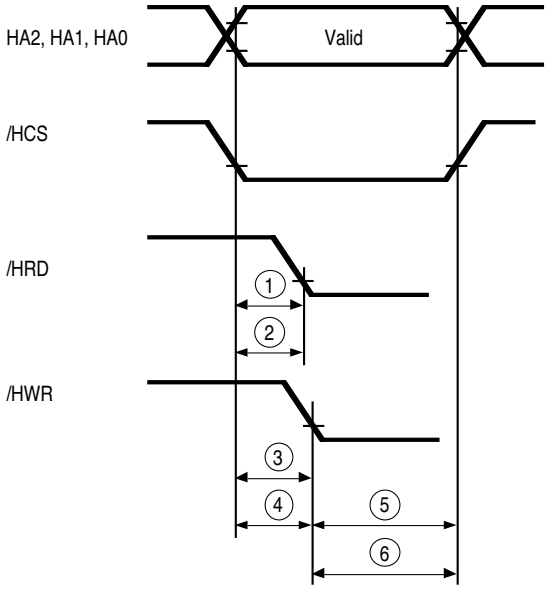

Figure 110. PC Host /RD /WR Timing

Table H. PC Host /RD /WR Timing

No	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
1	tAR	/HRD Delay from Address	30		30		ns
2	tCSR	/HRD Delay from /HCS	30		30		ns
3	tAW	/HWR Delay from Address	30		30		ns
4	tCSW	/HWR Delay from /HCS	30		30		ns
5	tAh	Address Hold Time	20		20		ns
6	tCSh	/HCS Hold Time	20		20		ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

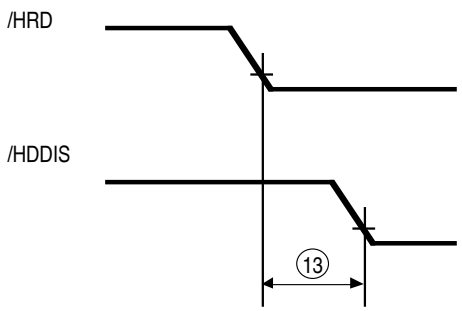

Figure 113. Driver Enable Timing

Table J. Driver Enable Timing

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
13	tRDD	/HRD to Driver Enable/Disable		60		60	ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

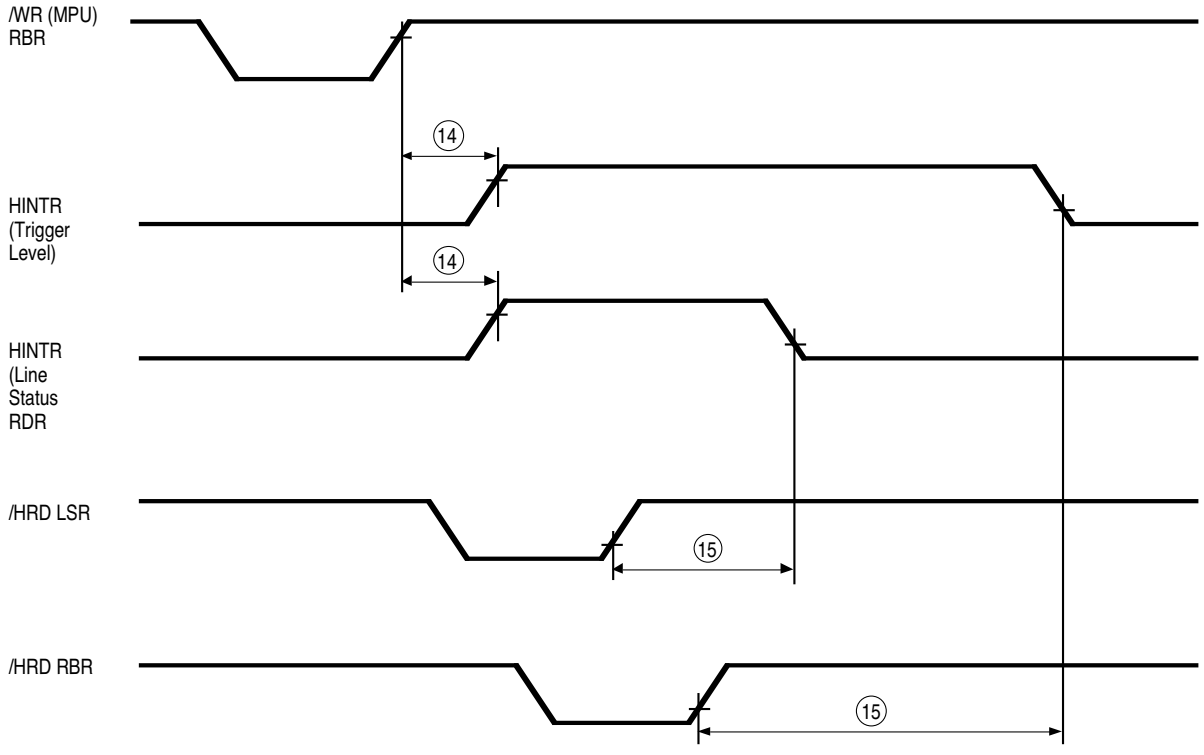

Figure 114. Interrupt Timing RCVR FIFO