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Understanding Embedded - Microprocessors

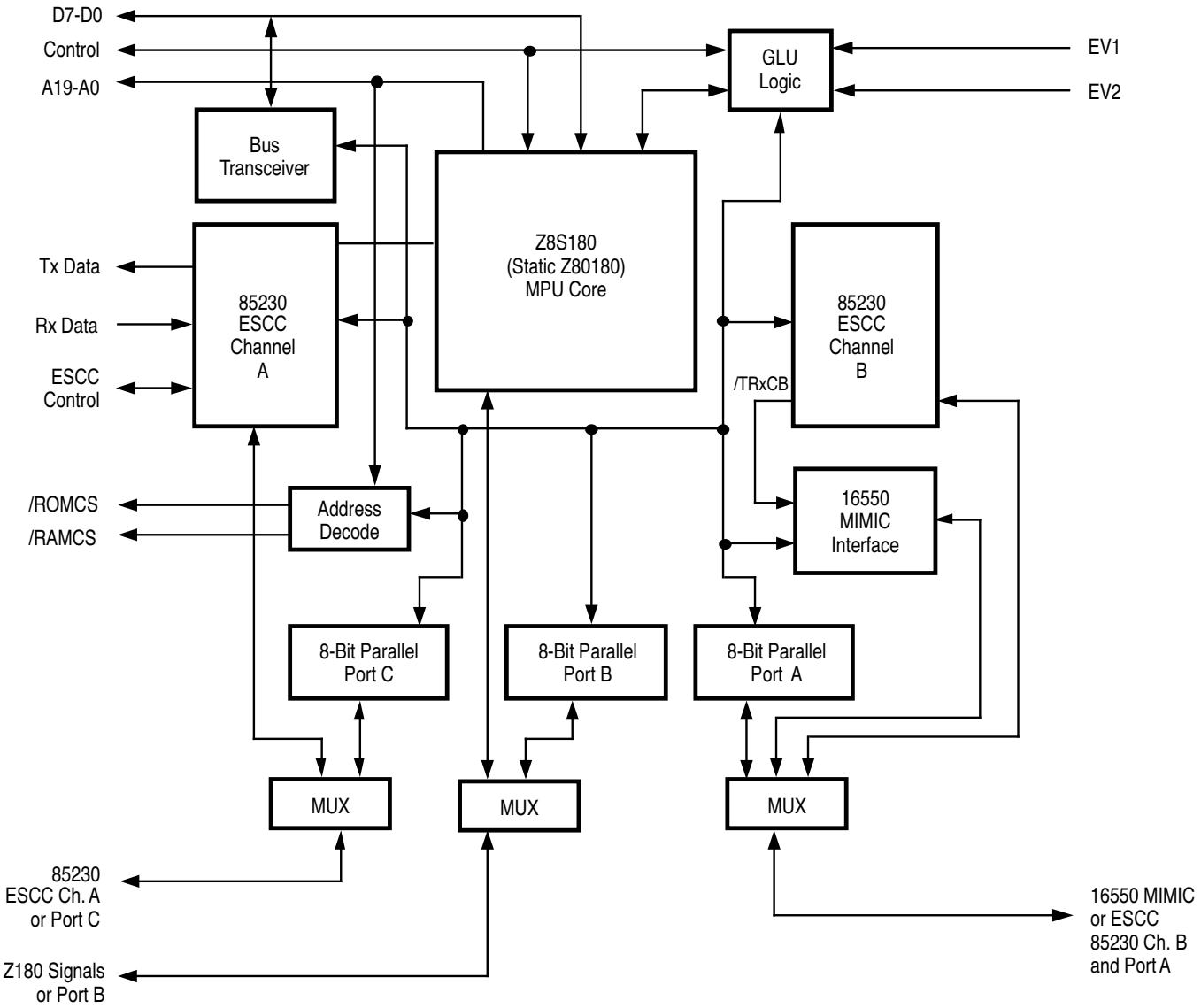
Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l18220aec

GENERAL DESCRIPTION (Continued)



Note: Conventional use of the term "MPU side" refers to all interface through the Z180 MPU core and "PC side" refers to all interface through the16550 MIMIC interface.

Figure 1. Z80182/Z8L182 Functional Block Diagram

GENERAL DESCRIPTION (Continued)

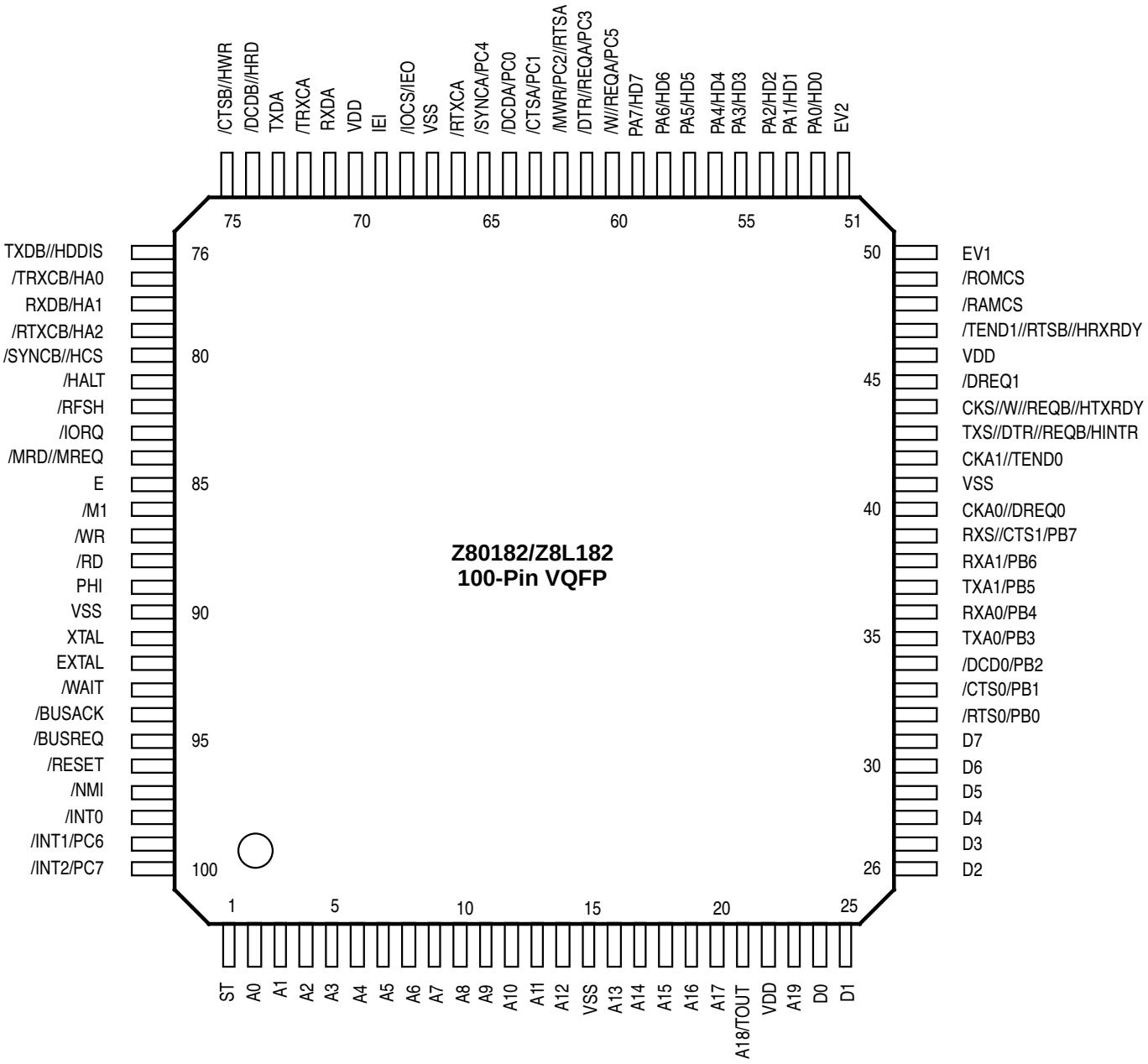


Figure 3. Z80182/Z8L182 100-Pin VQFP Pin Configuration

/W//REQB. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

16550 MIMIC INTERFACE SIGNALS

HD7-HD0. *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

/HDDIS. *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

HA2-HA0. *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

/HCS. *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

/HWR. *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

/HRD. *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

HINTR. *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

/HTxRDY. *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

/HRxRDY. *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

PARALLEL PORTS

PA7-PA0. *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

PC7-PC0. *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

MULTIPLEXED PIN DESCRIPTIONS (Continued)

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
41	44	V_{SS}			
42	45	CKA1//TEND0			
43	46	TxS	/DTR//REQB	HINTR	SYS CONF REG Bit 1,2
44	47	CKS	/W//REQB	/HTxRDY	SYS CONF REG Bit 1,2
45	48	/DREQ1			
46	49	V_{DD}			
47	50	/TEND1	/RTSB	/HRxRDY	SYS CONF REG Bit 1,2
48	51	/RAMCS			
49	52	/ROMCS			
50	53	EV1			
51	54	EV2			
52	55	PA0	HD0		SYS CONF REG Bit 1
53	56	PA1	HD1		SYS CONF REG Bit 1
54	57	PA2	HD2		SYS CONF REG Bit 1
55	58	PA3	HD3		SYS CONF REG Bit 1
56	59	PA4	HD4		SYS CONF REG Bit 1
57	60	PA5	HD5		SYS CONF REG Bit 1
58	61	PA6	HD6		SYS CONF REG Bit 1
59	62	PA7	HD7		SYS CONF REG Bit 1
60	63	/W//REQA	PC5		SYS CONF REG Bit 7
61	64	/DTR//REQA	PC3		SYS CONF REG Bit 7
62	65	/MWR	PC2	RTSA	SYS CONF REG Bit 7 *
63	66	/CTSA	PC1		SYS CONF REG Bit 7
64	67	/DCDA	PC0		SYS CONF REG Bit 7
65	68	/SYNCA	PC4		SYS CONF REG Bit 7
66	69	/RTxCA			
67	70	V_{SS}			
68	71	/IOCS	IEO		INT EDG/PIN REG Bit 2
69	72	IEI			
70	73	V_{DD}			

Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100% software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

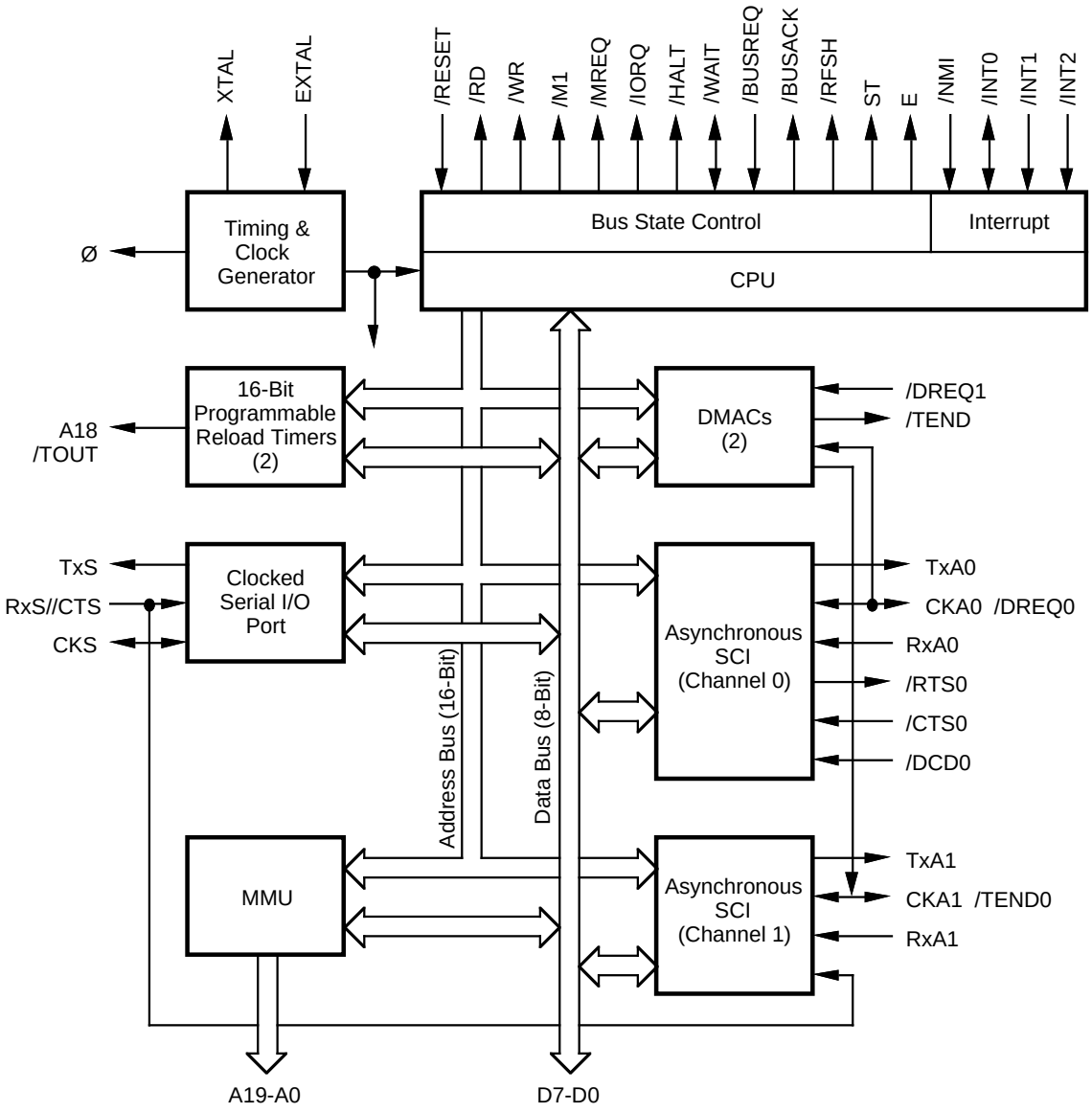


Figure 4. S180 MPU Block Diagram of Z182

Z85230 ESCC™ FUNCTIONAL DESCRIPTION

The Zilog Enhanced Serial Communication Controller ESCC™ is a dual channel, multiprotocol data communication peripheral. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions including on-chip baud rate generators, digital phase-lock loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, synchronous byte-oriented protocols such as IBM® Bisync, and synchronous bit-oriented protocols such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (telecommunication, LAN, etc.)

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem control in both channels in applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

With access to 14 Write registers and 7 Read registers per channel (number of the registers varies depending on the version), the user can configure the ESCC to handle all synchronous formats regardless of data size, number of stop bits, or parity requirements. The ESCC also accommodates all synchronous formats including character, byte, and bit-oriented protocols.

Within each operating mode, the ESCC also allows for protocol variations by checking odd or even parity bits, character insertion or deletion, CRC generation, checking break and abort generation and detection, and many other protocol-dependent features.

The ESCC (Enhanced SCC) is pin and software compatible to the CMOS SCC version. The following enhancements were made to the CMOS SCC:

- Deeper Transmit FIFO (4 bytes)
- Deeper Receive FIFO (8 bytes)
- Programmable FIFO interrupt and DMA request level
- Seven enhancements to improve SDLC link layer supports:
  - Automatic transmission of the opening flag
  - Automatic reset of Tx Underrun/EOM latch
  - Deactivation of /RTS pin after closing flag
  - Automatic CRC generator preset
  - Complete CRC reception
  - TxD pin automatically forced High with NRZI encoding when using mark idle
  - Status FIFO handles better frames with an ABORT
  - Receive FIFO automatically unlocked for special receive interrupts when using the SDLC status FIFO
- Delayed bus latching for easier microprocessor interface
- New programmable features added with Write Register 7' (WR seven prime)
- Write registers, 3, 4, 5 and 10 are now readable
- Read register 0 latched during access
- DPLL counter output available as jitter-free transmitter clock source
- Enhanced /DTR, /RTS deactivation timing

16550 MIMIC FIFO DESCRIPTION

The receiver FIFO consists of a 16-word FIFO capable of storing eight data bits and three error bits for each character stored (Figure 7). Parity error, Framing error and Break detect bits are stored along with the data bits by copying their value from three shadow bits that are Write Only bits for the Z80180 MPU LSR address. The three shadow bits are cleared after they are copied to the FIFO memory. In FIFO mode, to write error bits into the receiver FIFO, the MPU must first write the Parity, Framing and Break detect status to the Line Status Register (shadow bits) and then write the character associated into the receiver buffer. The data and error bits will then move into the same address in the FIFO. The error bits become available to the PC side of the interface when that particular location becomes the next address to read (top of FIFO). At that time, they may either be read by the PC by accessing them in the LSR, or they may cause an interrupt to the PC interface if so enabled. The error bits are set by the error status of the byte at the top of the FIFO, but may only be cleared by reading the LSR. If successive reads of the receiver FIFO are performed without reading the LSR, the status bits will be set if any of the bytes read have the respective error bit set. See Table 6 for the setting and clearing of the Line Status Register bits.

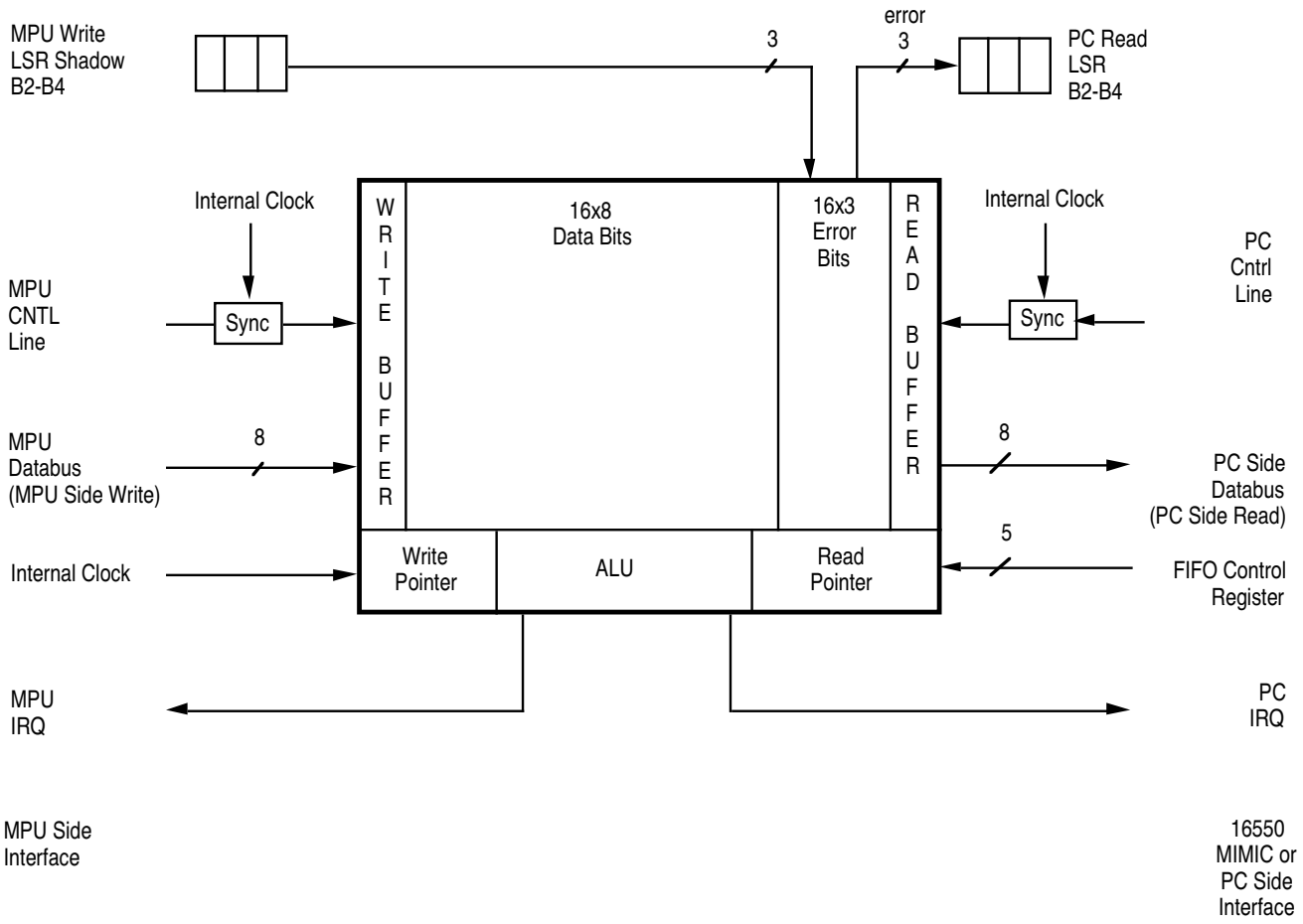
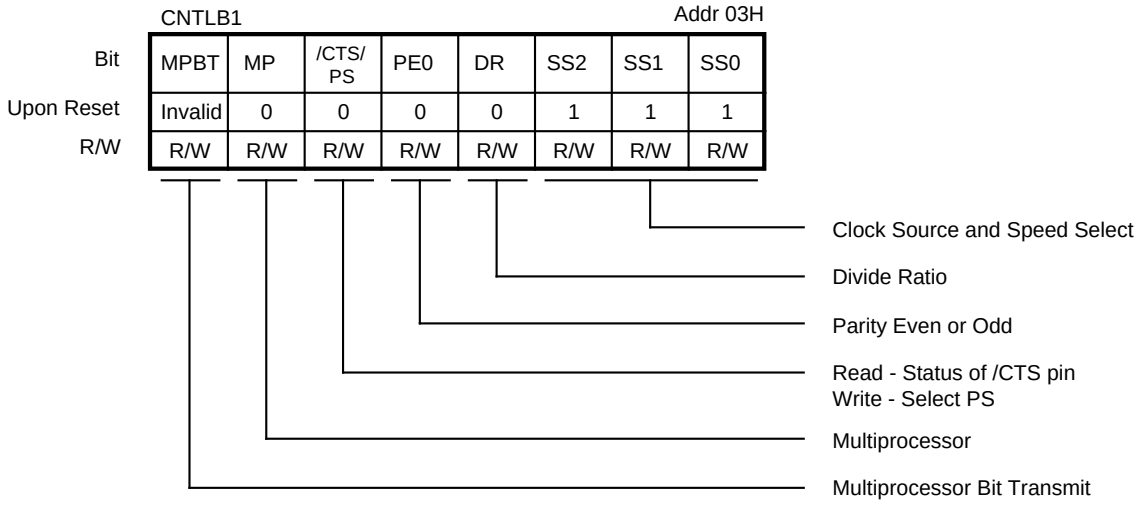


Figure 7. 16550 MIMIC Receiver FIFO Block Diagram

ASCI CHANNELS CONTROL REGISTERS (Continued)



General Divide Ratio SS, 2, 1, 0	PS = 0 (Divide Ratio = 10) DR = 0 (x16)	DR = 1 (x64)	PS = 1 (Divide Ratio = 30) DR = 0 (x16)	DR = 1 (x64)
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
*111	External Clock (Frequency < Ø ÷ 40)			

Note:
* Baud rate is external clock rate ÷ 16; therefore, Ø ÷ (40 x 16) is maximum baud rate using external clocking.

Figure 12. ASCI Control Register B (Ch. 1)

TIMER DATA REGISTERS

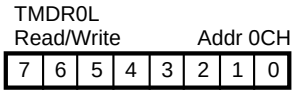


Figure 23. Timer 0 Data Register L

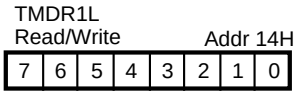
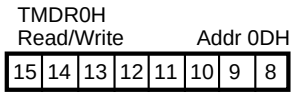
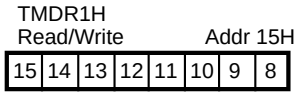


Figure 24. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 25. Timer 0 Data Register H



When Read, read Data Register L before reading Data Register H.

Figure 26. Timer 1 Data Register H

TIMER RELOAD REGISTERS

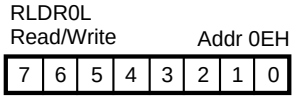


Figure 27. Timer 0 Reload Register L

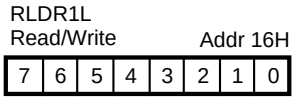


Figure 28. Timer 1 Reload Register L

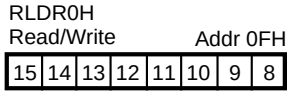


Figure 29. Timer 0 Reload Register H

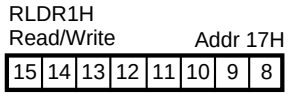


Figure 30. Timer 1 Reload Register H

Z85230 ESCC™ CONTROL REGISTERS

See Figures 52 and 53 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification /Technical Manual.

The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. ***It is recommended that /TRxCB be programmed as an output with proper baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.***

Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

PROGRAMMING THE ESCC™

The ESCC contains write registers in each channel that are programmed by the system separately to configure the functional uniqueness of the channels.

In the ESCC, the data registers are directly addressed by selecting a High on the D//C pin. With all other registers (with the exception of WR0 and RR0), programming the write registers requires two write operations and reading the read registers, both a write and a read operation. The first write is to WR0 and contains three bits that point to the selected register. The second write is the actual control word for the selected read register accessed. All of the ESCC registers, including the data registers, may be accessed in this fashion. The pointer bits are automatically cleared after the read or write operation so that WR0 (or RR0) is addressed again.

With the Z80182/Z8L182, a new feature is implemented in the ESCC. The Transmitter and Receiver is now capable of sending and comparing a 32-bit CRC-32 (Ethernet Polynomial):

$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$

This feature is enabled by access to WR7' Bit 7, which selects the 32-bit CRC polynomial for the transmitter and receiver and overrides any selection of SDLC/CRC-16 CRCs. When the 32-bit CRC override feature is enabled, the transmitter will only send 32-bit CRC when CRC is to be sent. On the receive side, the CRC comparison/calculation will be done only on 32-bit CRC values. The result of the 32-bit CRC comparison will be maintained in RR1 bit D6 in place of the 16-bit CRC comparison result. The 32-bit CRC compare result will also be maintained in the 10x19 FIFO for frames in which 32-bit CRC is enabled. The CRC still can be preset to all 0s or all 1s. 32-bit CRC is disabled upon power-up or reset.

Note: The ESCC cannot do simultaneous calculation/ comparison using both 16-bit and 32-bit CRC.

Also, for the Z80182/Z8L182 only, the clock provided to the ESCC core is equal to the system clock divided by 1 or 2. The divider is programmed in the Z80182 Enhancement Register bit 3.

Divide-by-two should be programmed when running the Z182 beyond:

- 20 MHz, 5V
- 10 MHz, 3V

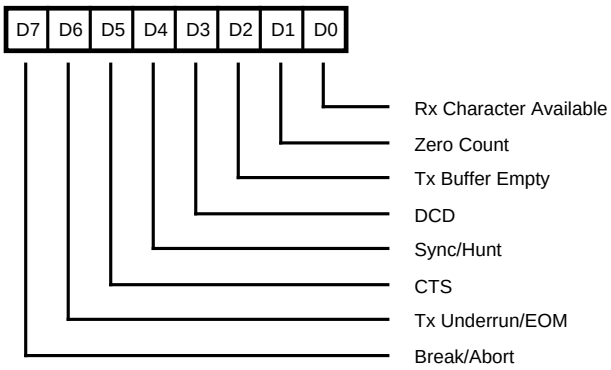
Note: Upon power-up or reset the system clock is equal to the ESCC clock.

Initialization. The system program first issues a series of commands to initialize the basic mode of operation. This is followed by other commands to qualify conditions within the selected mode. For example, in the Asynchronous mode, character length, clock rate, number of stop bits, and even or odd parity should be set first. Then the interrupt mode is set, and finally, the receiver and transmitter are enabled.

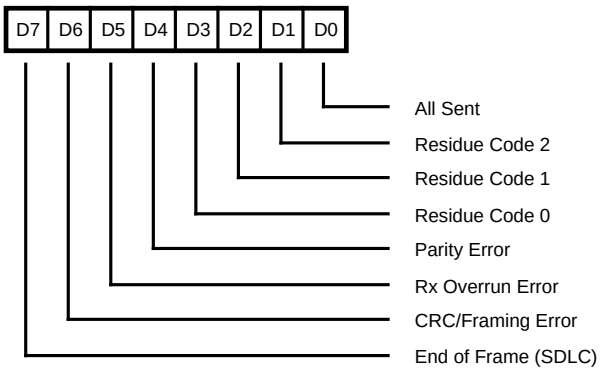
Write Registers. The ESCC contains 16 write registers (17 counting the transmit buffer) in each channel. These write registers are programmed separately to configure the functional "personality" of the channels. There are two registers (WR2 and WR9) shared by the two channels that are accessed through either of them. WR2 contains the interrupt vector for both channels, while WR9 contains the interrupt control bits and reset commands. A new register, WR7', was added to the ESCC and may be written to if WR15, D0 is set. Figure 50 shows the format of each write register.

Read Registers. The ESCC contains ten read registers (eleven, counting the receive buffer (RR8) in each channel). Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15). Two registers (RR12 and RR13) are read to learn the baud rate generator time constant. RR2 contains either the unmodified interrupt vector (channel A) or the vector modified by status information (channel B). RR3 contains the Interrupt Pending (IP) bits (channel A only). RR6 and RR7 contain the information in the SDLC Frame Status FIFO, but is only read when WR15, D2 is set. If WR7' D6 is set, Write Registers WR3, WR4, WR5, WR7, and WR10 can be read as RR9, RR4, RR5, and RR14, respectively. Figure 51 shows the format of each Read register.

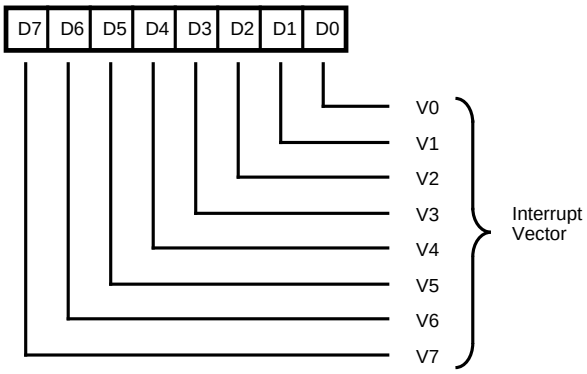
Read Register 0



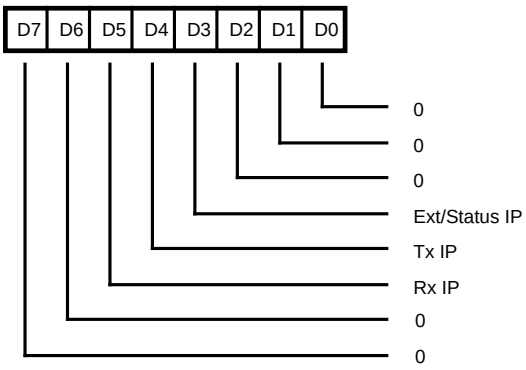
Read Register 1



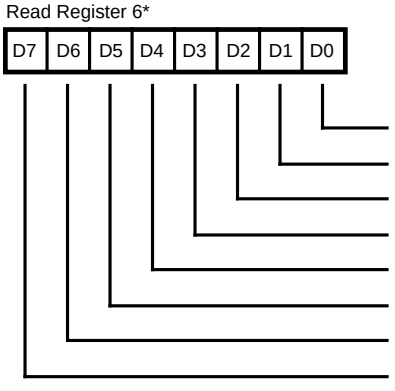
Read Register 2



Read Register 3



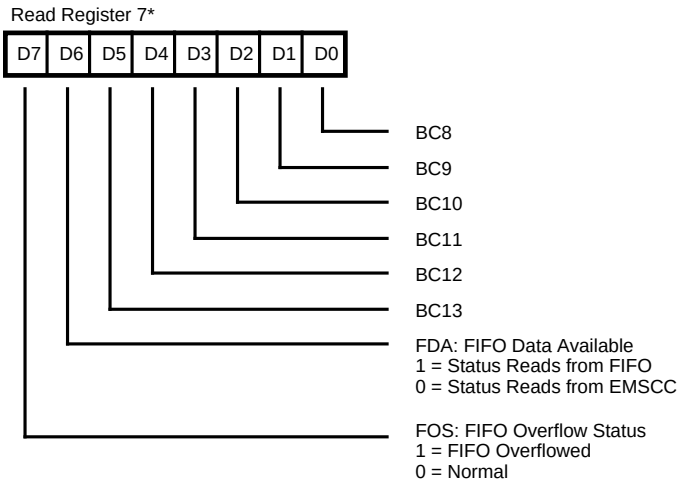
Read Register 6*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Read Register 7*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Figure 52. Write Register Bit Functions (Continued)

16550 MIMIC INTERFACE REGISTERS

MIMIC Master Control Register (MMC)

The 16550 MIMIC interface is controlled by the MMC register. Setting it allows for different modes of operation such as using the 8-bit counters, DMA accesses, and which IRQ structure is used with the PC/XT/AT.

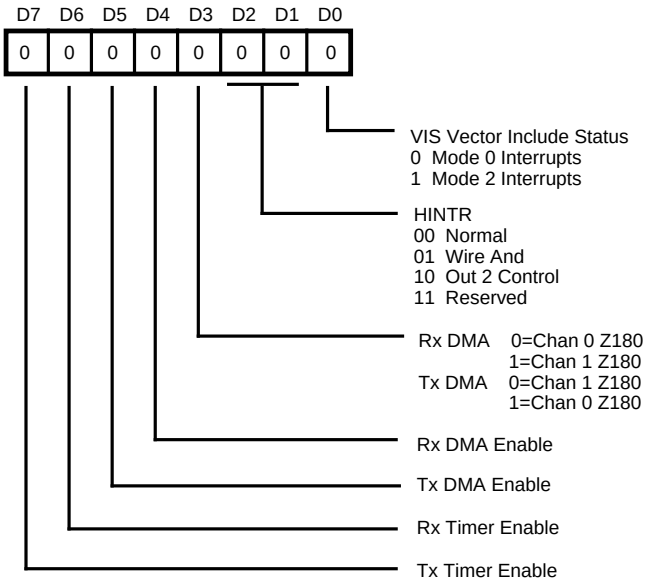


Figure 60. MIMIC Master Control Register
(Z180 MPU Read/Write, Address xxFFH)

Bit 7 Transmit Emulation Delay Counter Enable (Read/Write)
If bit 7 is set to 1, it enables the transmit delay timer. When the Z180 reads the Transmit Register, it loads the transmit delay timer from the Transmit Time Constant Register and enables the timer to count down to zero. This timer delays setting the Transmit Holding Register Empty (THRE) bit until the timer times out. If this bit is 0, then THRE is set immediately on a Z180 read of the Transmit Register. This bit also enables the emulation timer used in Transmitter Double Buffering.

Bit 6 Receive Emulation Delay Counter Enable (Read/Write)
If bit 6 is set to 1, it enables the receive delay timer. When the Z180 writes to the Receive Buffer, it loads the receive delay timer from the Receive Time Constant Register and enables the timer to count down to zero. This timer delays setting the Data Ready (DR) bit in the LSR until the timer times out. If this bit is 0 then DR is set immediately on a Z180 write to the Receive Buffer.

Both counters are single pass and stop on a count of Zero. Their purpose is to delay data transfer just as if the 16550 UART had to shift the data in and out. This is provided to alleviate any software problems a high speed continuous data transfer might cause to existing software. If this is not a concern, then data can be read and written as fast as the two machines can access the devices. In FIFO mode of operation , the timers are used to delay the status to the PC interface by the time required to actually shift the characters out, or in, if an actual UART were present.

Bit 5 Transmit DMA Enable (Read/Write)
If this bit is set to 1, it enables the Transmit DMA function.

Bit 4 Receive DMA Enable (Read/Write)
If this bit is set to 1, it enables the Receive DMA function.

Bit 3 Receive DMA Channel Select (Read/Write)
If bit 3 is set to 0, then Receive DMA transfer is done through Z180 DMA channel 0 and the Transmit DMA is done through DMA channel 1. If bit 3 is set to 1, then Receive DMA transfer is done through Z180 DMA channel 1 and the Transmit DMA is done through DMA channel 0.

Bits 2,1 Interrupt Select (Read/Write).
See Table 15.

Bit 0 Vector Include Status (Read/Write)
This bit is used to select the interrupt response mode of the Z180. A 0 in this bit enables Mode 0 interrupts; a 1 enables Mode 2 response.

Table 15. MIMIC Master Control Register Interrupt Select

Bit 2	Bit 1	HINTR Function
0	0	HINTR is set to normal 16550 MIMIC mode. A fully driven output is required when external priority arbiters are used.
0	1	A wired AND condition on the HINTR pin is possible to the PC/XT/AT. The interrupt is active High with only the pull-up of the HINTR pin driving; otherwise this pin is tri-state. Wired AND is needed when an external arbiter is not available.
1	0	HINTR is driven when out 2 of the Modem Control Register is 1. HINTR is tri-state when MCR out 2 is 0.
1	1	RESERVED

16550 MIMIC REGISTERS (Continued)

Modem Status Register

Bit 7 Data Carrier Detect
This bit must be written by the Z180 MPU.

Bit 6 Ring Indicator
This bit must be written by the Z180 MPU.

Bit 5 Data Set Ready
This bit must be written by the Z180 MPU.

Bit 4 Clear to Send
This bit must be written by the Z180™ MPU.

Bit 3 Delta Data Carrier Detect
This bit is set to 1 whenever the Data Carrier Detect bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 2 Trailing Edge Ring Indicator
This bit is set to 1 on the falling edge of the Ring Indicator bit. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 1 Delta Data Set Ready
This bit is set to 1 whenever the Data Set Ready bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

Bit 0 Delta Clear To Send
This bit is set to 1 whenever the Clear To Send bit changes state. This bit is reset when the PC/XT/AT reads the Modem Status Register.

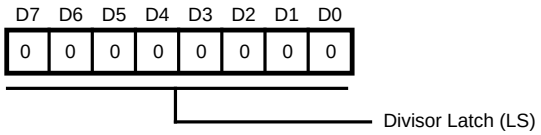


Figure 79. Scratch Register
(PC Read/Write, Address 07H)
(Z180 MPU Read Only, Address xxF7H)

Scratch Register

Bits 7-0 Scratch Register
This register is used by the PC/XT/AT programmer for temporary data storage. The Z180 MPU is able to read this register. If the PC/XT/AT writes to this register, no interrupt to the Z180 MPU is generated.

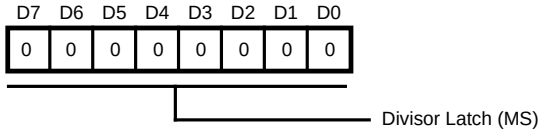


Figure 80. Divisor Latch (LS)
(PC Read/Write, Address 00H and DLAB=1)
(Z180 MPU Read Only, Address xxF8H)

Divisor Latch (LS)

Bit 7-0 Divisor Latch Most Significant Byte (MS)
This register contains the Low order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT will generate an interrupt to the Z180 MPU. It can then read the Baud rate divisor and set up the application.

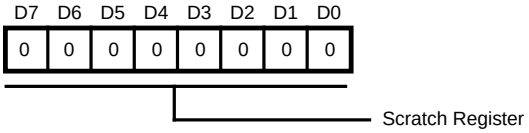


Figure 81. Divisor Latch (MS)
(PC Read/Write, Address 01H and DLAB=1)
(Z180 MPU Read Only, Address xxF9H)

Divisor Latch (MS)

Bit 7-0 Divisor Latch Most Significant Byte (MS)
This register contains the High order byte of the Baud rate divisor. Writing to this register with the PC/XT/AT will generate an interrupt to the Z180 MPU. It can then read the Baud rate divisor and set up the application.

Z80182 ENHANCEMENTS REGISTER

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode
If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit is used to allow DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TxDA Tri-state
The TxDA pin can be tri-stated on assertion of the /HALT pin. This prevents the TxDA from driving and external device when /HALT output is used to force other devices into power-down modes. This feature is disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider
The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock will be Z180's PHI clock divided by two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5V or 10 MHz/3V, this bit should be set for ESCC divide-by-two mode.

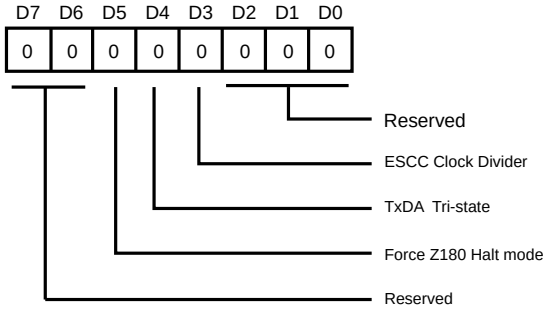


Figure 82. Z80182 Enhancements Register
(Z180 MPU Read/Write, Address xxD9H)

EMULATION MODES (Continued)

Table 21. Emulation Mode 1

Signal	Normal Mode 0	Emulation Adaptor Mode 1
PHI	Output	Input
/M1	Output	Input
/MREQ,/MRD	Output	Input
/IORQ	Output	Input
/RD	Output	Input
/WR	Output	Input
/RFSH	Output	Input
/HALT	Output	Input
ST	Output	Input
E	Output	Tri-state
/BUSACK	Output	Input
/WAIT	Input	Output
A19,A18/T_{OUT}	Output	Input
A17-A0	Output	Input
D7-D0	Input/Output	Input/Output
TxA0	Output	Tri-state
/RTS0	Output	Tri-state
TxA1	Output	Tri-state
/INT0	Input	Output, Open-Drain

Mode 2 Emulation Probe Mode
In the Emulator Probe Mode all of the Z182 output signals are tri-state. This scheme allows a Z182 emulator probe to grab on to the Z182 package leads on the target system.

Mode 3 RESERVED (for test purposes only)
This mode is reserved for test purpose only, do not use.

Notes:
Z182 has two branches of reset. /RESET controls the Z182 overall configuration, RAM and ROM boundaries, plus the ESCC, Port and the 16550 MIMIC interface. In Normal Mode, a "one shot" circuit samples the input of the /RESET pin to assert the internal reset to its proper duration. In Adapter Mode, this "one shot" circuit is bypassed. Note also that the Z180's crystal oscillator is disabled in Mode 1 and Mode 2.

In Mode 1 the emulator must provide /MREQ on the (/MREQ,/MRD) Z80182/Z8L182 pin (not /MRD); and A18 (not T_{OUT}) on the A18/T_{OUT} pin.

SLEEP, HALT EFFECT ON MIMIC AND 182 SIGNALS

The following Z80182/Z8L182 signals are driven High when Z180™ MPU enters a SLEEP or HALT state:

- /MRD when selected in the Interrupt Edge/Pin MUX Register.
- /MWR when selected in the Interrupt Edge/Pin MUX Register.
- /ROMCS,/RAMCS always High in SLEEP or HALT.

The following signals are High-Z during SLEEP and HALT:

- /IOCS when so selected in the Interrupt Edge/Pin MUX Register.
- /RD and /WR.

A0-A19 (A18 if selected) always High-Z in power down.

D0-D7 always High-Z in power down modes.

The MIMIC logic of the 182 is disabled during power down modes of the Z180.

TIMING DIAGRAMS (Continued)

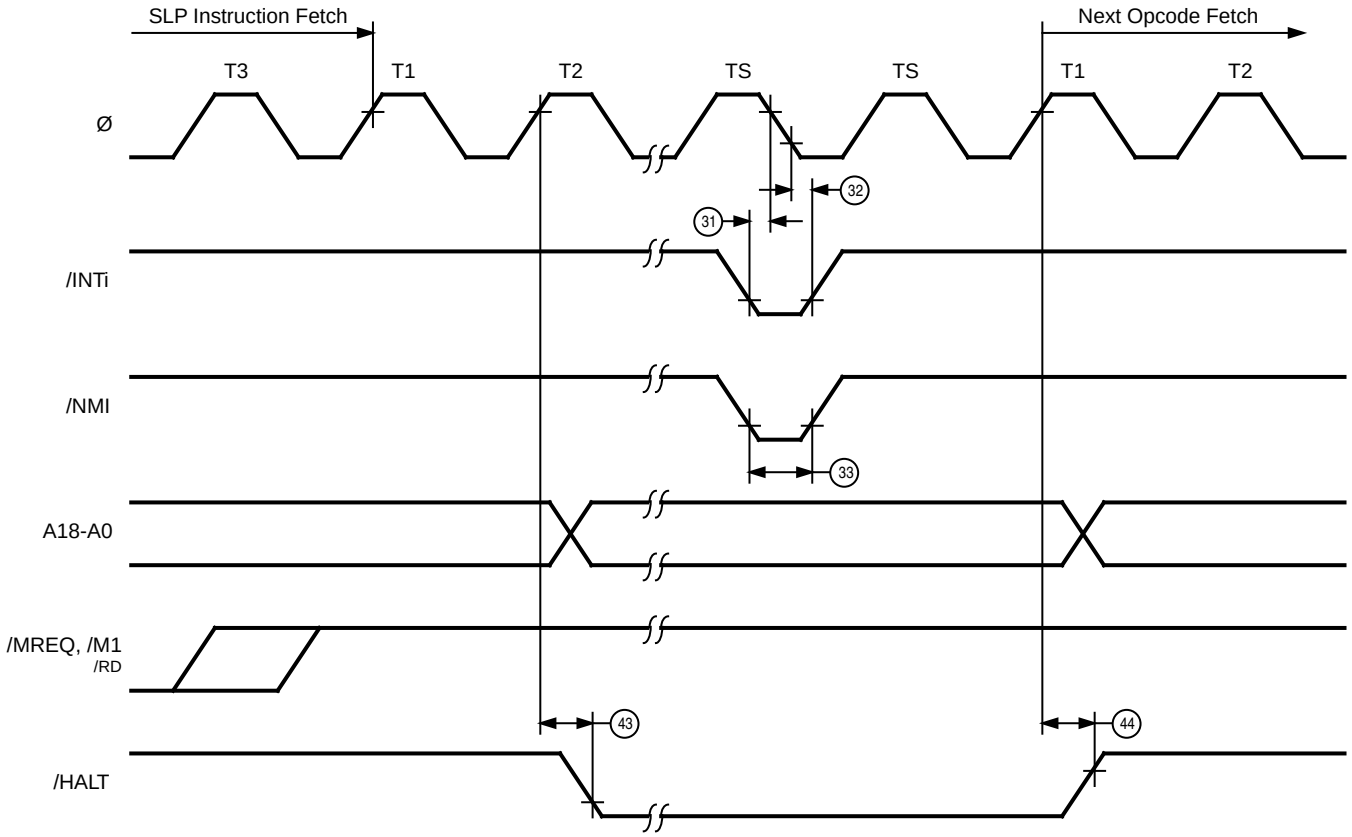


Figure 98. SLEEP Execution Cycle

Table C. Z85230 General Timing Table

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Notes
1	TdPC(REQ)	/PCLK to W/REQ Valid		70	
2	TdPC(W)	/PCLK to Wait Inactive		170	
3	TsRxC(PC)	/RxC to /PCLK Setup Time	N/A		[1,4]
4	TsRxD(RxCr)	RxD to /RxC Setup Time		0	[1]
5	ThRxD(RxCr)	RxD to /RxC Hold Time	45		[1]
6	TsRxD(RxCf)	RxD to /RxC Setup Time	0		[1,5]
7	ThRxD(RxCf)	RxD to /RxC Hold Time	45		[1,5]
8	TsSY(RxC)	/SYNC to /RxC Setup Time	–90		[1]
9	ThSY(RXC)	/SYNC to/RxC Hold Time	5TcPc		[1]
10	TsTxC(PC)	/TxC to /PCLK Setup Time	N/A		[2,4]
11	TdTxCf(TXD)	/TxC to TxD Delay		70	[2]
12	TdTxCr(TXD)	/TxC to TxD Delay		70	[2,5]
13	TdTxD(TRX)	TxD to TRxC Delay		70	
14	TwRTxh	RTxC High Width	70		[6]
15	TwRTxl	TRxC Low Width	70		[6]
16a	TcRTx	RTxC Cycle Time	200		[6,7]
16b	TxRx(DPLL)	DPLL Cycle Time Min	50		[7,8]
17	TcRTxx	Crystal Osc. Period	61	1000	[3]
18	TwTRxh	TRxC High Width	70		[6]
19	TwTRxl	TRxC Low Width	70		[6]
20	TcTRx	TRxC Cycle Time	200		[6,7]
21	TwExT	DCD or CTS Pulse Width	60		
22	TwSY	SYNC Pulse Width	60		

Notes:
These AC parameter values are preliminary and subject to change without notice.
[1] RxC is /RTxC or /TRxC, whichever is supplying the receive clock.
[2] TxC is /TRxC or /RTxC, whichever is supplying the transmit clock.
[3] Both /RTxC and /SYNC have 30 pF capacitors to ground connected to them.
[4] Synchronization of RxC to PCLK is eliminated in divide by four operation.
[5] Parameter applies only to FM encoding/decoding.
[6] Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to case PCLK requirements.
[7] The maximum receive or transmit data rate is 1/4 PCLK.
[8] Applies to DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock should have a 50% duty cycle.

16550 MIMIC TIMING

Refer to Figures 106 thru 112 for MIMIC AC Timing.

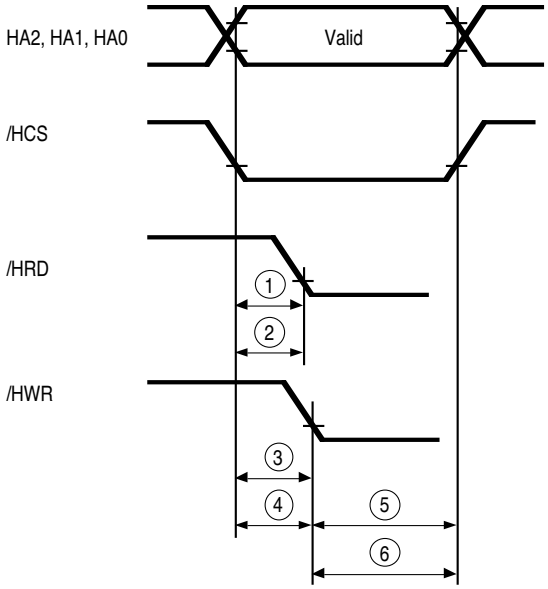


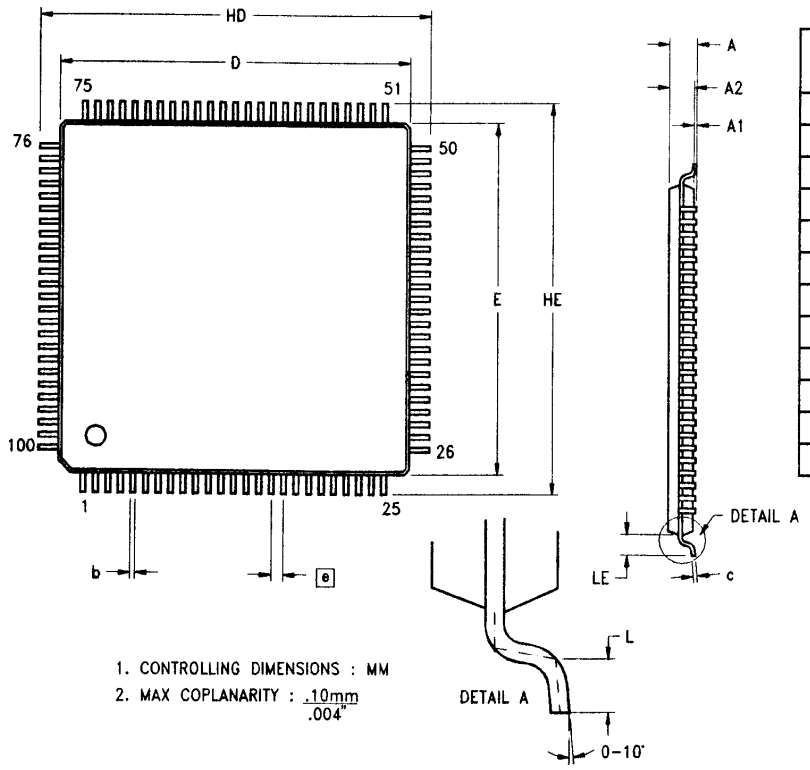
Figure 110. PC Host /RD /WR Timing

Table H. PC Host /RD /WR Timing

No	Symbol	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max	Units
1	tAR	/HRD Delay from Address	30		30		ns
2	tCSR	/HRD Delay from /HCS	30		30		ns
3	tAW	/HWR Delay from Address	30		30		ns
4	tCSW	/HWR Delay from /HCS	30		30		ns
5	tAh	Address Hold Time	20		20		ns
6	tCSh	/HCS Hold Time	20		20		ns

Note:
These AC parameter values are preliminary and are subject to change without notice.

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	1.35	1.60	.053	.063
A1	0.05	0.20	.002	.008
A2	1.30	1.50	.051	.059
b	0.15	0.26	.C06	.010
c	0.10	0.20	.004	.008
HD	15.85	16.15	.624	.636
D	13.90	14.10	.547	.555
HE	15.85	16.15	.624	.636
E	13.90	14.10	.547	.555
e	0.50 TYP		.0197 TYP	
L	0.35	0.65	.014	.026
LE	0.90	1.10	.035	.043

100-Pin VQFP Package Diagram