Zilog - Z8L18220AEG Datasheet

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l18220aeg

MULTIPLEXED PIN DESCRIPTIONS

A18/$T_{OUT.}$ During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, The T_{OUT} function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/T_{OUT}. Therefore, the selection of T_{OUT} will not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

CKA0//DREQ0. During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, /DREQ0 function is always selected.

CKA1//TEND0. During Reset, this pin is initialized as CKA1 pin. If CKA1D bit in the ASCI control register Ch1(CNTLA1) is set to 1, /TEND0 function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

RxS//CTS1. During Reset, this pin is initialized as the RxS pin. If CTS1E bit in the ASCI status register Ch1 (STAT1) is set to 1, /CTS1 function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 2 specifies. On Reset, both bits 1 and 2 are 0, so /TEND1,TxS,CKS are selected.

Table 2. Triple Multiplexed Pins

Bit 1	Bit 2	Master Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/RTSB,/DTR//REQB,/W//REQB
1	0	/TEND1,TxS,CKS
1	1	/HRxRDY,//HTxRDY,HINTR

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is 0, then the Z80182/Z8L182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is 1, then Z80182/Z8L182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182/Z8L182 Mode 0 is always selected as shown in Table 3.

Table 3. Mode 0 and Mode 1 Multiplexed Pins

Z80182/Z8L182 Mode 0	Z80182/Z8L182 Mode 1
TxDB	/HDDIS
RxDB	HA1
/TRxCB	HA0
/RTxCB	HA2
/SYNCB	/HCS
/CTSB	/HWR
/DCDB	/HRD
PA7-PA0	HD7-HD0

Table 5. Primary, Secondary and Tertiary Pin Functions

Pin Number VQFP	Pin Number QFP	1st Function	2nd Function	3rd Function	MUX Control
1	4	ST			
2	5	A0			
3	6	A1			
4	7	A2			
5	8	A3			
6	9	A4			
7	10	A5			
8	11	A6			
9	12	A7			
10	13	A8			
11	14	A9			
12	15	A10			
13	16	A11			
14	17	A12			
15	18	V_{SS}			
16	19	A13			
17	20	A14			
18	21	A15			
19	22	A16			
20	23	A17			
21	24	A18/T_{OUT}			
22	25	V_{DD}			
23	26	A19			
24	27	D0			
25	28	D1			
26	29	D2			
27	30	D3			
28	31	D4			
29	32	D5			
30	33	D6			
31	34	D7			
32	35	/RTS0	PB0		SYS CONF REG Bit 5
33	36	/CTS0	PB1		SYS CONF REG Bit 5
34	37	/DCD0	PB2		SYS CONF REG Bit 5
35	38	TxA0	PB3		SYS CONF REG Bit 5
36	39	RxA0	PB4		SYS CONF REG Bit 5
37	40	TxA1	PB5		SYS CONF REG Bit 6
38	41	RxA1	PB6		SYS CONF REG Bit 6
39	42	RxS//CTS1	PB7		SYS CONF REG Bit 6
40	43	CKA0//DREQ0			

16550 MIMIC INTERFACE FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has a 16550 MIMIC interface that allows it to mimic the 16550 device. It has all the interface pins necessary to connect to the PC/XT/AT bus. It contains the complete register set of the part with the same interrupt structure. The data path allows parallel transfer of data to and from the register set by the internal Z80180 of the Z80182/Z8L182. There is no shift register associated with the mimic of the 16550 UART. This interface saves the application from doing a serial transfer before performing data compression or error correction on the data.

Control of the register set is maintained by six priority encoded interrupts to the Z80182/Z8L182. When the PC/XT/AT writes to THR, MCR, LCR, DLL, DLM, FCR or reads the RBR, an interrupt to the Z80182/Z8L182 is generated. Each interrupt can be individually masked off or all interrupts can be disabled by writing a single bit. Both mode 0 and mode 2 interrupts are supported by the 16550 MIMIC interface.

Two eight-bit timers are also available to control the data transfer rate of the 16550 MIMIC interface. Their input is tied to the ESCC channel B divide clock, so a down count of 24 bits is possible. An additional two eight bit timers are available for programming the FIFO timeout feature (Four Character Time Emulation) for both Receive and Transmit FIFO's.

The 16550 MIMIC interface supports the PC/XT/AT interrupt structure as well as an additional mode that allows for a wired Logic AND interrupt structure.

The 16550 MIMIC interface is also capable of high speed parallel DMA transfers by using two control lines and the transmit and receive registers of the 16550 MIMIC interface.

All registers of the 16550 MIMIC interface are accessible in any page of I/O space since only the lowest eight address lines are decoded. See Figure 6 for a block diagram of the 16550 MIMIC interface.

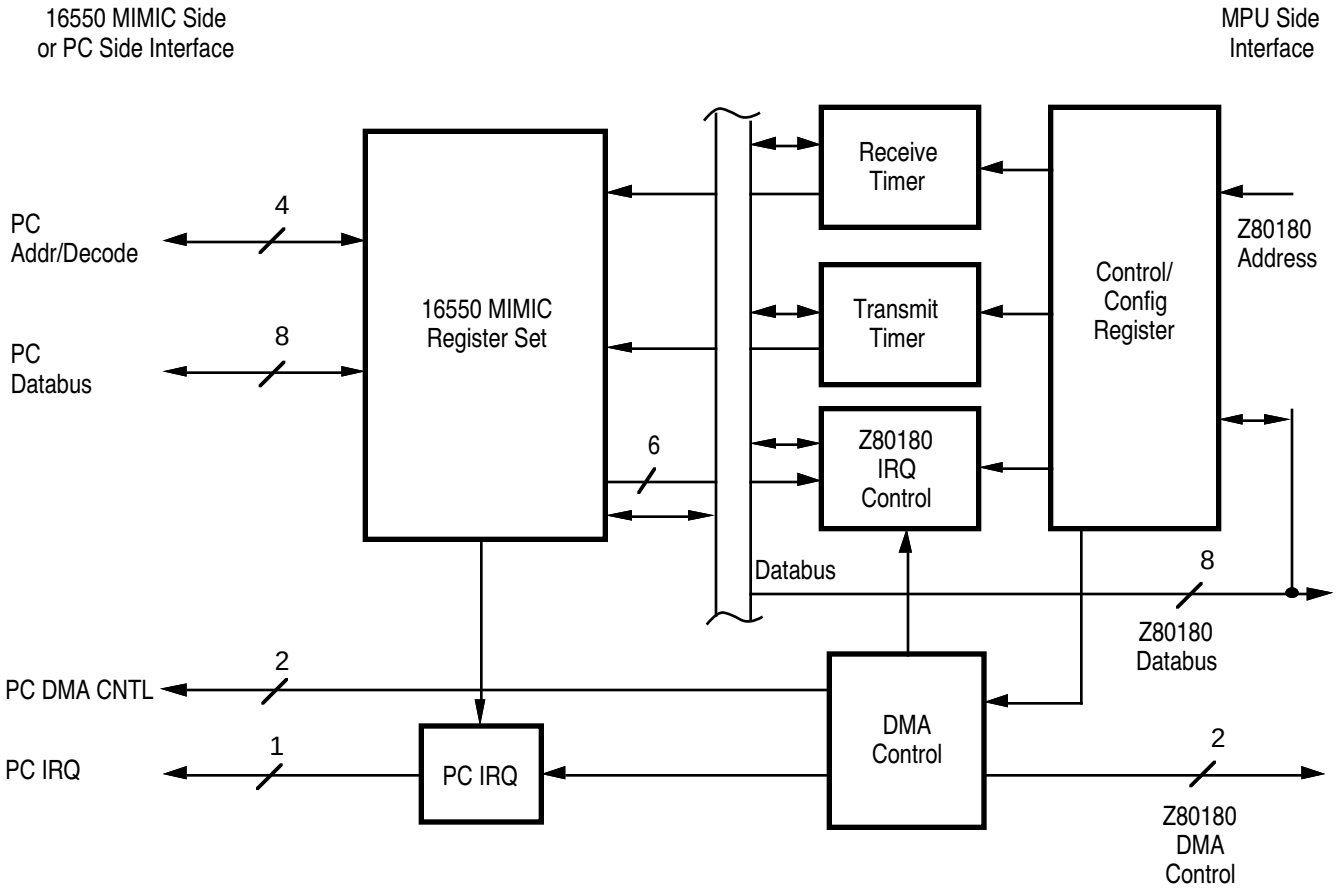


Figure 6. 16550 MIMIC Block Diagram

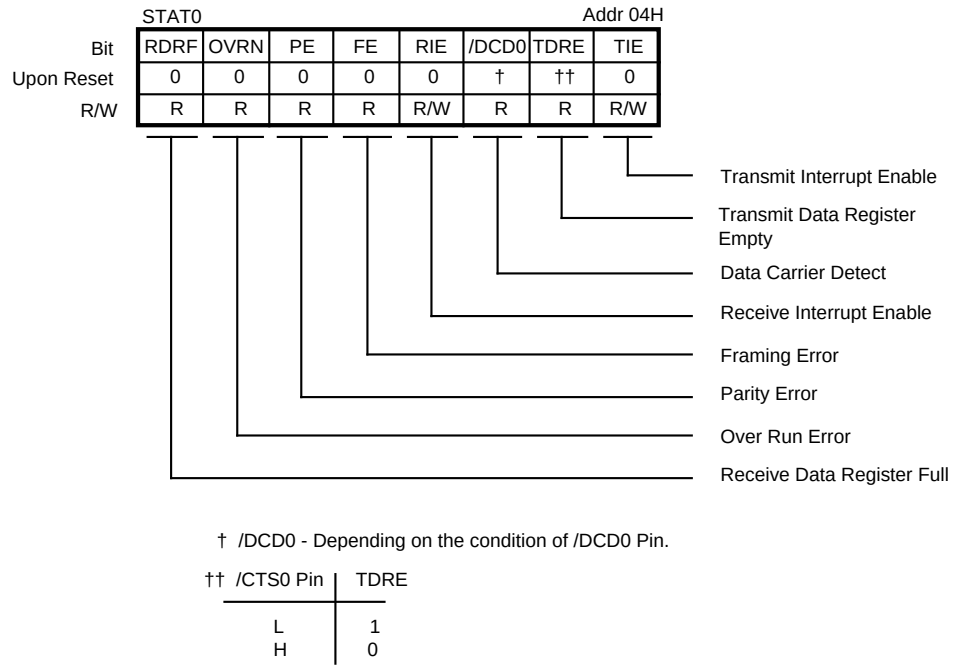


Figure 13. ASCI Status Register

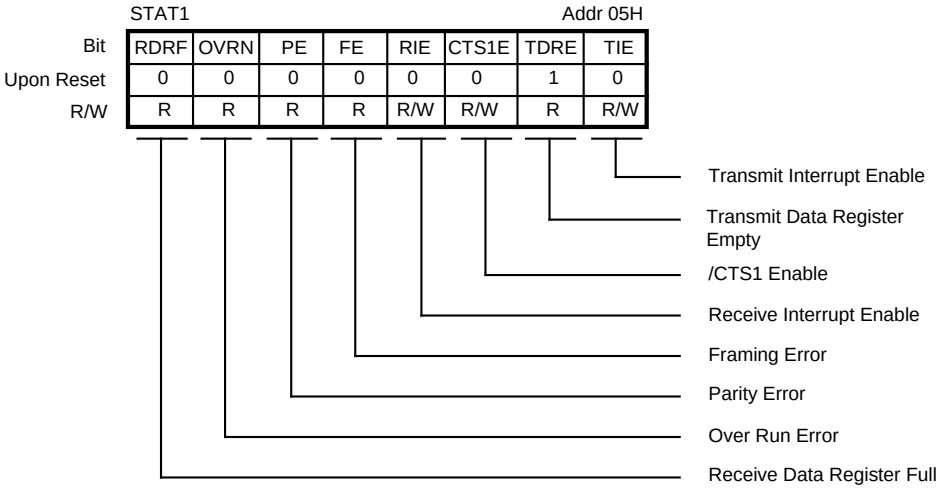


Figure 14. ASCI Status Register (Ch. 1)

MMU REGISTERS

CBR — Addr 38H

Bit	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Common Base Register

Figure 43. MMU Common Base Register

BBR — Addr 39H

Bit	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
Upon Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Bank Base Register

Figure 44. MMU Bank Base Register

CBAR — Addr 3AH

Bit	CA3	CA2	CA1	CA0	BA3	BA2	BA1	BA0
Upon Reset	1	1	1	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

MMU Bank Area Register

MMU Common Area Register

Figure 45. MMU Common/Bank Area Register

CPU Control Register

Bit 7. *Clock Divide Select.* Bit 7 of the CCR allows the programmer to set the internal clock to divide the external clock by 2 if the bit is 0 and divide-by-one if the bit is 1. Upon reset, this bit is set to 0 and the part is in divide-by-two mode. Since the on-board oscillator is not guaranteed to operate above 20 MHz, an external source must be used to achieve the maximum 33 MHz operation of the part, i.e., an external clock at 66 MHz with 50% duty cycle.

If an external oscillator is used in divide-by-one mode, the minimum pulse width requirement must be satisfied.

Bits 6 and 3. *STANDBY/IDLE Enable.* These two bits are used for enabling/disabling the IDLE and STANDBY mode.

Setting D6, D3 to 0 and 1, respectively, enables the IDLE mode. In the IDLE mode, the clock oscillator is kept oscillating but the clock to the rest of the internal circuit, including the CLKOUT, is stopped. The Z8S180 enters IDLE mode after fetching the second opcode of a SLEEP instruction, if the I/O STOP bit is set.

Setting D6, D3 to 1 and 0, respectively, enables the STANDBY mode. In the STANDBY mode, the clock oscillator is stopped completely. The Z8S180 enters STANDBY after fetching the second opcode of a SLEEP instruction, if the I/O STOP bit is set.

Setting D6, D3 to 1 and 1, respectively, enables the STANDBY-QUICK RECOVERY mode. In this mode, its operations are identical to STANDBY except that the clock recovery is reduced to 64 clock cycles after the exit conditions are gathered. Similarly, in STANDBY mode, the Z8S180 enters STANDBY after fetching the second opcode of a SLEEP instruction, if the I/O STOP bit is set.

Bit 5. *BREXT.* This bit controls the ability of the Z8S180 to honor a bus request during STANDBY mode. If this bit is set to 1 and the part is in STANDBY mode, a BUSREQ is honored after the clock stabilization timer is timed out.

Bit 4. *LNPHI.* This bit controls the drive capability on the PHI Clock output. If this bit is set to 1, the PHI Clock output is reduced to 25% of its drive capability.

Bit 2. Reserved

Bit 1. *LNCPUCTL.* This bit controls the drive capability of the CPU Control pins. When this bit is set to 1, the output drive capability of the following pins is reduced to 25% of the original drive capability:

- /BUSACK
- /RD
- /WR
- /M1
- E
- /MREQ
- /IORQ
- /RFSH
- /HALT
- /TEND1

Bit 0. *LNAD/DATA.* This bit controls the drive capability of the Address/Data bus output drivers. If this bit is set to 1, the output drive capability of the Address and Data bus output is reduced to 25% of its original drive capability.

Z85230 ESCC™ CONTROL REGISTERS

See Figures 52 and 53 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification /Technical Manual.

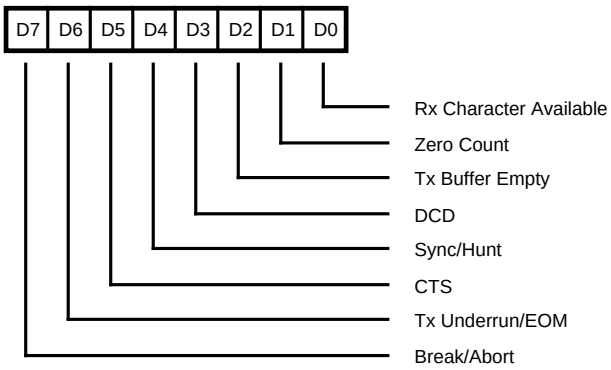
The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. ***It is recommended that /TRxCB be programmed as an output with proper baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.***

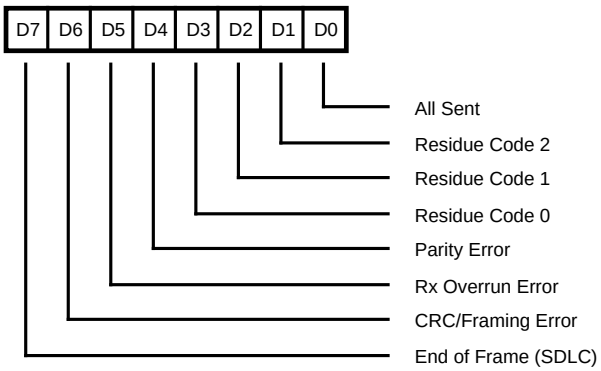
Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

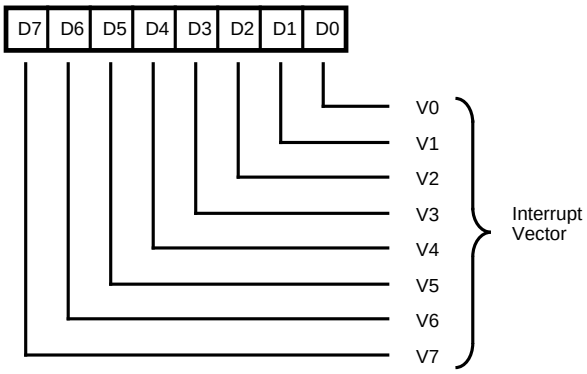
Read Register 0



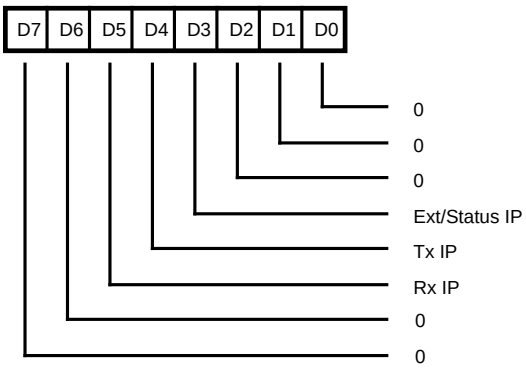
Read Register 1



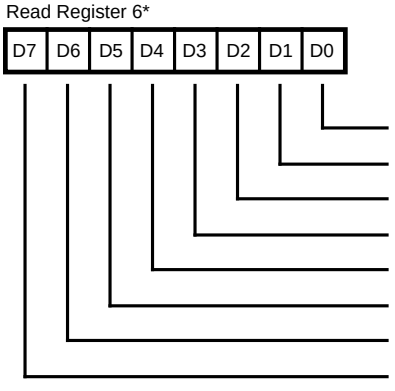
Read Register 2



Read Register 3



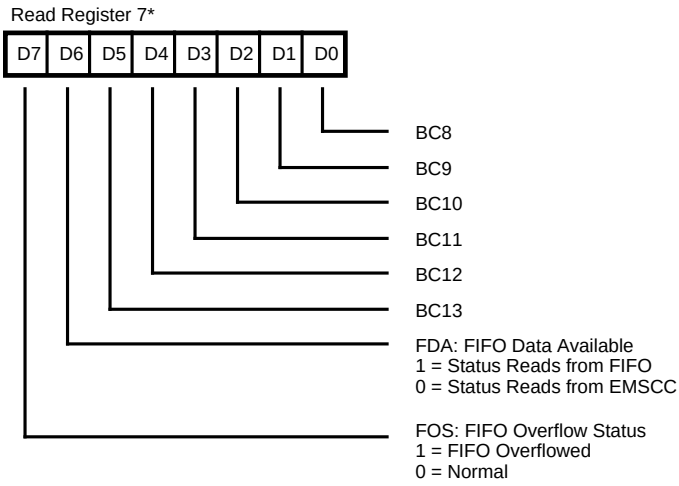
Read Register 6*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Read Register 7*



*Can only be accessed if the SDLC FIFO enhancement is enabled (WR15 bit D2 set to 1)

SDLC FIFO Status and Byte Count (LSB)

Figure 52. Write Register Bit Functions (Continued)

Bit 0 16450 MIMIC Mode Enable
(Reset value=0) This bit = 1 will force the mimic into 16450 mode. Bit 0 in the FCR reg is forced to zero as well as the mimic internal FIFO enable. When used, this bit should be programmed at MIMIC initialization and not modified afterwards.

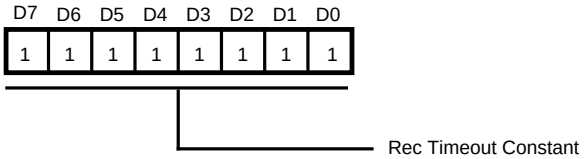


Figure 65. Receive Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEAH)

This register contains an 8-bit constant for emulation of the 16550 four character timeout feature. Software must determine the value to load into this register based on the bit rate and word length specified by the MIMIC interface with the PC. This timer receives its input from the /TRxCB Clock of the ESCC. This timer is enabled to down count when the enable bit in the FSR register is set and the trigger level interrupt has not been activated on the RCVR FIFO. The counter reloads and counts down each time there is a read or write to the RCVR FIFO.

The receive timeout timer is enhanced to emulate the actual 16550 when bit 1 of the FIFO status and control register is enabled. Under most circumstances, this register should be programmed for four character timers (40d, 8-N-1).

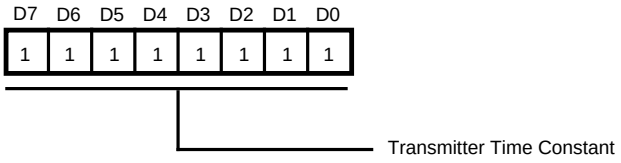


Figure 66. Transmit Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEBH)

This register contains an 8-bit constant for determining the interval for the Transmit Timeout Timer. If allowed to decrement to zero, this timer interrupts the MPU by setting the THR bit in the IUS/IP register. This timer receives its input from the /TRxCB Clock of the SCC. The timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the XMIT FIFO. The counter reloads each time there is a read or write to the XMIT FIFO.

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z180™ MPU and the PC/XT/AT, two timers have been added to alleviate any software problems that a high speed parallel data transfer might cause. These timers allow the programmer to slow down the data transfer just as if the 16550 MIMIC interface had to shift the data in and out serially. The Timers receive their input from the /TRxCB Clock since, in 16550 MIMIC mode, the ESCC channel B is disabled. For example, the clock source for the 8-bit registers: RTTC (Receive Timeout Time Constant, xxEAH), TTTC (Transmit Timeout Time Constant, xxEBH), TTCR (Transmit Time Constant Register, xxFAH) and RTCR (Receive Time Constant Register, xxFBH) uses the /TRxCB Clock output. The /TRxCB Clock output needs to be generated by the ESCC's channel B's 16-bit BRG as its clock source, thus allowing the programmer to access a total of 24 bits as a timer to slow down the data transfer.

In most cases, ESCC Ch. B BRG should be programmed to output at a frequency equivalent to the desired serial transfer rate. The output of the BRG should be routed to the /TRxCB pin.

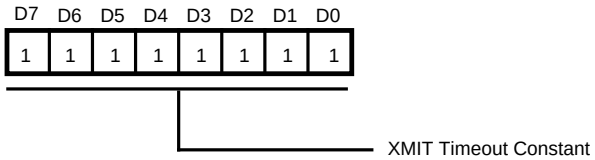


Figure 67. Transmitter Time Constant Register
(Z180 MPU Read/Write, Address xxFAH)

Transmit And Receive Timers (Continued)

When a write from the PC/XT/AT is made to the Transmit Holding Register, an interrupt to the Z180 MPU is generated. The Z180 MPU then reads the data in the Transmit Holding Register. Upon this read, if the Transmitter timer is enabled, the time constant from the Transmitter Time Constant Register is loaded into the Transmitter timer and enables the count. After the timer reaches a count of zero the Transmit Holding Register Empty bit is set. However, the above is only true when the PC/XT/AT is reading the Transmit Holding Register Empty bit. To allow the Z180 MPU to know that it has already read the byte of data, immediately following a read from the Transmit Holding Register, a mirrored Transmit Holding Register, Empty bit is set. This mirrored bit is always read back to the Z180 MPU when it reads the Line Status Register.

If the transmitter timer is not enabled when the Z180 MPU reads the Transmit Holding Register, both Transmit Holding Register Empty bits are set immediately. In FIFO mode of operation, the effect is similar as the status to PC is always delayed such that a PC interrupt for empty FIFO will not occur before the time required for each character read from the FIFO by the Z180 has elapsed. The effect is that the PC will not see data requests from an empty FIFO any faster than would occur with a true UART when the delay feature is enabled. This timer is also used to delay data transfer for TSR buffer to Z80182 THR in double buffer mode.

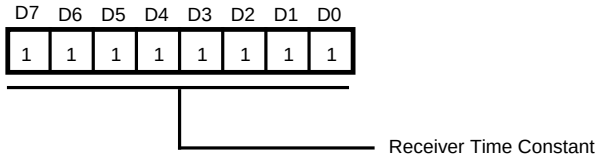


Figure 68. Receive Time Constant Register
(Z180 MPU Read/Write, Address xxFBH)

When the Z180™ MPU writes to the Receive Buffer register and the Receive Timer is enabled, the Receive Timer is loaded with the Receive Time Constant, the timer is enabled and counts down to zero. When the timer reaches zero, the Data Ready bit in the Line Status Register is set. As with the Transmit Timer, the Data Ready bit is also mirrored. Immediately upon a write to the Receive Buffer, the mirrored bit is set to let the Z180 MPU know that the byte has already been written. If the timer is not enabled, then both Data Ready bits are set immediately upon a write to the Receive Buffer. The FIFO mode of operation is similar in that the status to the PC is always delayed by the time required for each character written to the FIFO by the Z180. The effect is that the PC will not see a FIFO trigger level or DMA request faster than would occur with a true UART when the delay feature is enabled.

16550 MIMIC REGISTERS (Continued)

Line Status Register

Bit 7 Error in RCVR FIFO
In 16450 mode, this bit will read logic 0. In 16550 mode this bit is set if at least one data byte is available in the FIFO with one of its associated error bits set. This bit will clear when there are no more errors (or break detects) in the FIFO.

Bit 6 Transmitter Empty
This bit must be set or reset by the MPU by a write to this register bit. If Double Buffer Mode is enabled, the TEMT bit is set/reset automatically. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 5 Transmit Holding Register Empty, THRE
This bit is set to 1 when either the THR has been read (emptied) by the MPU (16450 mode) or the XMIT FIFO is empty (16550 mode). This bit is set to 0 when either the THR or XMIT FIFO become non-empty. A shadow bit exists so that the register bit setting to 1 is delayed by the Transmitter Timer if enabled. The MPU when reading this bit will not see the delay. Both shadow and register bits are cleared when the PC writes to the THR of XMIT FIFO. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 2, 3, 4 Parity Error, Framing Error, Break Detect
These bits are written, indirectly, by the MPU as follows: The bits are first written to shadow bit locations when the MPU write accesses the LSR. When the next character is written to the Receive Buffer or RCVR FIFO, the data in the shadow bits is then copied to the LSR (16450 mode) or FIFO RAM (16550 mode). In FIFO mode bits become available to the PC when the data byte associated with the bits is next to be read (top of FIFO). In FIFO mode, with successive reads of the receiver, the status bits will be set if an error occurs on any byte. Once the MPU writes to the Receive Buffer or RCVR FIFO, the shadow bits are auto cleared. The register bits are cleared upon the PC reading the LSR. In FIFO mode these bits will be set if any byte has the respective error bit set while the PC reads multiple characters from the FIFO.

Bit 1 Overrun Error
This bit is set if the Z180 MPU makes a second write to the Receive Buffer before the PC reads the data in the Buffer (16450 mode) or with a full RCVR FIFO (16550 mode.) No data will be transferred to the RCVR FIFO under these circumstances. This bit is reset when the PC reads the Line Status Register.

Bit 0 Data Ready
This bit is set to 1 when received data is available, either in the RCVR FIFO (16550 mode) or Receive Buffer Register (16450 mode). This bit is set immediately upon the MPU writing data to the Receive Buffer or FIFO if the Receive Timer is not enabled but is delayed by the timer interval if the Receive Timer is enabled. For MPU read access a shadow bit exists so that the MPU does not see the delay the PC does. Both bits are cleared to logic zero immediately upon reading all the data in either the Receive Buffer or FIFO.

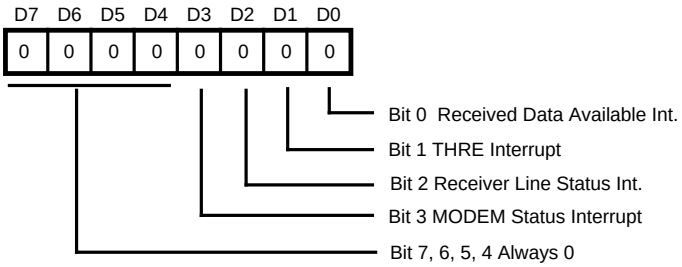


Figure 75. Interrupt Enable Register
(PC Read/Write, Address 01H)
(Z180 MPU Read Only, Address xxF1H)

Interrupt Enable Register

Bits 7, 6, 5, 4 Reserved
These bits will always read 0 (PC and MPU).

Bit 3 Modem Status IRQ
If bits 0, 1, 2 or 3 of the Modem Status Register are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 2 Receive Line Status IRQ
If bits 1, 2, 3 or 4 of the LSR are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 1 Transmit Holding Register Empty IRQ
If bit 5 of the LSR is set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 0 Received Data Available IRQ
If bit 0 of the LSR is set or a Receive Timeout occurs and this enable bit is a logic 1, then an interrupt to the PC is generated.

EMULATION MODES (Continued)

Table 21. Emulation Mode 1

Signal	Normal Mode 0	Emulation Adaptor Mode 1
PHI	Output	Input
/M1	Output	Input
/MREQ,/MRD	Output	Input
/IORQ	Output	Input
/RD	Output	Input
/WR	Output	Input
/RFSH	Output	Input
/HALT	Output	Input
ST	Output	Input
E	Output	Tri-state
/BUSACK	Output	Input
/WAIT	Input	Output
A19,A18/T_{OUT}	Output	Input
A17-A0	Output	Input
D7-D0	Input/Output	Input/Output
TxA0	Output	Tri-state
/RTS0	Output	Tri-state
TxA1	Output	Tri-state
/INT0	Input	Output, Open-Drain

Mode 2 Emulation Probe Mode
In the Emulator Probe Mode all of the Z182 output signals are tri-state. This scheme allows a Z182 emulator probe to grab on to the Z182 package leads on the target system.

Mode 3 RESERVED (for test purposes only)
This mode is reserved for test purpose only, do not use.

Notes:
Z182 has two branches of reset. /RESET controls the Z182 overall configuration, RAM and ROM boundaries, plus the ESCC, Port and the 16550 MIMIC interface. In Normal Mode, a "one shot" circuit samples the input of the /RESET pin to assert the internal reset to its proper duration. In Adapter Mode, this "one shot" circuit is bypassed. Note also that the Z180's crystal oscillator is disabled in Mode 1 and Mode 2.

In Mode 1 the emulator must provide /MREQ on the (/MREQ,/MRD) Z80182/Z8L182 pin (not /MRD); and A18 (not T_{OUT}) on the A18/T_{OUT} pin.

SLEEP, HALT EFFECT ON MIMIC AND 182 SIGNALS

The following Z80182/Z8L182 signals are driven High when Z180™ MPU enters a SLEEP or HALT state:

- /MRD when selected in the Interrupt Edge/Pin MUX Register.
- /MWR when selected in the Interrupt Edge/Pin MUX Register.
- /ROMCS,/RAMCS always High in SLEEP or HALT.

The following signals are High-Z during SLEEP and HALT:

- /IOCS when so selected in the Interrupt Edge/Pin MUX Register.
- /RD and /WR.

A0-A19 (A18 if selected) always High-Z in power down.

D0-D7 always High-Z in power down modes.

The MIMIC logic of the 182 is disabled during power down modes of the Z180.

TIMING DIAGRAMS (Continued)

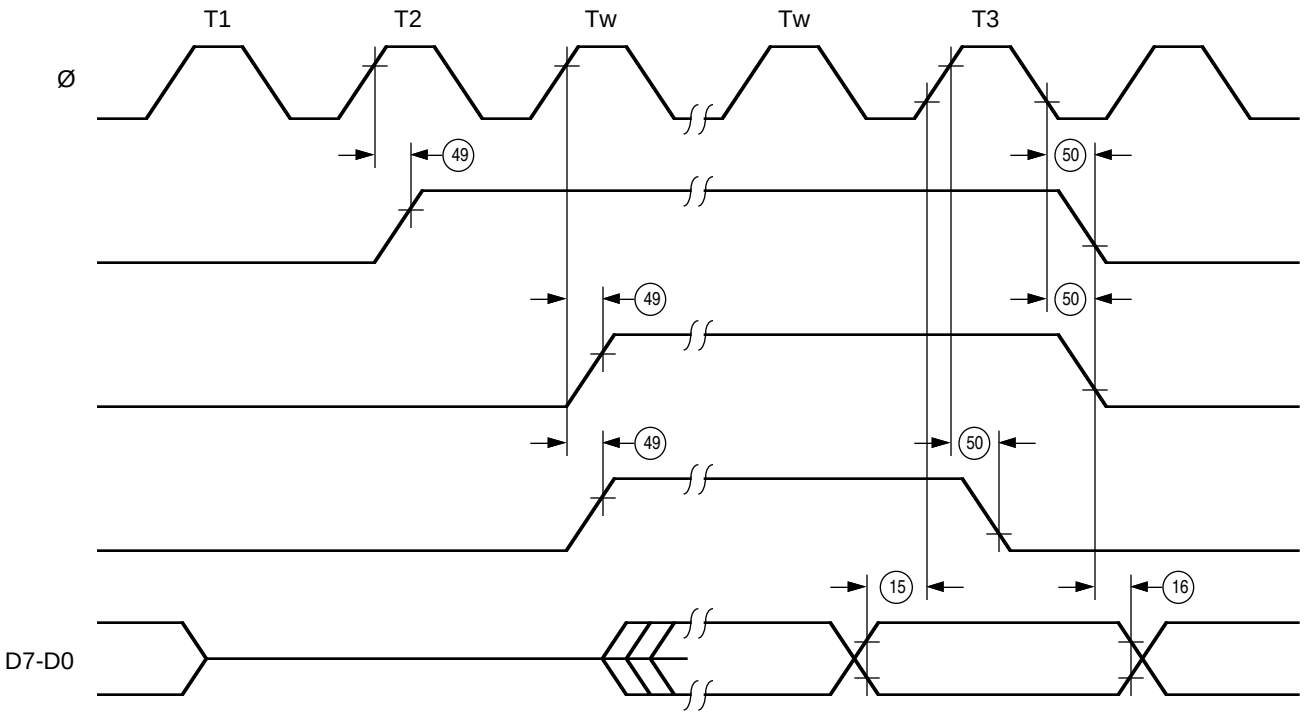


Figure 94. E Clock Timing
(Memory Read/Write Cycle
I/O Read/Write Cycle)

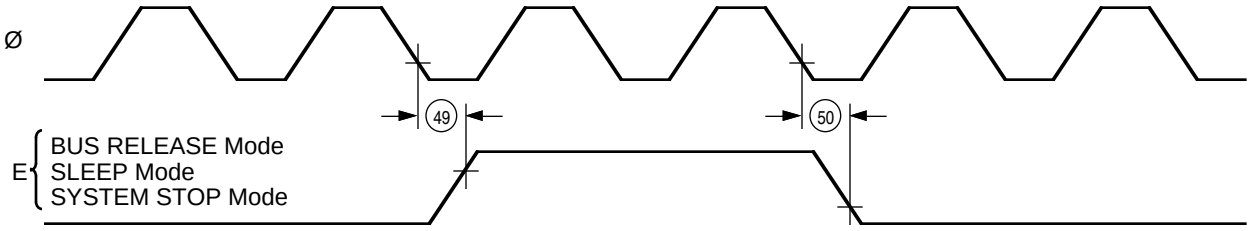


Figure 95. E Clock Timing

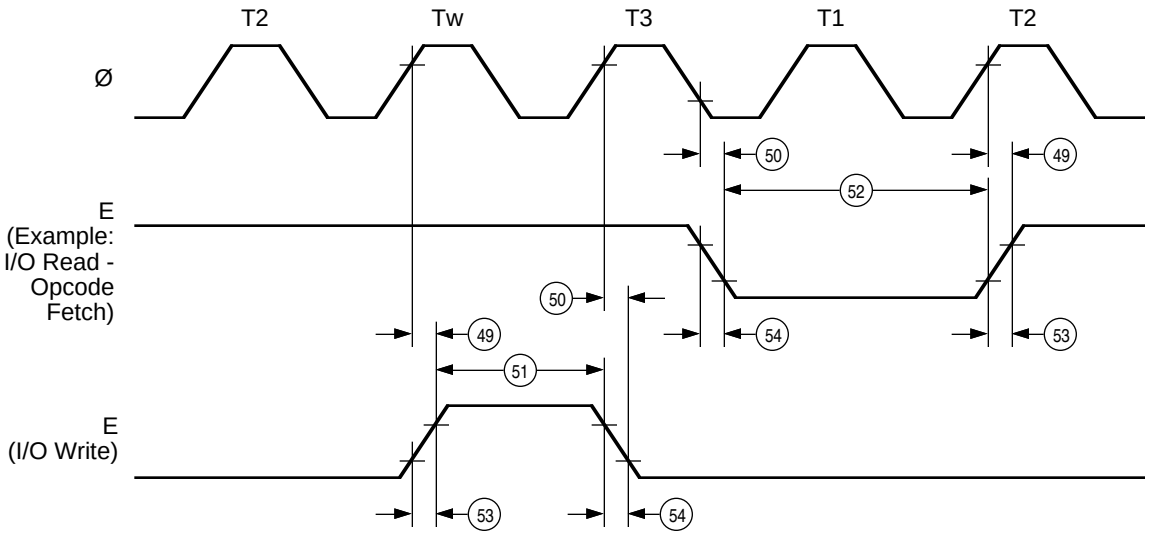


Figure 96. E Clock Timing
(Minimum timing example
of PWEL and PWEH)

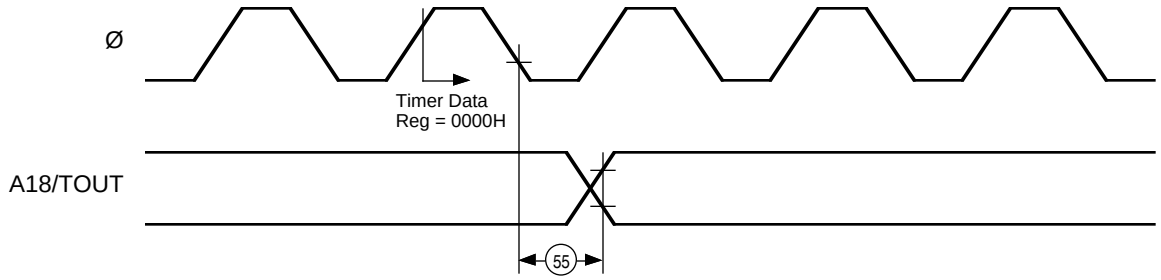


Figure 97. Timer Output Timing

TIMING DIAGRAMS (Continued)

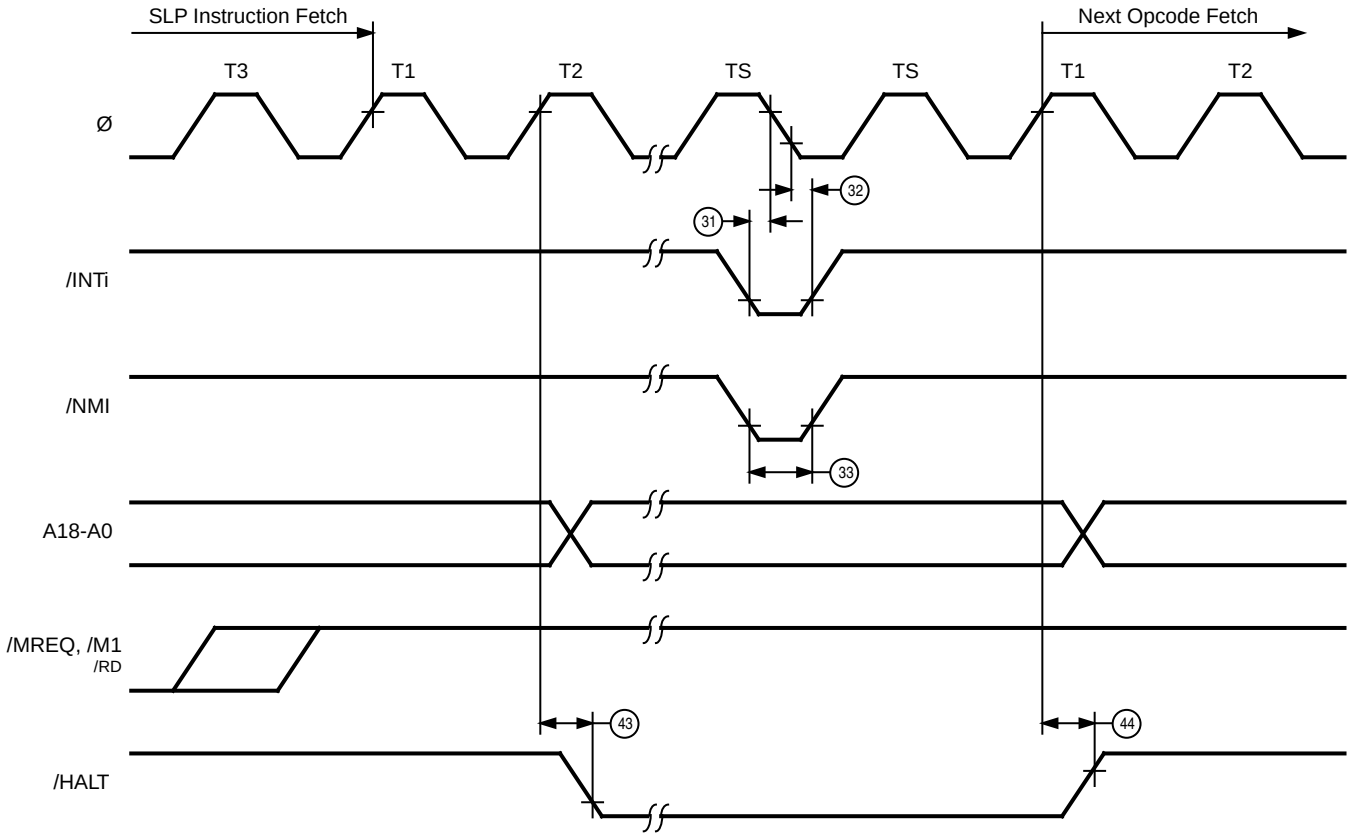


Figure 98. SLEEP Execution Cycle

ESCC Timing

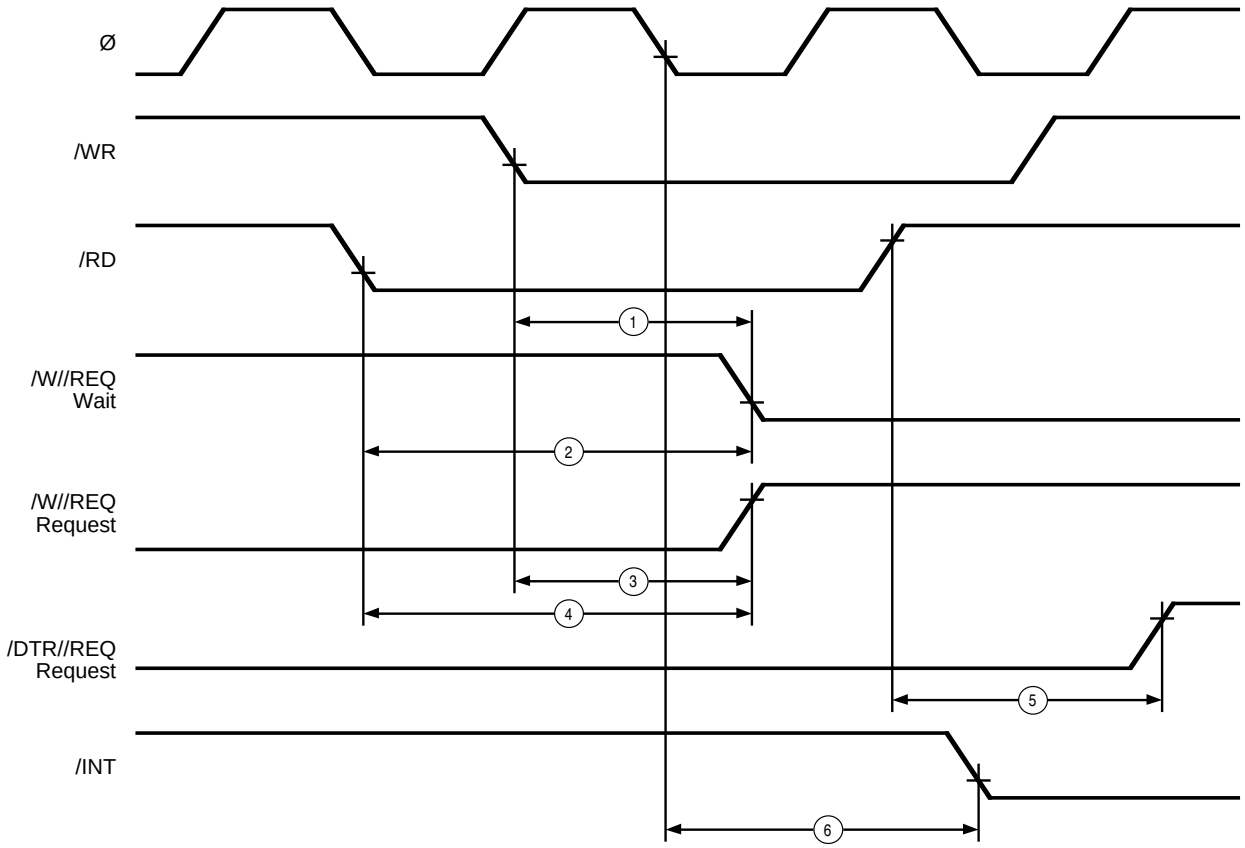


Figure 104. ESCC AC Parameter

Table B. ESCC Timing Parameters

No.	Symbol	Parameter	20 MHz Min	20 MHz Max	Unit
1	TdWR(W)	/WR Fall to Wait Valid Delay		50	ns
2	TdRD(W)	/RD Fall to Wait Valid Delay		50	
3	TdWRf(REQ)	/WR Fall to /W//REQ Not Valid Delay		65	
4	TdRDf(REQ)	/RD Fall to /W//REQ Not Valid Delay		65	
5	TdRdr(REQ)	/RD Rise to /DTR//REQ Not Valid Delay		TBD	
6	TdPC(INT)	Clock to /INT Valid Delay		160	

AC CHARACTERISTICS (Continued)

Z85230 General Timing Diagram

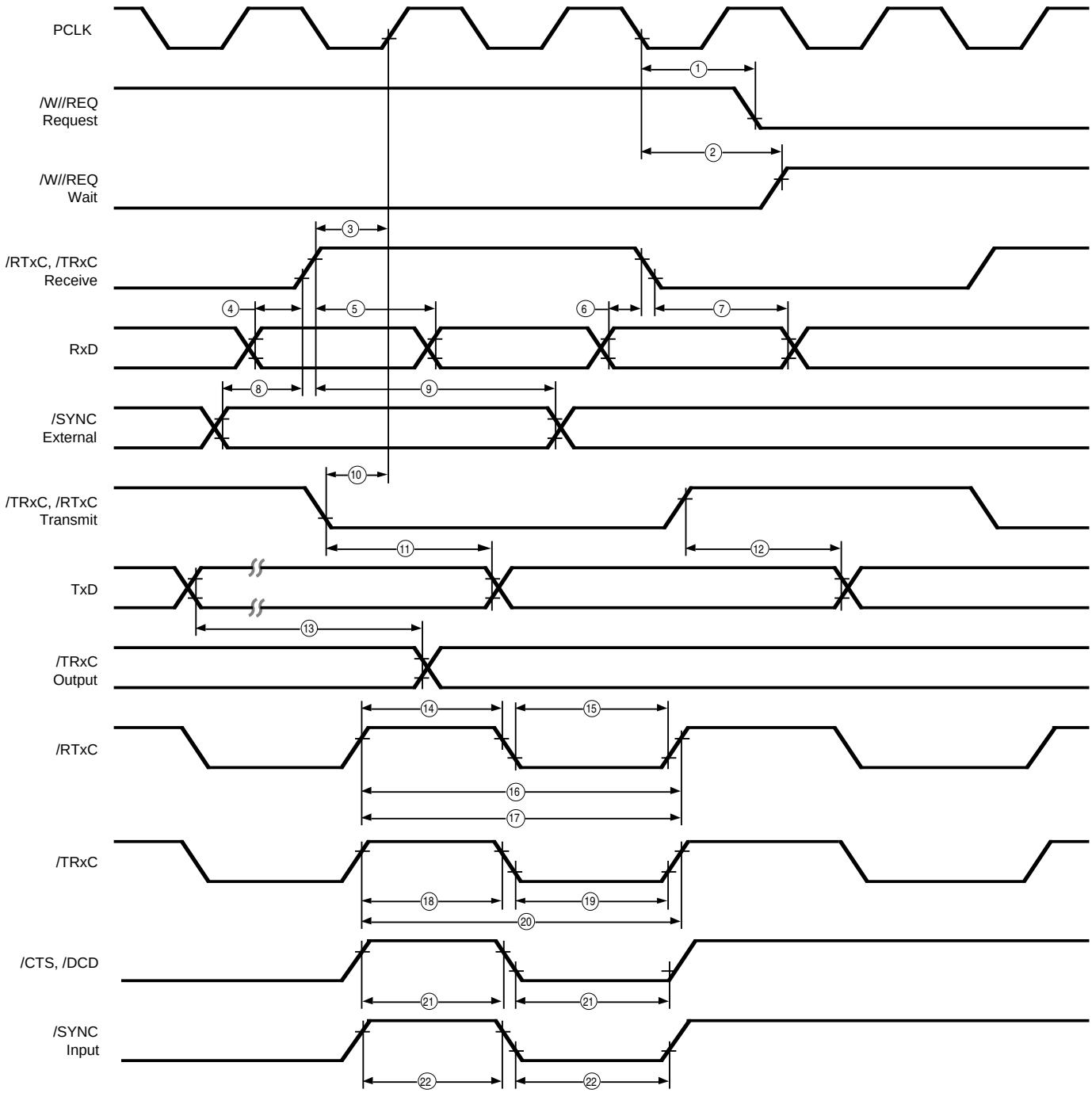


Figure 105. General Timing Diagram

16550 MIMIC TIMING (Continued)

Table K. Interrupt Timing RCVR FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
14	tSINT	Delay from Stop to Set Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles
15	tRINT	Delay from /HRD (RD RBR or RD LSR) to Reset Interrupt		2 MPU Clock Cycles		2 MPU Clock Cycles

Note:
These AC parameter values are preliminary and are subject to change without notice.

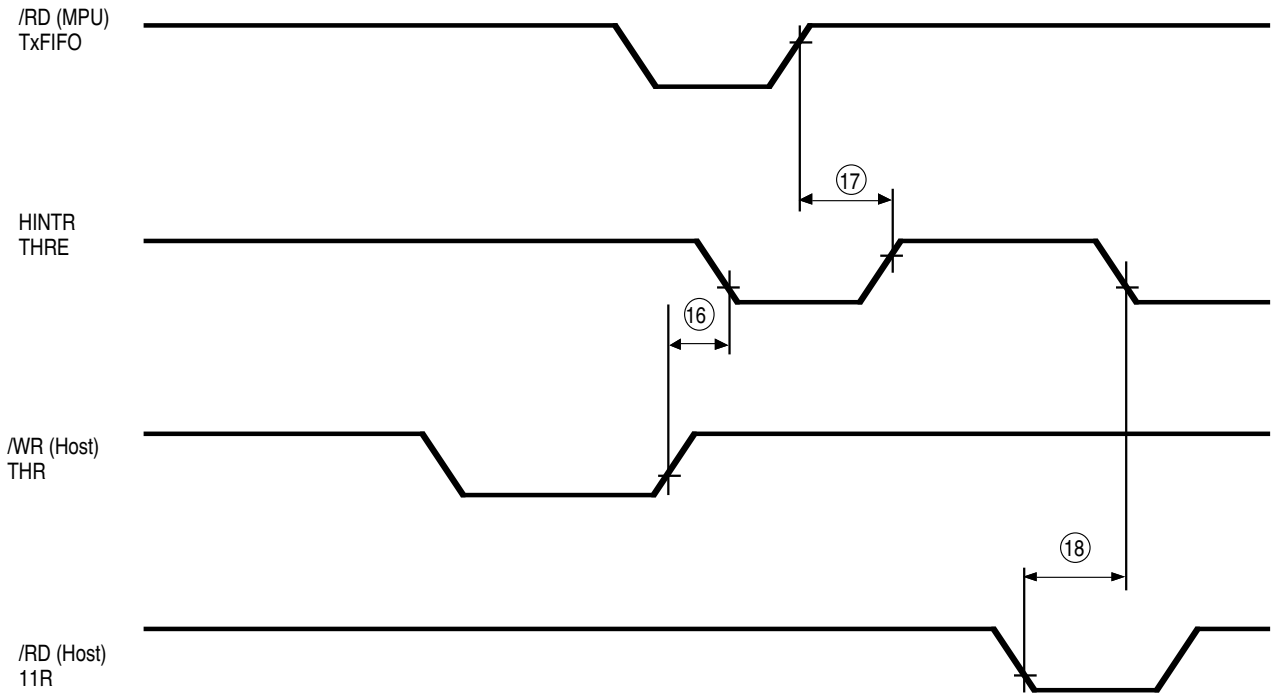


Figure 115. Interrupt Timing Transmitter FIFO

Table L. Interrupt Timing Transmitter FIFO

No.	Sym	Parameter	Z8L182 20 MHz Min	Z8L182 20 MHz Max	Z80182 33 MHz Min	Z80182 33 MHz Max
16	tHR	Delay from /WR (WR THR) to Reset Interrupt		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles
17	TSTI	Delay from Stop to Interrupt (THRE)	2 MPU Clock Cycles		2 MPU Clock Cycles	
18	TIR	Delay from /RD (RD IIR) to Reset Interrupt (THRIE)		75		75

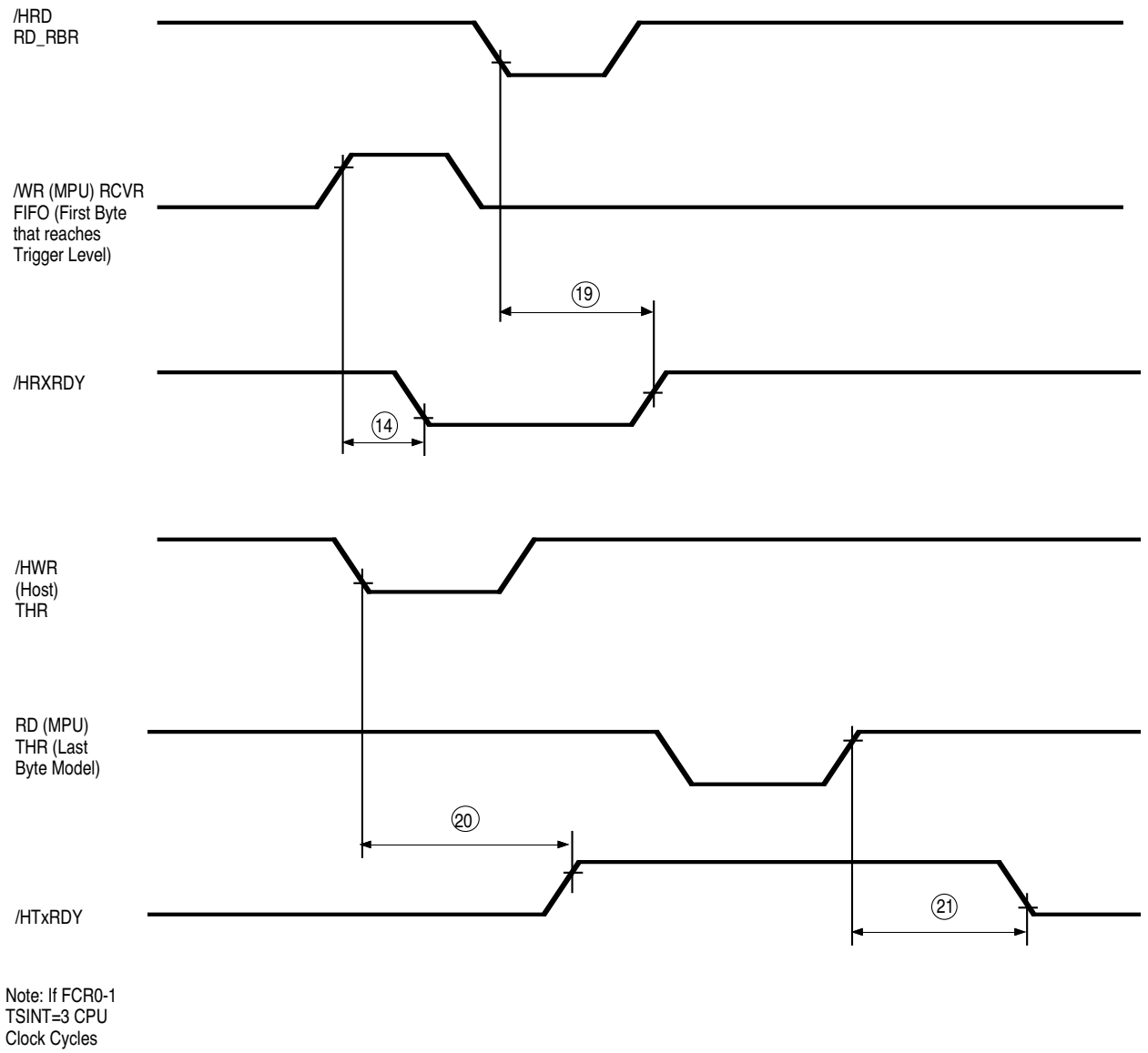


Figure 116 RCVR FIFO Bytes Other Than First

ORDERING INFORMATION

Z8L182	Z80182
20 MHz	**33 MHz**
Z8L18220ASC	Z8018233ASC
Z8L18220FSC	Z8018233FSC

For fast results, contact your local Zilog sales office for assistance in ordering the part(s) desired.

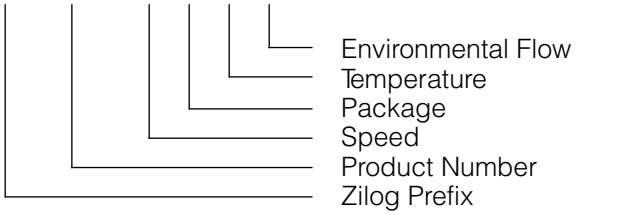
Preferred Package
A = VQFP (Very Small QFP)
F = Plastic Quad Flatpack

Preferred Temperature
S = 0°C to +70°C

Speeds
20 = 20 MHz
33 = 33 MHZ

Environmental
C = Plastic Standard
D = Plastic Stressed
E = Hermetric Standard

Example:
Z 80182 20 F S C is a Z80182, 20 MHz, QFP, 0°C to +70°C, Plastic Standard Flow



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