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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l18220asc

Z180 MPU DMA SIGNALS

/TEND0. *Transfer End 0 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND0 is multiplexed with CKA1 on the CKA1//TEND0 pin.

/TEND1. *Transfer End 1 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND1 is multiplexed with the ESCC signal /RTSB and the 16550 MIMIC interface signal /HRxRDY on the /TEND1//RTSB//HRxRDY pin.

/DREQ0. *DMA request 0 (input, active Low).* /DREQ0 is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. /DREQ0 is multiplexed with CKA0 on the CKA0//DREQ0 pin.

/DREQ1. *DMA request 1 (input, active Low).* /DREQ1 is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

Z180™ MPU TIMER SIGNALS

T_{OUT}. *Timer Out (output, active High).* T_{OUT} is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/T_{OUT} pin.

Z85230 ESCC™ SIGNALS

TxDA. *Transmit Data (output, active High).* This output signal transmits channel A's serial data at standard TTL levels. This output can be tri-stated during power down modes.

TxDB. *Transmit Data (output, active High).* This output signal transmits channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface /HDDIS signal on the TxDB//HDDIS pin.

RxDA. *Receive Data (inputs, active High).* These inputs receive channel A's serial data at standard TTL levels.

RxDB. *Receive Data (input, active High).* These inputs receive channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB//HA1 pin.

/TRxCA. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel A program control. /TRxCA may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/TRxCB. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel B program

control. /TRxCB may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in output mode. In Z80182/Z8L182 mode 1 /TRxCB is multiplexed with the 16550 MIMIC interface HA0 input on the /TRxCB//HA0 pin.

/RTxCA. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel A program control. In channel A, /RTxCA may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCA pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

/RTxCB. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel B program control. In channel B, /RTxCB may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCB pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182/Z8L182 mode 1 the /RTxCB signal is multiplexed with 16550 MIMIC interface HA2 input on the /RTxCB//HA2 pin.

/W//REQB. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This pin is similar in functionality to /W//REQA but is applicable on

channel B. The /W//REQB signal is multiplexed with the Z180 MPU CKS signal and the 16550 MIMIC interface /HTxRDY signal on the CKS//W//REQB//HTxRDY pin.

16550 MIMIC INTERFACE SIGNALS

HD7-HD0. *Host Data Bus (input/output, tri-state).* In Z80182/Z8L182 mode 1, the host data bus is used to communicate between the 16550 MIMIC interface and the PC/XT/AT. It is multiplexed with the PA7-PA0 of parallel Port A when the Z80182/Z8L182 is in mode 0.

/HDDIS. *Host Driver Disable (output, active Low).* In Z80182/Z8L182 mode 1, this signal goes Low whenever the PC/XT/AT is reading data from the 16550 MIMIC interface. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC™ TxDB signal on the TxDB//HDDIS pin.

HA2-HA0. *Host Address (input).* In Z80182/Z8L182 mode 1, these pins are the address inputs to the 16550 MIMIC interface. This address determines which register the PC/XT/AT accesses. HA0 is multiplexed with /TRxCB on the /TRxCB/HA0 pin; HA1 is multiplexed with RxDB on the RxDB/HA1 pin; HA2 is multiplexed with /RTxCB on the /RTxCB/HA2 pin.

/HCS. *Host Chip Select (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to select the 16550 MIMIC interface for an access. In Z80182/Z8L182 mode 0, it is multiplexed with the ESCC /SYNCB signal on the SYNCB//HCS pin.

/HWR. *Host Write (Input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a write operation is taking place. In Z80182/Z8L182 mode 0, this input is multiplexed with the ESCC /CTSB signal on the /CTSB//HWR pin.

/HRD. *Host Read (input, active Low).* In Z80182/Z8L182 mode 1, this input is used by the PC/XT/AT to signal the 16550 MIMIC interface that a read operation is taking place. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /DCDB signal on the /DCDB//HRD pin.

HINTR. *Host Interrupt (output, active High).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface to signal the PC/XT/AT that an interrupt is pending. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/DTR//REQB) signal and the Z180 MPU TxS signal on the TxS//DTR//REQB//HINTR pin.

/HTxRDY. *Host Transmit Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC in DMA mode to signal the PC/XT/AT that the Transmit Holding Register is empty. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC (/W//REQB) signal and the Z180 MPU CKS signal on the CKS//W//REQB//HTxRDY pin.

/HRxRDY. *Host Receive Ready (output, active Low).* In Z80182/Z8L182 mode 1, this output is used by the 16550 MIMIC interface in DMA mode to signal the PC/XT/AT that a data byte is ready in the Receive Buffer. In Z80182/Z8L182 mode 0, this pin is multiplexed with the ESCC /RTSB signal and the Z180 MPU /TEND1 signal on the /TEND1/RTSB /HRxRDY pin.

PARALLEL PORTS

PA7-PA0. *Parallel Port A (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Z80182/Z8L182 is operated in mode 0. These pins are multiplexed with the HD7-HD0 when the Z80182/Z8L182 is in mode 1.

PB7-PB0. *Parallel Port B (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis when the Port function is selected in the System Configuration register. The pins are multiplexed with the following Z180 peripheral functions: /RTS0, /CTS0, /DCD0, TxA0, RxA0, TxA1, RxA1, (RxS//CTS1).

PC7-PC0. *Parallel Port C (input/output).* These lines can be configured as inputs or outputs on a bit-by-bit basis for bits PC5-PC0. Bits PC7 and PC6 are input only and read the level of the external /INT2 and /INT1 pins. When /INT2 and/or /INT1 are in edge capture mode, writing a 1 to the respective PC7, PC6 bit clears the interrupt capture latch; writing a 0 has no effect. Bits PC5-PC0 are multiplexed with the following pins from ESCC channel A: (/W//REQA), /SYNCA, (/DTR//REQA), /RTSA, /MWR, /CTSA, /DCDA. The Port function is selected through a bit in the System Configuration Register.

EMULATION SIGNALS

EV1, EV2. *Emulation Select (input).* These two pins determine the emulation mode of the Z180 MPU (Table 1).

Table 1. Evaluation Modes

Mode	EV2	EV1	Description
0	0	0	Normal mode, on-chip Z180 bus master
1	0	1	Emulation Adapter Mode
2	1	0	Emulator Probe Mode
3	1	1	Reserved for Test

SYSTEM CONTROL SIGNALS

ST. *Status (output, active High).* This signal is used with the /M1 and /HALT output to decode the status of the CPU machine cycle. If unused, this pin should be pulled to V_{DD} .

/RESET. *Reset Signal (input, active Low).* /RESET signal is used for initializing the MPU and other devices in the system. It must be kept in the active state for a period of at least three system clock cycles.

IEI. *Interrupt Enable Signal (input, active High).* IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.

IEO. *Interrupt Enable Output Signal (output, active High).* In the daisy-chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is 1 and the CPU is not servicing an interrupt from the on-chip peripherals. This pin is multiplexed with /IOCS on the /IOCS/IEO pin. The /IOCS function is the default on Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/IOCS. *Auxiliary Chip Select Output Signal (output, active Low).* This pin is multiplexed with /IEO on the /IOCS/IEO pin. /IOCS is an auxiliary chip select that decodes A7, A6, /IORQ, /M1 and effectively decodes the address space xx80H to xxBFH for I/O transactions. A15 through A8 are not decoded so that the chip select is active in all pages of I/O address space. The /IOCS function is the default on the /IOCS/IEO pin after Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/RAMCS. *RAM Chip Select (output, active Low).* Signal used to access RAM based upon the Address and the RAMLBR and RAMUBR registers and /MREQ.

/ROMCS. *ROM Chip Select (output, active Low).* Signal used to access ROM based upon the address and the ROMBR register and /MREQ.

E. *Enable Clock (output, active High).* Synchronous machine cycle clock output during bus transactions.

XTAL. *Crystal (input, active High).* Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

EXTAL. *External Clock/Crystal (input, active High).* Crystal oscillator connections to an external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

PHI. *System Clock (output, active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is reflective of the functional speed of the processor. In clock divide-by-two mode, the PHI frequency is half that of the crystal or input clock. If divide-by-one mode is enabled, the PHI frequency is equivalent to that of crystal or input frequency. The PHI frequency is also fed to the ESCC core. If running over 20 MHz (5V) or 10 MHz (3V) the PHI-ESCC frequency divider should be enabled to divide the PHI clock by two prior to feeding into the ESCC core.

Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 4.

Table 4. Multiplexed Port Pins

Port Mode Function	ASCI/ESCC Mode Function
PB7	RxS,/CTS1
PB6 Select with bit 6=1	RxA1
PB5 System Config Reg.	TxA1
PB4	RxA0
PB3	TxA0
PB2 Select with bit 5=1	/DCD0
PB1 System Config Reg.	/CTS0 (Note 1)
PB0	/RTS0
PC7	Always Reads /INT2 Ext. Status
PC6	Always Reads /INT1 Ext. Status
PC5	/W//REQA
PC4	/SYNCA
PC3 Select with bit 7=1	/DTR//REQA
PC2 System Config Reg.	/RTSA (Note 2)
PC1	/CTSA
PC0	/DCDA

Note 1:

When the Port function (PB1) is selected, the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

Note 2:

Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functions.

Z80182/Z8L182 FUNCTIONAL DESCRIPTION

Functionally, the on-chip Z182 MPU and ESCC™ are the same as the discrete devices (Figure 1). Therefore, for a detailed description of each individual unit, refer to the

Product Specification/Technical Manuals of each discrete product. The following subsections describe each of the individual units of the Z182.

Z182 MPU FUNCTIONAL DESCRIPTION

This unit provides all the capabilities and pins of the Zilog Z8S180 MPU (Static Z80180 MPU). Figure 4 shows the S180 MPU Block Diagram of the Z182. This allows 100%

software compatibility with existing Z180™ (and Z80®) software. The following is an overview of the major functional units of the Z182.

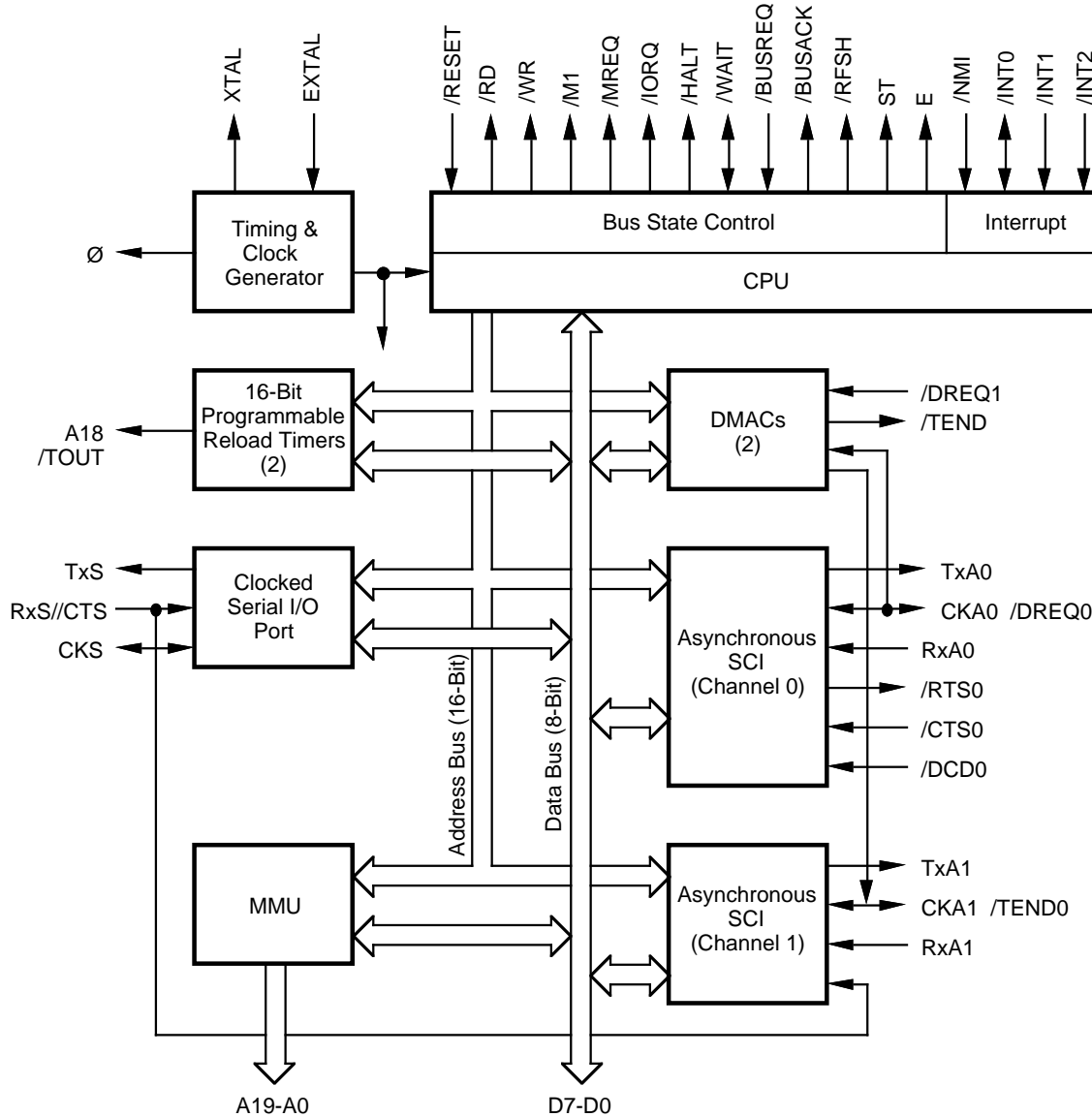


Figure 4. S180 MPU Block Diagram of Z182

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer,

which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

PARALLEL PORTS FUNCTIONAL DESCRIPTION

The Z80182/Z8L182 has three 8-bit bi-directional Ports. Each bit is individually programmable for input or output (with the exception of PC6 and PC7 which are inputs only).

The Ports are controlled through two registers: the Port Direction Control Register and the Port Data Register. (Please see register description for Ports A, B and C).

PROGRAMMING

The following subsections explain and define the parameters for I/O Address assignments. The three tables in this section describe the mapping of the common registers shared by the MPU and the 16550 MIMIC. The MPU address refers to the I/O address as accessed from the MPU side (the Z180™ MPU interface side of the 16550 MIMIC). Note that only the lowest eight address lines are decoded for Z182 peripheral access. The full sixteen

address lines are decoded for on-chip Z180 MPU access. The PC address (coined because the UART is common in PCs) is the address needed to access the MIMIC registers through the MIMIC interface signals. The MIMIC interface signals are multiplexed with the ESCC channel B and the Port A signals, and must be activated through the System Configuration Register and the Interrupt Edge/Pin MUX Register.

Table 7. Z80182/Z8L182 MPU Registers

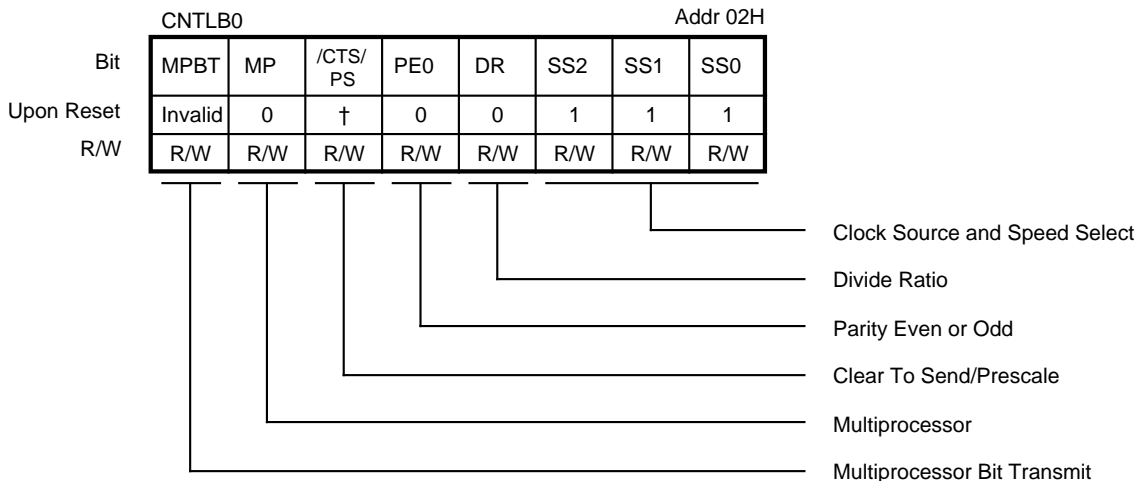
Register Name	MPU Addr	PC Addr
Z80182/Z8L182 MPU Control Registers	0000H to 00x3FH (Relocatable to 0040H to 007FH or 0080H to 00BFH)	None

Note:

“x” indicates don't care condition

Table 8. Z80182/Z8L182 MIMIC Register MAP

Register Name	MPU Addr/Access	PC Addr/Access
MMC MIMIC Master Control Register	xxFFH R/W	None
IUS/IP Interrupt Pending	xxFEH R/Wb7	None
IE Interrupt Enable	xxFDH R/W	None
IVC Interrupt Vector	xxFCH R/W	None
TTCR Transmit Time Constant	xxFAH R/W	None
RTCR Receive Time Constant	xxFBH R/W	None
FSCR FIFO Status and Control	xxECH R/W7-4	None
RTTC Receive Timeout Time Constant	xxEAH R/W	None
TTTC Transmit Timeout Time Constant	xxEBH R/W	None
RBR Receive Buffer Register	xxF0H W only	00H DLAB=0 R only
THR Transmit Holding Register	xxF0H R only	00H DLAB=0 W only
IER Interrupt Enable Register	xxF1H R only	01H DLAB=0 R/W
IIR Interrupt Identification	None	02H R only
FCR FIFO Control Register	xxE9H R only	02H W only
MM REGISTER	XXE9H W only	None
LCR Line Control Register	xxF3H R only	03H R/W
MCR Modem Control Register	xxF4H R only	04H R/W
LSR Line Status Register	xxF5H R/Wb6432	05H R only
MSR Modem Status Register	xxF6H R/Wb7-4	06H R only
SCR Scratch Register	xxF7H R only	07H R/W
DLL Divisor Latch (LSByte)	xxF8H R only	00H DLAB=1 R/W
DLM Divisor Latch (MSByte)	xxF9H R only	01H DLAB=1 R/W

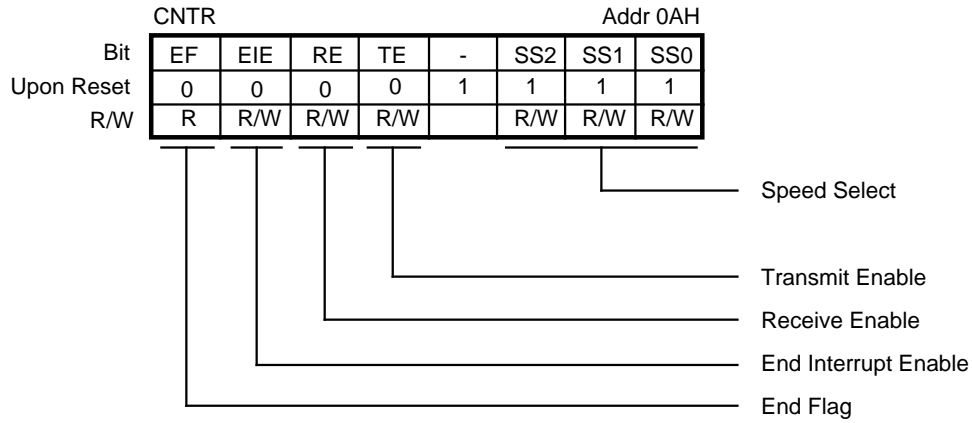


† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

General Divide Ratio	PS = 0 (Divide Ratio = 10)		PS = 1 (Divide Ratio = 30)	
SS, 2, 1, 0	DR = 0 (x16)	DR = 1 (x64)	DR = 0 (x16)	DR = 1 (x64)
000	$\emptyset \div 160$	$\emptyset \div 640$	$\emptyset \div 480$	$\emptyset \div 1920$
001	$\emptyset \div 320$	$\emptyset \div 1280$	$\emptyset \div 960$	$\emptyset \div 3840$
010	$\emptyset \div 640$	$\emptyset \div 2580$	$\emptyset \div 1920$	$\emptyset \div 7680$
011	$\emptyset \div 1280$	$\emptyset \div 5120$	$\emptyset \div 3840$	$\emptyset \div 15360$
100	$\emptyset \div 2560$	$\emptyset \div 10240$	$\emptyset \div 7680$	$\emptyset \div 30720$
101	$\emptyset \div 5120$	$\emptyset \div 20480$	$\emptyset \div 15360$	$\emptyset \div 61440$
110	$\emptyset \div 10240$	$\emptyset \div 40960$	$\emptyset \div 30720$	$\emptyset \div 122880$
111	External Clock (Frequency < $\emptyset \div 40$)			

Figure 11. ASCI Control Register B (Ch. 0)

CSI/O REGISTERS



SS2, 1, 0	Baud Rate
000	$\emptyset \div 20$
001	$\emptyset \div 40$
010	$\emptyset \div 80$
011	$\emptyset \div 100$

SS2, 1, 0	Baud Rate
100	$\emptyset \div 320$
101	$\emptyset \div 640$
110	$\emptyset \div 1280$
111	External Clock (Frequency < $\emptyset \div 20$)

Figure 21. CSI/O Control Register

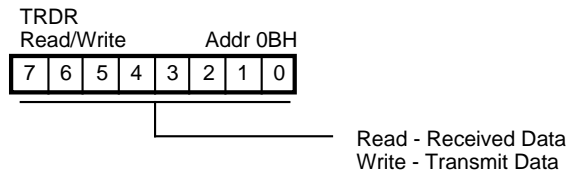


Figure 22. CSI/O Transmit/Receive Data Register

TIMER DATA REGISTERS

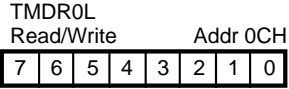
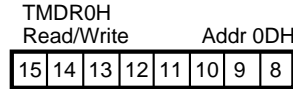


Figure 23. Timer 0 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 25. Timer 0 Data Register H

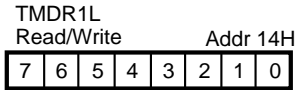
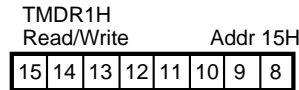


Figure 24. Timer 1 Data Register L



When Read, read Data Register L before reading Data Register H.

Figure 26. Timer 1 Data Register H

TIMER RELOAD REGISTERS

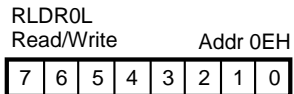


Figure 27. Timer 0 Reload Register L

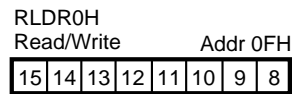


Figure 29. Timer 0 Reload Register H

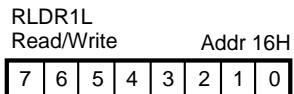


Figure 28. Timer 1 Reload Register L

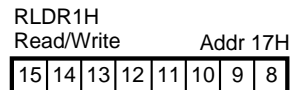


Figure 30. Timer 1 Reload Register H

When the part is in IDLE mode, the clock oscillator is kept oscillating, but the clock to the rest of the internal circuit, including the CLKOUT, is stopped completely. IDLE mode is exited in a similar way as STANDBY mode, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS, except that the 2^{17} bit wake-up timer is bypassed; all control signals are asserted eight clock cycles after the exit conditions are gathered.

STANDBY-QUICK RECOVERY Mode

STANDBY-QUICK RECOVERY mode is an option offered in STANDBY mode to reduce the clock recovery time in STANDBY mode from 2^{17} clock cycles (6.5 ms at 20 MHz) to 2^6 clock cycles (3.2 μ s at 20 MHz). This feature can only be used when providing an oscillator as clock source.

To enter STANDBY-QUICK RECOVERY mode:

1. Set D6 and D3 to 1 and 1, respectively.
2. Set the I/O STOP bit (D5 of ICR, I/O Address = 3FH) to 1.
3. Execute the SLEEP instruction.

When the part is in STANDBY-QUICK RECOVERY mode, the operation is identical to STANDBY mode except when exit conditions are gathered, i.e., RESET, BUS REQUEST or EXTERNAL INTERRUPTS; the clock and other control signals are recovered sooner than the STANDBY mode.

Note: If STANDBY-QUICK RECOVERY is enabled, the user must make sure stable oscillation is obtained within 64 clock cycles.

CPU Control Register

The Z8S180 has an additional register which allows the programmer to select options that directly affect the CPU performance as well as controlling the STANDBY operating mode of the chip. The CPU Control Register (CCR) allows the programmer to change the divide-by-two internal clock to divide-by-one. In addition, applications where EMI noise is a problem, the Z8S180 can reduce the output drivers on selected groups of pins to 25% of normal pad driver capability which minimizes the EMI noise generated by the part.

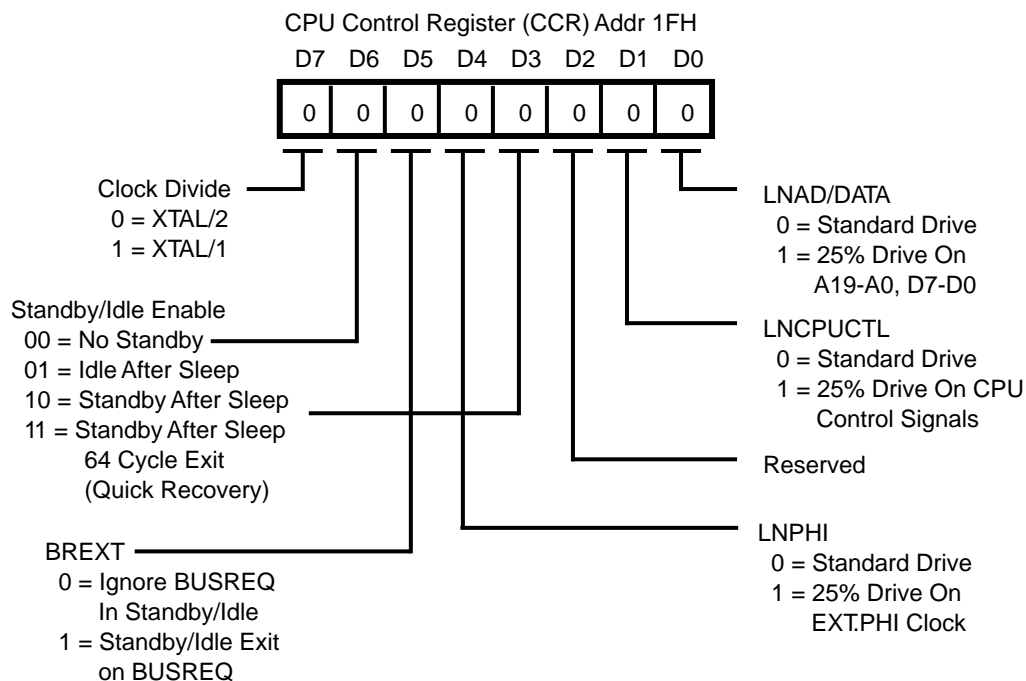


Figure 51. CPU Control Register

Z85230 ESCC™ CONTROL REGISTERS

See Figures 52 and 53 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification /Technical Manual.

The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. ***It is recommended that /TRxCB be programmed as an output with proper baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.***

Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

CONTROL REGISTERS (Continued)

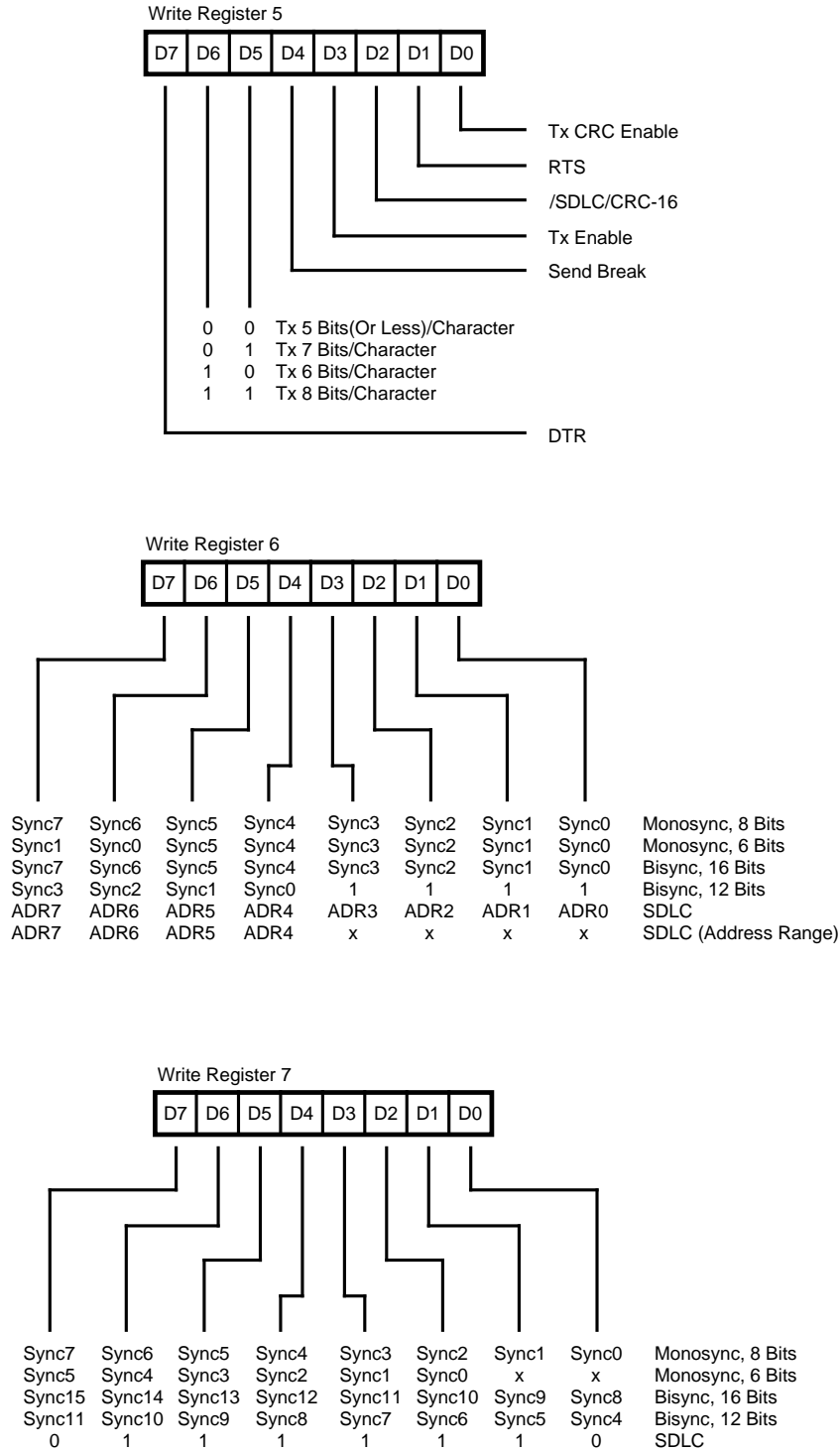


Figure 52. Write Register Bit Functions (Continued)

CONTROL REGISTERS (Continued)

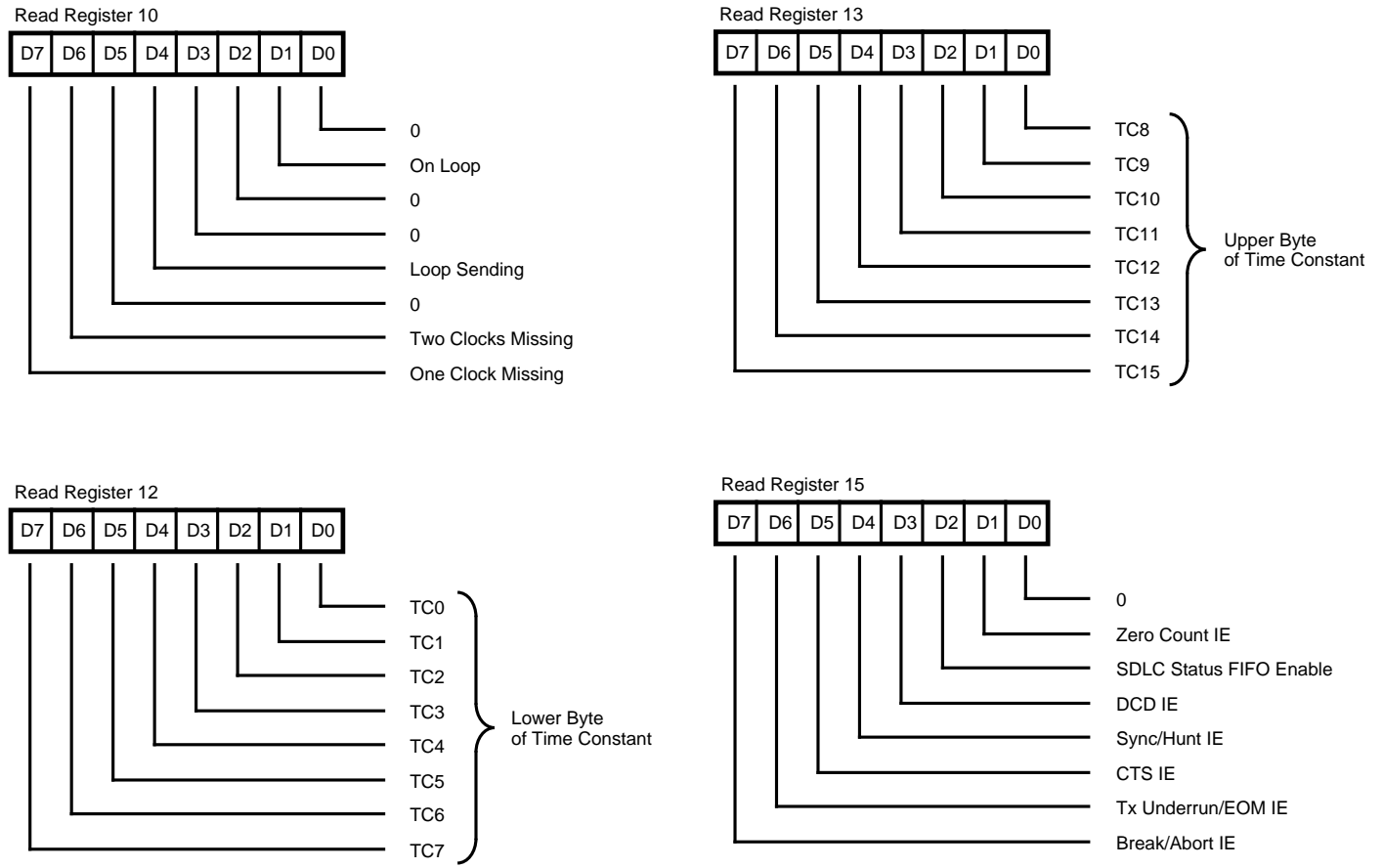


Figure 53. Read Register Bit Functions

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Bit 3 Disable ROMs

If this bit is 1, it disables the ROMCS pin. If it is 0, addresses below the ROM boundary set by the ROMBR register will cause the ROMCS pin to go Low.

Bit 2 Tri-Muxed Pins Select

The Z80182/Z8L182 has three pins that are triple multiplexed and controlled by bit 2 and bit 1. Table 14 shows the different modes.

Table 14. SCR Control for Triple Multiplexed Pins

Bit 2	Bit 1	System Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/TEND1,TxS,CKS
1	0	/RTSB,(/DTR//REQB),(/W//REQB)
1	1	/HRxRDY,/(HTxRDY,HINTR)

Bit 1 ESCC™ Channel B/MIMIC

If this bit is 0, Mode 0 is selected.
If this bit is 1, Mode 1 is selected.

Mode 0:

Channel A ESCC Enabled
Channel B ESCC Enabled
PIA Port Enabled
16550 MIMIC Interface Disabled

Mode 1:

Channel A ESCC enabled
Channel B outputs disabled
PIA disabled
16550 MIMIC Interface Enabled

Bit 0 Daisy Chain

This bit is used to set interrupt priority of the ESCC and 16550 MIMIC interface. If it is 0, the ESCC is higher up in the daisy chain than the 16550 MIMIC interface. If it is 1, the 16550 interface is higher up than the ESCC. Note that /INT0 is used for both MIMIC and ESCC Interrupts.

/RAMCS AND /ROMCS REGISTERS

To assist decoding of ROM and RAM blocks of memory, three more registers and two pins have been added to the

Z80182/Z8L182. The two pins are /ROMCS and /RAMCS. The three registers are RAMUBR, RAMLBR and ROMBR.

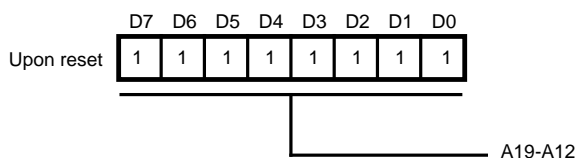


Figure 55. RAMUBR
(Z180 MPU Read/Write, Address xxE6H)

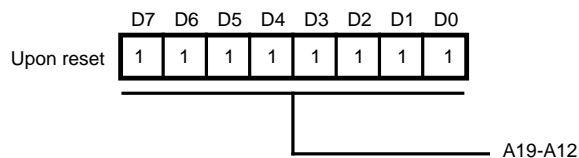


Figure 56. RAMLBR
(Z180 MPU Read/Write, Address xxE7H)

Bit 0 16450 MIMIC Mode Enable

(Reset value=0) This bit = 1 will force the mimic into 16450 mode. Bit 0 in the FCR reg is forced to zero as well as the mimic internal FIFO enable. When used, this bit should be programmed at MIMIC initialization and not modified afterwards.

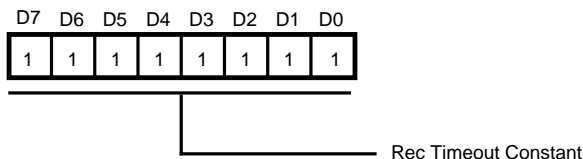


Figure 65. Receive Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEAH)

This register contains an 8-bit constant for emulation of the 16550 four character timeout feature. Software must determine the value to load into this register based on the bit rate and word length specified by the MIMIC interface with the PC. This timer receives its input from the /TRxCB Clock of the ESCC. This timer is enabled to down count when the enable bit in the FSR register is set and the trigger level interrupt has not been activated on the RCVR FIFO. The counter reloads and counts down each time there is a read or write to the RCVR FIFO.

The receive timeout timer is enhanced to emulate the actual 16550 when bit 1 of the FIFO status and control register is enabled. Under most circumstances, this register should be programmed for four character timers (40d, 8-N-1).

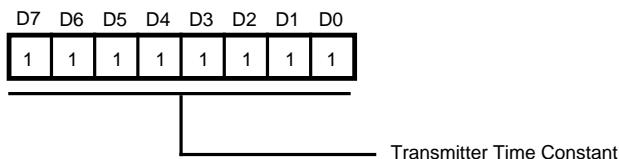


Figure 66. Transmitter Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEBH)

This register contains an 8-bit constant for determining the interval for the Transmit Timeout Timer. If allowed to decrement to zero, this timer interrupts the MPU by setting the THR bit in the IUS/IP register. This timer receives its input from the /TRxCB Clock of the SCC. The timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the XMIT FIFO. The counter reloads each time there is a read or write to the XMIT FIFO.

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z180™ MPU and the PC/XT/AT, two timers have been added to alleviate any software problems that a high speed parallel data transfer might cause. These timers allow the programmer to slow down the data transfer just as if the 16550 MIMIC interface had to shift the data in and out serially. The Timers receive their input from the /TRxCB Clock since, in 16550 MIMIC mode, the ESCC channel B is disabled. For example, the clock source for the 8-bit registers: RTTC (Receive Timeout Time Constant, xxEAH), TTTC (Transmit Timeout Time Constant, xxEBH), TTCR (Transmit Time Constant Register, xxFAH) and RTCR (Receive Time Constant Register, xxFBH) uses the /TRxCB Clock output. The /TRxCB Clock output needs to be generated by the ESCC's channel B's 16-bit BRG as its clock source, thus allowing the programmer to access a total of 24 bits as a timer to slow down the data transfer.

In most cases, ESCC Ch. B BRG should be programmed to output at a frequency equivalent to the desired serial transfer rate. The output of the BRG should be routed to the /TRxCB pin.

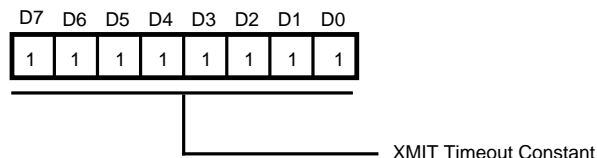


Figure 67. Transmitter Time Constant Register
(Z180 MPU Read/Write, Address xxFAH)

16550 MIMIC REGISTERS (Continued)

FIFO Control Register

Bit 6 and Bit 7 RCVR trigger LSB and MSB bits

This 2-bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs (see Table 18).

Bit 4 and Bit 5

Reserved for future use (PC side). Note: From the MPU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side will clear a previously set bit 4 or bit 5.

Bit 3 DMA mode select

Setting this bit to 1 will cause the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A 1 in this bit enables multi-byte DMA).

Bit 2 XMIT FIFO Reset

Setting this bit to 1 will cause the transmitter FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 1 RCVR FIFO Reset

Setting this bit to 1 will cause the receiver FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 0 FIFO Enable

The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be 1 when writing to the other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared. This feature can be forced in a disabled state by the MPU.

Table 18. Receive Trigger Level

b7	b6	Trigger Level, Number of Bytes
0	0	1
0	1	4
1	0	8
1	1	14

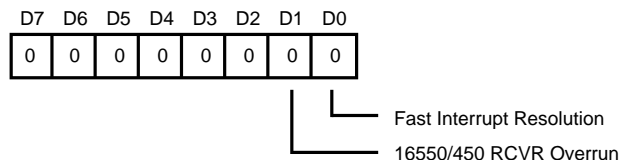


Figure 72. MIMIC Modification Register
(Z180 MPU Write only, Address xxE9h)

Bit 7-2 Reserved. Program to zero.

Bit 1 RCVR Overrun Modification

The actual 16450/16550 device allows the last position in FIFO to be overwritten by DCE during receiver overrun condition. When this bit is enabled (programmed to 1) the last position in FIFO can be overwritten by Z180 during receiver overrun. This feature is disabled by default. When this modification is not enabled, the MIMIC will ignore any write to RBR during an overrun condition.

Bit 0 Fast MIMIC-ESCC Interrupt Resolution

When enabling this modification, the internal MIMIC IEO signal into the ESCC IEI input is forced Low when the MIMIC Interrupt line becomes active. This is required to prevent the ESCC from putting it's vector on the databus during an INTACK cycle (given that the MIMIC is programmed to have higher interrupt priority).

When disabled, the internal MIMIC IEO becomes deasserted only after an interrupt acknowledge cycle. In this case, it is possible for the ESCC to force it's interrupt vector onto the data bus even when the MIMIC has a pending interrupt and is higher in priority.

Z80182 ENHANCEMENTS REGISTER

Bit <7-6> Reserved

Bit 5 Force Z180 Halt Mode

If this bit is set to 1, it disables the 16 cycle halt recovery and halt control over the busses and pins. This bit is used to allow DMA and Refresh Access to take place during halt (like Z180). This bit is set to 0 on reset.

Bit 4 TxDA Tri-state

The TxDA pin can be tri-stated on assertion of the /HALT pin. This prevents the TxDA from driving and external device when /HALT output is used to force other devices into power-down modes. This feature is disabled on power-up or reset. It is also controlled by bit 5 in the enhancement register, this feature is disabled if bit 5 is set.

Bit 3 ESCC Clock Divider

The ESCC clock can be provided with the Z180 core's PHI clock or by a PHI clock divide by 2 circuit. When this bit is set, the ESCC's clock will be Z180's PHI clock divided by

two. Upon power-up or reset, the ESCC clock frequency is equal to the Z180 core's PHI clock output.

Note: If operating above 20 MHz/5V or 10 MHz/3V, this bit should be set for ESCC divide-by-two mode.

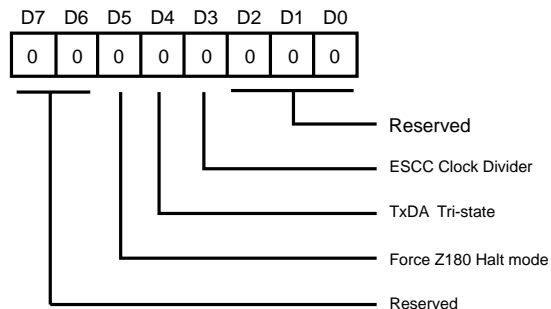
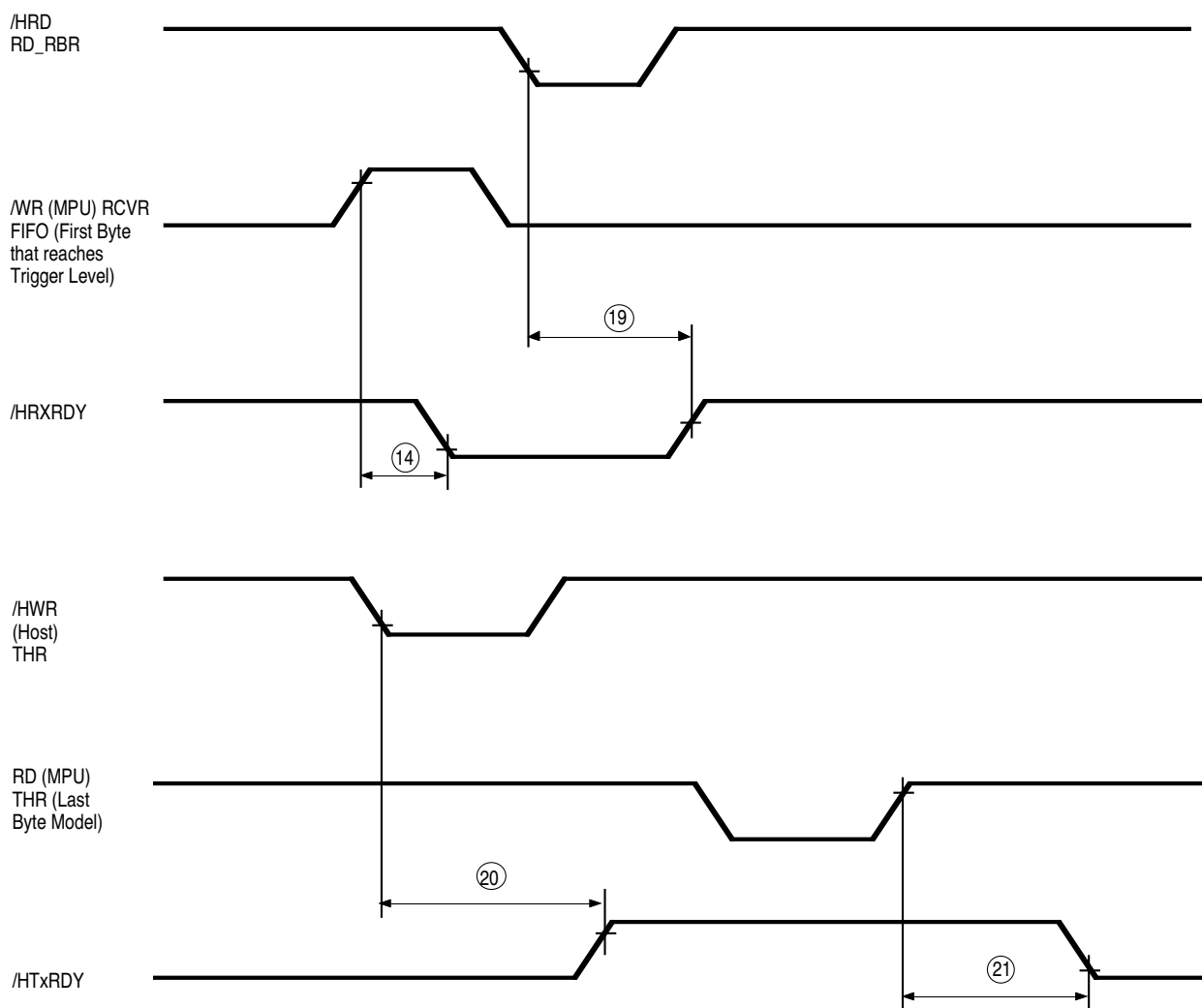


Figure 82. Z80182 Enhancements Register
(Z180 MPU Read/Write, Address xxD9H)

Table L. Interrupt Timing Transmitter FIFO

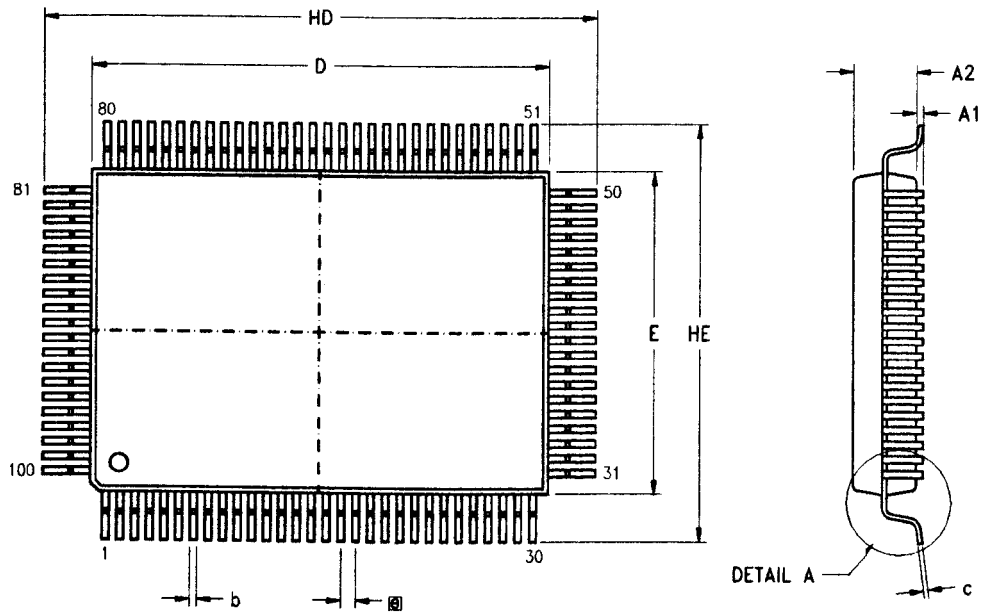
No.	Sym	Parameter	Z8L182 20 MHz		Z80182 33 MHz	
			Min	Max	Min	Max
16	tHR	Delay from /WR (WR THR) to Reset Interrupt		2.5 MPU Clock Cycles		2.5 MPU Clock Cycles
17	TSTI	Delay from Stop to Interrupt (THRE)	2 MPU Clock Cycles		2 MPU Clock Cycles	
18	TIR	Delay from /RD (RD IIR) to Reset Interrupt (THRIE)		75		75



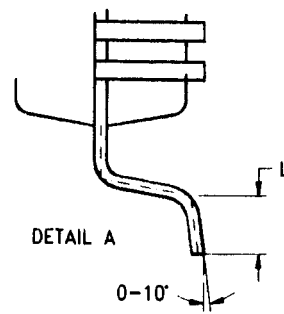
Note: If FCR0-1
TSINT=3 CPU
Clock Cycles

Figure 116 RCVR FIFO Bytes Other Than First

PACKAGE INFORMATION (Continued)



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.10	0.30	.004	.012
A2	2.60	2.80	.102	.110
b	0.25	0.40	.010	.016
c	0.13	0.20	.005	.008
HD	23.70	24.15	.933	.951
D	19.90	20.10	.783	.791
HE	17.70	18.15	.697	.715
E	13.90	14.10	.547	.555
e	0.65 TYP		.0256 TYP	
L	0.70	1.10	.028	.043



NOTES:
 1. CONTROLLING DIMENSIONS : MILLIMETER
 2. MAX COPLANARITY : $\frac{.10}{.004}$

100-Pin QFP Package Diagram