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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-LQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l18220asg

Z180 CPU SIGNALS

A19-A0. *Address Bus (input/output, active High, tri-state).* A19-A0 form a 20-bit address bus. The Address Bus provides the address for memory data bus exchanges up to 1 Mbyte, and I/O data bus exchanges up to 64K. The address bus enters a high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states. This bus is an input when the external bus master is accessing the on-chip peripherals. Address line A18 is multiplexed with the output of PRT channel 1 (T_{OUT}, selected as address output on reset).

D7-D0. *Data Bus (bi-directional, active High, tri-state).* D7-D0 constitute an 8-bit bi-directional data bus, used for the transfer of information to and from I/O and memory devices. The data bus enters the high impedance state during reset and external bus acknowledge cycles, as well as during SLEEP and HALT states.

/RD. *Read (input/output, active Low, tri-state).* /RD indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O or memory device should use this signal to gate data onto the CPU data bus.

/WR. *Write (input/output, active Low, tri-state).* /WR indicates that the CPU data bus holds valid data to be stored at the addressed I/O or memory location.

/IORQ. *I/O Request (input/output, active Low, tri-state).* /IORQ indicates that the address bus contains a valid I/O address for an I/O read or I/O write operation. /IORQ is also generated, along with /M1, during the acknowledgment of the /INT0 input signal to indicate that an interrupt response vector can be placed onto the data bus. This signal is analogous to the IOE signal of the Z64180.

/M1. *Machine Cycle 1 (input/output, active Low).* Together with /MREQ, /M1 indicates that the current cycle is the opcode fetch cycle of an instruction execution; unless /M1E bit in the OMCR is cleared to 0. Together with /IORQ, /M1 indicates that the current cycle is for an interrupt acknowledge. It is also used with the /HALT and ST signals to decode status of the CPU machine cycle. This signal is analogous to the /LIR signal of the Z64180.

/MREQ. *Memory Request (input/output, active Low, tri-state).* /MREQ indicates that the address bus holds a valid address for a memory read or memory write operation. This signal is analogous to the /ME signal of the Z64180. /MREQ is multiplexed with /MRD on the /MRD//MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if the /MREQ function is selected; and is inactive High if /MRD function is selected.

/MRD. *Memory Read (input/output, active Low, tri-state).* /MRD is active when both the internal /MREQ and /RD are active. /MRD is multiplexed with /MREQ on the /MRD//MREQ pin. The /MRD//MREQ pin is an input during adapter modes; is tri-state during bus acknowledge if /MREQ function is selected; and is inactive High if /MRD function is selected. The default function on power up is /MRD and may be changed by programming bit 3 of the Interrupt Edge/Pin MUX Register (xxDFH).

/MWR. *Memory Write (input/output, active Low, tri-state).* /MWR is active when both the internal /MREQ and /WR are active. This /RTSA or PC2 combination is pin multiplexed with /MWR on the /MWR/PC2//RTSA pin. The default function of this pin on power up is /MWR, which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/WAIT. *(input/output active Low).* /WAIT indicates to the MPU that the addressed memory or I/O devices are not ready for a data transfer. This input is used to induce additional clock cycles into the current machine cycle. The /WAIT input is sampled on the falling edge of T2 (and subsequent wait states). If the input is sampled Low, then additional wait states are inserted until the /WAIT input is sampled High, at which time execution will continue.

/HALT. *Halt/Sleep Status (input/output, active Low).* This output is asserted after the CPU has executed either the HALT or SLEEP instruction, and is waiting for either non-maskable or maskable interrupts before operation can resume. It is also used with the /M1 and ST signals to decode status of the CPU machine cycle. On exit of HALT/SLEEP mode, the first instruction fetch can be delayed by 16 clock cycles after the /HALT pin goes High, if HALT 16 feature is selected.

/BUSACK. *Bus Acknowledge (input/output, active Low).* /BUSACK indicates to the requesting device, the MPU address and data bus, and some control signals, have entered their high impedance state.

/BUSREQ. *Bus Request (input, active Low).* This input is used by external devices (such as DMA controllers) to request access to the system bus. This request has a higher priority than /NMI and is always recognized at the end of the current machine cycle. This signal will stop the CPU from executing further instructions and places the address/data buses and other control signals, into the high impedance state.

MULTIPLEXED PIN DESCRIPTIONS

A18/$T_{OUT.}$ During Reset, this pin is initialized as an A18 pin. If either TOC1 or TOC0 bit of the Timer Control Register (TCR) is set to 1, The T_{OUT} function is selected. If TOC1 and TOC0 bits are cleared to 0, the A18 function is selected.

In normal user mode (on-chip bus master), the A18 signal for the chip select logic is obtained from the CPU before the external pin is muxed as A18/T_{OUT}. Therefore, the selection of T_{OUT} will not affect the operation of the 182 chip select logic. However, in adapter mode (off-chip bus master), the A18 signal MUST be provided by the external bus master.

CKA0//DREQ0. During Reset, this pin is initialized as CKA0 pin. If either DM1 or SM1 in the DMA Mode Register (DMODE) is set to 1, /DREQ0 function is always selected.

CKA1//TEND0. During Reset, this pin is initialized as CKA1 pin. If CKA1D bit in the ASCI control register Ch1(CNTLA1) is set to 1, /TEND0 function is selected. If CKA1D bit is set to 0, CKA1 function is selected.

RxS//CTS1. During Reset, this pin is initialized as the RxS pin. If CTS1E bit in the ASCI status register Ch1 (STAT1) is set to 1, /CTS1 function is selected. If CTS1E bit is set to 0, RxS function is selected. This pin is also multiplexed with PB7 based on bit 6 in the System Configuration Register.

The pins below are triple-multiplexed based upon the values of bit 1 and bit 2 of the System Configuration Register. The pins are configured as Table 2 specifies. On Reset, both bits 1 and 2 are 0, so /TEND1,TxS,CKS are selected.

Table 2. Triple Multiplexed Pins

Bit 1	Bit 2	Master Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/RTSB,/DTR//REQB,/W//REQB
1	0	/TEND1,TxS,CKS
1	1	/HRxRDY,//HTxRDY,HINTR

The pins below are multiplexed based upon the value of bit 1 of the System Configuration register. If bit 1 is 0, then the Z80182/Z8L182 Mode 0 (non-16550 MIMIC mode) signals are selected; if bit 1 is 1, then Z80182/Z8L182 Mode 1 (16550 MIMIC mode) signals are selected. On Reset, Z80182/Z8L182 Mode 0 is always selected as shown in Table 3.

Table 3. Mode 0 and Mode 1 Multiplexed Pins

Z80182/Z8L182 Mode 0	Z80182/Z8L182 Mode 1
TxDB	/HDDIS
RxDB	HA1
/TRxCB	HA0
/RTxCB	HA2
/SYNCB	/HCS
/CTSB	/HWR
/DCDB	/HRD
PA7-PA0	HD7-HD0

Table 5. Primary, Secondary and Tertiary Pin Functions (Continued)

Pin Number VQFP	QFP	1st Function	2nd Function	3rd Function	MUX Control
71	74	RxDA			
72	75	/TRxCA			
73	76	TxDA			
74	77	/DCDB	/HRD		SYS CONF REG Bit 1
75	78	/CTSB	/HWR		SYS CONF REG Bit 1
76	79	TxDB	/HDDIS		SYS CONF REG Bit 1
77	80	/TRxCB	HA0		SYS CONF REG Bit 1
78	81	RxDB	HA1		SYS CONF REG Bit 1
79	82	/RTxCB	HA2		SYS CONF REG Bit 1
80	83	/SYNCB	/HCS		SYS CONF REG Bit 1
81	84	/HALT			
82	85	/RFSH			
83	86	/IORQ			
84	87	/MRD	/MREQ		INT EDG/PIN REG Bit 3
85	88	E			
86	89	/M1			
87	90	/WR			
88	91	/RD			
89	92	PHI			
90	93	V_{SS}			
91	94	XTAL			
92	95	EXTAL			
93	96	/WAIT			
94	97	/BUSACK			
95	98	/BUSREQ			
96	99	/RESET			
97	100	/NMI			
98	1	/INT0			
99	2	/INT1	PC6**		
100	3	/INT2	PC7**		

Notes:
* Also controlled by Interrupt Edge/Pin MUX Register
** PC7 and PC6 are inputs only and can read values of /INT1 and /INT2.

On the MPU interface, the transmitted data available can be programmed to interrupt the MPU on 1, 4, 8 or 14 bytes of available data by seeing the appropriate value in the MPU FSCR control register (MPU write only xxECH) bits 6 and 7. A timeout feature exists, Transmit Timeout Timer, which is an additional 8-bit timer with SCC TxRCB as the input source. If the transmitter FIFO is non-empty and no PC write or MPU read of the FIFO has taken place within the timer interval, a timeout occurs causing a corresponding interrupt to the MPU.

Z80182/Z8L182 MIMIC SYNCHRONIZATION CONSIDERATIONS

Because of the asynchronous nature of the FIFO's on the MIMIC, some synchronization plan must be provided to prevent conflict from the dual port accesses of the MPU and the PC.

To solve this problem, I/O to the FIFO is buffered and the buffers allow both PC and MPU to access the FIFO asynchronously. Read and Write requests are then synchronized by means of the MPU clock. Incoming signals are buffered in such a way that metastable input levels are stabilized to valid 1 or 0 levels. Actual transfers to and from the buffers, from and to the FIFO memory, are timed by the MPU clock. ALU evaluation is performed on a different phase than the transfer to ensure stable pointer values.

Another potential problem is that of simultaneous access of the MPU and PC to any of the various 'mailbox' type registers. This is solved by dual buffering of the various read/write registers. During a read access by either the MPU or PC to a mailbox register, the data in the output or slave portion of the buffered register is not permitted to change. Any write that might take place during this time will be stored in the input of master part of the register. The corresponding status/interrupt is reset appropriately based on the write having followed the read to the register. For example, the IUS/IP bit for the LCR write will not be cleared by the MPU read of the LCR if a simultaneous write to the LCR by the PC takes place. Instead the LSR data will change after the read access and IUS/IP bit 3 remains at logic 1.

Z80182 MIMIC DOUBLE BUFFERING FOR THE TRANSMITTER

The Z80182 Rev DA implements double buffering for the transmitter in 16450 mode and sets the TEMT bit in the LSR Register automatically.

When this feature is enabled and character delay emulation is being used (see Figure 9):

1. The PC THRE bit in the LSR Register is set when the THR Register is empty;
2. PC Host writes to the 16450 THR Register;
3. Whenever the Z80182 TSR buffer is empty and one character delay timer is in a timed-out state, the byte from the THR Register is transferred to the TSR buffer; the timer is in timed-out state after FIFO Reset or after Host TEMT is set. This allows a dual write to THR when Host TEMT is set.
4. Restart character delay timer (timer reloads and counts down) with byte transfer from THR Register to the TSR buffer;
5. Whenever the TSR buffer is full, the TEMT bit in MPU LSR Register is reset with no delay;
6. MPU reads TSR buffer;
7. TEMT bit in LSR Register for MPU is set with no delay whenever the TSR buffer is empty;
8. When the TSR buffer is read by MPU and THR Register is empty and one character delay timer reaches zero, the TEMT bit in the LSR Register for Host is set from 0 to 1.

The PC THRE bit in the LSR Register is reset whenever the THR Register is full and set whenever THR Register is empty.

MPU IREQ and DMA Request for the transmit data is trigger whenever TSR buffer is full and cleared whenever TSR buffer is empty.

If character delay emulation is not used the TEMT bit in the LSR Register is set whenever both the THR Register and the TSR buffer are both empty. The Host TEMT bit is clear if there is data in either the TSR buffer of THR Register.

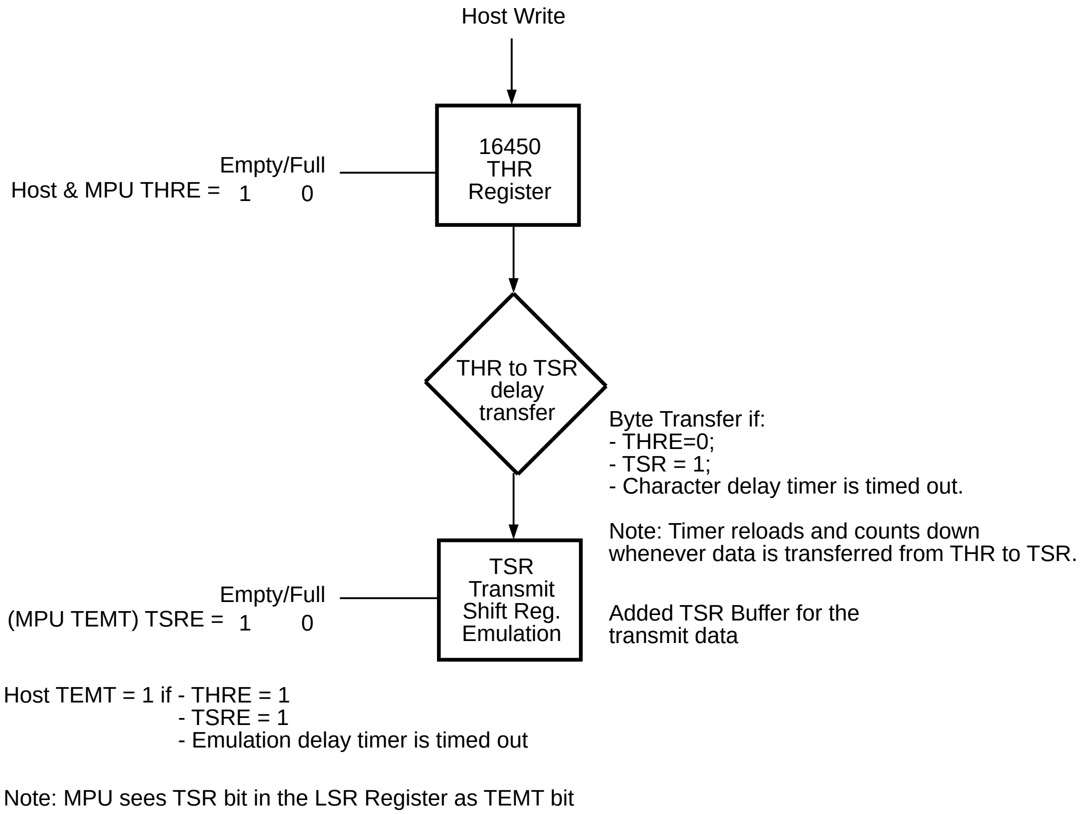

Host Write
16450 THR Register
Empty/Full
Host & MPU THRE = 1 0
THR to TSR delay transfer
Byte Transfer if:
- THRE=0;
- TSR = 1;
- Character delay timer is timed out.
Note: Timer reloads and counts down whenever data is transferred from THR to TSR.
TSR Transmit Shift Reg. Emulation
Empty/Full
(MPU TEMT) TSRE = 1 0
Added TSR Buffer for the transmit data
Host TEMT = 1 if - THRE = 1
- TSRE = 1
- Emulation delay timer is timed out
Note: MPU sees TSR bit in the LSR Register as TEMT bit

Figure 9. TEMT Emulation Logic Implementation

PROGRAMMING (Continued)

Table 9. Z80182/Z8L182 ESCC, PIA and MISC Registers

Register Name	MPU Addr/Access		PC Addr/Access
WSG Chip Select Register	xxD8H	R/W	None
Z80182 Enhancements Register	xxD9H	R/W	None
PC Data Direction Register	xxDDH	R/W	None
PC Data Register	xxDEH	R/W	None
Interrupt Edge/Pin MUX Control	xxDFH	R/W	None
ESCC Chan A Control Register	xxE0H	R/W	None
ESCC Chan A Data Register	xxE1H	R/W	None
ESCC Chan B Control Register	xxE2H	R/W	None
ESCC Chan B Data Register	xxE3H	R/W	None
PB Data Direction Register	xxE4H	R/W	None
PB Data Register	xxE5H	R/W	None
RAMUBR RAM Upper Boundary Register	xxE6H	R/W	None
RAMLBR RAM Lower Boundary Register	xxE7H	R/W	None
ROM Address Boundary Register	xxE8H	R/W	None
PA Data Direction Register	xxEDH	R/W	None
PA Data Register	xxEEH	R/W	None
System Configuration Register	xxEFH	R/W	None

ASCI CHANNELS CONTROL REGISTERS (Continued)

CNTLA1 Addr 01H

Bit	MPE	RE	TE	CKA1D	MPBR/ EFR	MOD2	MOD1	MOD0
Upon RESET	0	0	0	1	x	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

			MODE Selection
0	0	0	Start + 7-Bit Data + 1 Stop
0	0	1	Start + 7-Bit Data + 2 Stop
0	1	0	Start + 7-Bit Data + Parity + 1 Stop
0	1	1	Start + 7-Bit Data + Parity + 2 Stop
1	0	0	Start + 8-Bit Data + 1 Stop
1	0	1	Start + 8-Bit Data + 2 Stop
1	1	0	Start + 8-Bit Data + Parity + 1 Stop
1	1	1	Start + 8-Bit Data + Parity + 2 Stop

Read - Multiprocessor Bit Receive
Write - Error Flag Reset

CKA1 Disable

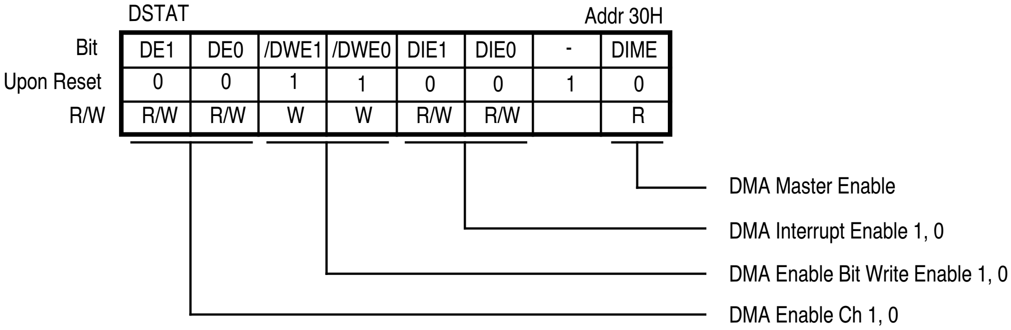
Transmit Enable

Receive Enable

Multiprocessor Enable

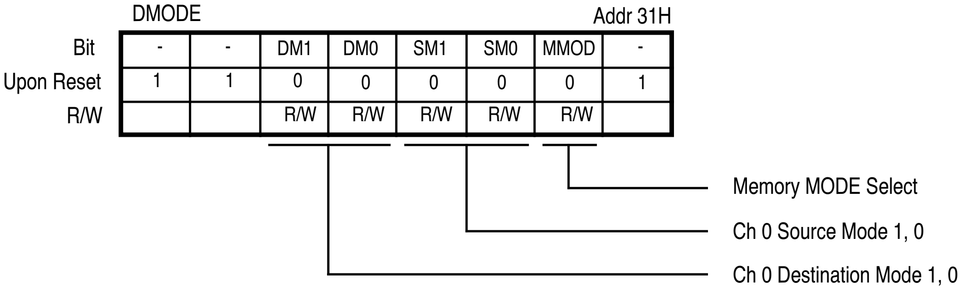
Figure 10b. ASCI Control Register A (Ch. 1)

DMA REGISTERS (Continued)


DSTAT
Addr 30H
DMA Master Enable
DMA Interrupt Enable 1, 0
DMA Enable Bit Write Enable 1, 0
DMA Enable Ch 1, 0

Bit	DE1	DE0	/DWE1	/DWE0	DIE1	DIE0	-	DIME
Upon Reset	0	0	1	1	0	0	1	0
R/W	R/W	R/W	W	W	R/W	R/W		R

Figure 40. DMA Status Register


DMODE
Addr 31H
Memory MODE Select
Ch 0 Source Mode 1, 0
Ch 0 Destination Mode 1, 0

Bit	-	-	DM1	DM0	SM1	SM0	MMOD	-
Upon Reset	1	1	0	0	0	0	0	1
R/W			R/W	R/W	R/W	R/W	R/W	

DM1, 0	Destination	Address
00	M	DAR0+1
01	M	DAR0-1
10	M	DAR0 Fixed
11	I/O	DAR0 Fixed

SM1, 0	Source	Address
00	M	SAR0+1
01	M	SAR0-1
10	M	SAR0 Fixed
11	I/O	SAR0 Fixed

MMOD	Mode
0	Cycle Steal Mode
1	Burst Mode

Figure 41. DMA Mode Registers

STANDBY Mode Exit with BUS REQUEST

Optionally, if the BREXT bit (D5 of CPU Control Register) is set to 1, the Z8S180 exits STANDBY mode when the /BUSREQ input is asserted; the crystal oscillator is then restarted. An internal counter automatically provides time for the oscillator to stabilize, before the internal clocking and the system clock output of the Z8S180 are resumed.

The Z8S180 relinquishes the system bus after the clocking is resumed by:

- Tri-State the address outputs A19 through A0.
- Tri-State the bus control outputs /MREQ, /IORQ, /RD and /WR.
- Asserting /BUSACK

The Z8S180 regains the system bus when /BUSREQ is deactivated. The address outputs and the bus control outputs are then driven High; the STANDBY mode is exited.

If the BREXT bit of the CPU Control Register (CCR) is cleared, asserting the /BUSREQ would not cause the Z8S180 to exit STANDBY mode.

If STANDBY mode is exited due to a reset or an external interrupt, the Z8S180 remains relinquished from the system bus as long as /BUSREQ is active.

STANDBY Mode Exit with External Interrupts

STANDBY mode can be exited by asserting input /NMI. The STANDBY mode may also exit by asserting /INT0, /INT1 or /INT2, depending on the conditions specified in the following paragraphs.

/INT0 wake-up requires assertion throughout duration of clock stabilization time (2^{17} clocks).

If exit conditions are met, the internal counter provides time for the crystal oscillator to stabilize, before the internal clocking and the system clock output within the Z8S180 are resumed.

1. Exit with Non-Maskable Interrupts

If /NMI is asserted, the CPU begins a normal NMI interrupt acknowledge sequence after clocking resumes.

2. Exit with External Maskable Interrupts

If an External Maskable Interrupt input is asserted, the CPU responds according to the status of the Global Interrupt Enable Flag IEF1 (determined by the ITE1 bit) and the settings of the corresponding interrupt enable bit in the Interrupt/Trap Control Register (ITC: I/O Address = 34H):

a. If an interrupt source is disabled in the ITC, asserting the corresponding interrupt input would not cause the Z8S180 to exit STANDBY mode. This is true regardless of the state of the Global Interrupt Enable Flag IEF1.

b. If the Global Interrupt Flag IEF1 is set to 1, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input causes the Z8S180 to exit STANDBY mode. The CPU performs an interrupt acknowledge sequence appropriate to the input being asserted when clocking is resumed if:

- The interrupt input follows the normal interrupt daisy chain protocol.
- The interrupt source is active until the acknowledge cycle is completed.

c. If the Global Interrupt Flag IEF1 is disabled, i.e., reset to 0, and if an interrupt source is enabled in the ITC, asserting the corresponding interrupt input will still cause the Z8S180 to exit STANDBY mode. The CPU will proceed to fetch and execute instructions that follow the SLEEP instruction when clocking is resumed.

If the External Maskable Interrupt input is not active until clocking resumes, the Z8S180 will not exit STANDBY mode. If the Non-Maskable Interrupt (/NMI) is not active until clocking resumes, the Z8S180 still exits the STANDBY mode even if the interrupt sources go away before the timer times out, because /NMI is edge-triggered. The condition is latched internally once /NMI is asserted Low.

IDLE Mode

IDLE mode is another power-down mode offered by the Z8S180. To enter IDLE mode:

1. Set D6 and D3 to 0 and 1, respectively.

2. Set the I/O STOP bit (D5 of ICR,
I/O Address = 3FH) to 1.

3. Execute the SLEEP instruction.

Z85230 ESCC™ CONTROL REGISTERS

See Figures 52 and 53 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification /Technical Manual.

The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. ***It is recommended that /TRxCB be programmed as an output with proper baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.***

Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

CONTROL REGISTERS (Continued)

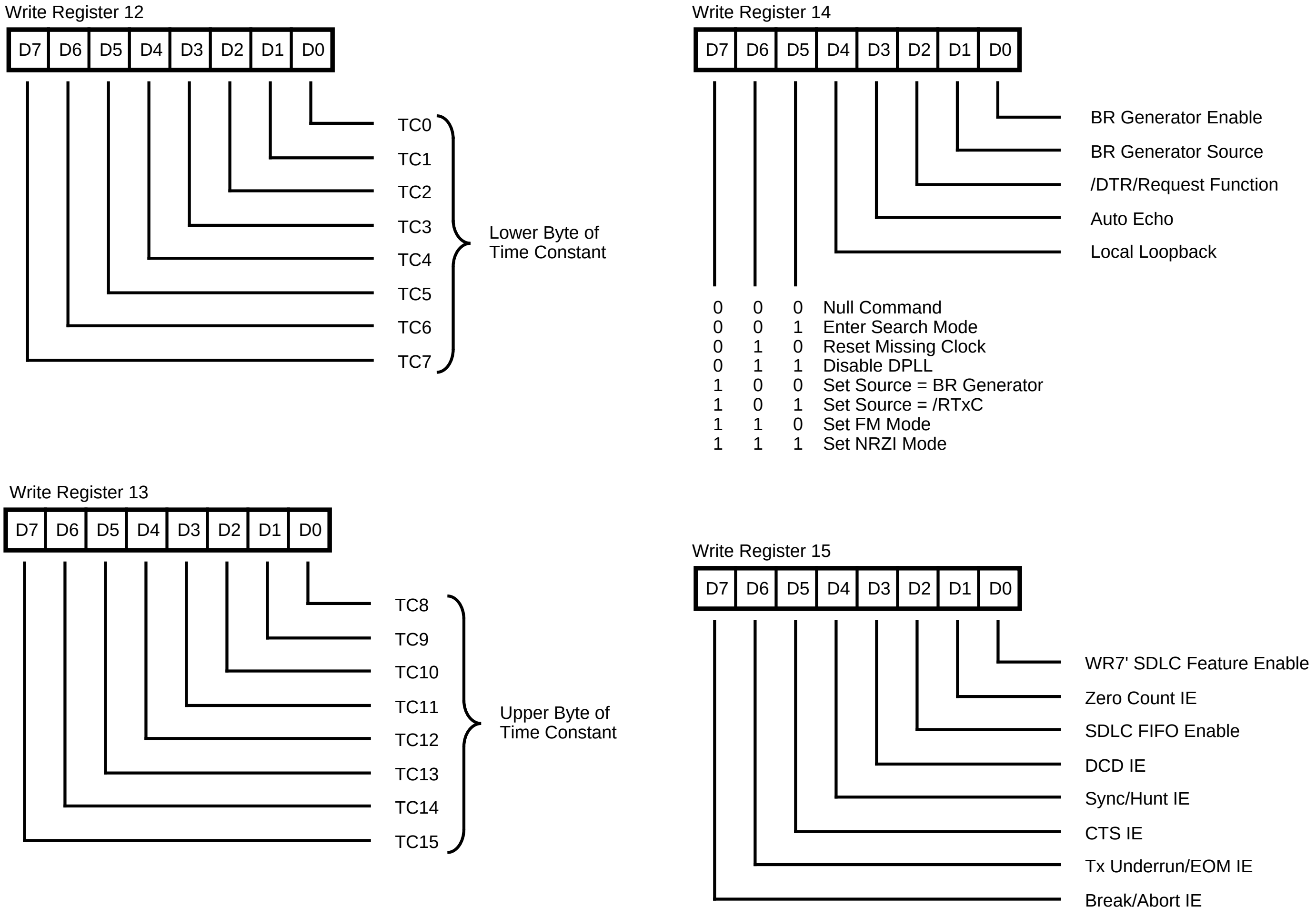

Write Register 12
D7 D6 D5 D4 D3 D2 D1 D0
TC0
TC1
TC2
TC3
TC4
TC5
TC6
TC7
Lower Byte of Time Constant
Write Register 14
D7 D6 D5 D4 D3 D2 D1 D0
BR Generator Enable
BR Generator Source
/DTR/Request Function
Auto Echo
Local Loopback
0 0 0 Null Command
0 0 1 Enter Search Mode
0 1 0 Reset Missing Clock
0 1 1 Disable DPLL
1 0 0 Set Source = BR Generator
1 0 1 Set Source = /RTxC
1 1 0 Set FM Mode
1 1 1 Set NRZI Mode
Write Register 13
D7 D6 D5 D4 D3 D2 D1 D0
TC8
TC9
TC10
TC11
TC12
TC13
TC14
TC15
Upper Byte of Time Constant
Write Register 15
D7 D6 D5 D4 D3 D2 D1 D0
WR7' SDLC Feature Enable
Zero Count IE
SDLC FIFO Enable
DCD IE
Sync/Hunt IE
CTS IE
Tx Underrun/EOM IE
Break/Abort IE

Figure 52. Write Register Bit Functions (Continued)

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Figures 54 through 65 describe miscellaneous registers that control the Z182 configuration, RAM/ROM chip select, interrupt and various status and timers.

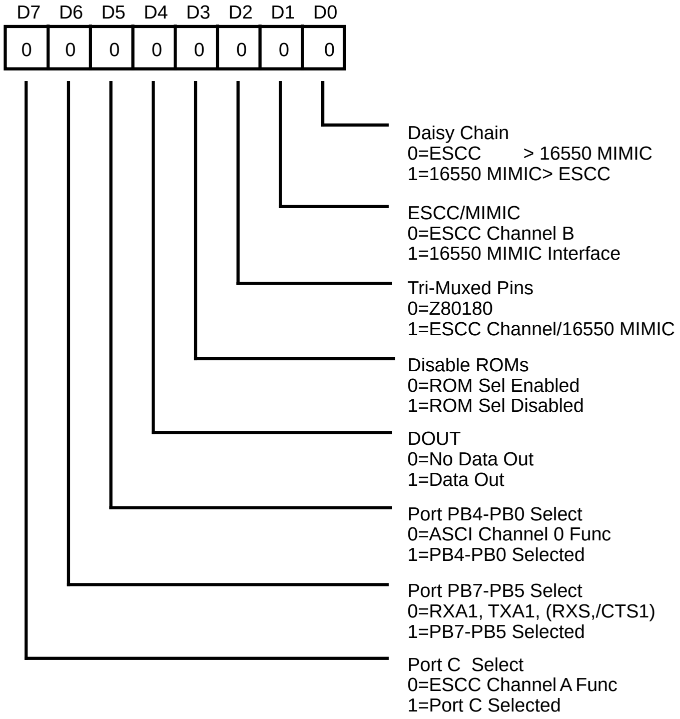

D7
D6
D5
D4
D3
D2
D1
D0
0
0
0
0
0
0
0
0
Daisy Chain
0=ESCC > 16550 MIMIC
1=16550 MIMIC> ESCC
ESCC/MIMIC
0=ESCC Channel B
1=16550 MIMIC Interface
Tri-Muxed Pins
0=Z80180
1=ESCC Channel/16550 MIMIC
Disable ROMs
0=ROM Sel Enabled
1=ROM Sel Disabled
DOUT
0=No Data Out
1=Data Out
Port PB4-PB0 Select
0=ASCI Channel 0 Func
1=PB4-PB0 Selected
Port PB7-PB5 Select
0=RXA1, TXA1, (RXS,/CTS1)
1=PB7-PB5 Selected
Port C Select
0=ESCC Channel A Func
1=Port C Selected

Figure 54. System Configuration Register
(Z180 MPU Read/Write, Address xxEFH)

System Configuration Register

Bit 7 Port C Select
When this bit is set to 1, bit 8 parallel Port C is selected on the multiplexed pins. When this bit is reset to 0 then these multiplexed pins take ESCC™ Channel A functions.

Bit 6 PB7-PB5 Select
When this bit is set to 1, parallel Port B bits 7 through 5 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins become RxA1, TxA1 and RxS/CTS1.

Bit 5 PB4-PB0 Select
When this bit is set to 1, parallel Port B bits 4 through 0 are selected on the multiplexed pins. When this bit is reset to 0, these multiplexed pins take ASCI channel 0 functions.

Bit 4 DD$_{OUT}$ ROM Emulator Mode Enable
When this bit is set to 1, the Z182 is in "ROM emulator mode". In this mode, bus direction for certain transaction periods are set to the opposite direction to export internal bus transactions outside the Z80182/Z8L182. This allows the use of ROM emulators/logic analyzers for application development (see Tables 12a and 12b).

Note: The word "Out" means that the Z182 data bus direction is in output mode, "In" means input mode, and "Z" means high impedance. DD$_{OUT}$ stands for Data Direction Out and is the status of the D4 bit in the System Configuration Register (SCR).

Table 12a. Data Bus Direction (Z182 Bus Master)

I/O And Memory Transactions

	I/O Write to On-Chip Peripherals	I/O Read From On-Chip Peripherals	I/O Write to Off-Chip Peripherals	I/O Read From Off-Chip Peripherals	Write To Memory	Read From Mode	Refresh	Z80182 /Z8L182 Idle Mode
Z80182 /Z8L182 Data Bus (DD$_{OUT}$ =0)	Out	Z	Out	In	Out	In	Z	Z
Z80182 /Z8L182 Data Bus (DD$_{OUT}$ =1)	Out	Out	Out	In	Out	In	Z	Z

Z182 MISCELLANEOUS CONTROL AND INTERFACE REGISTERS

Bit 3 Disable ROMs
If this bit is 1, it disables the ROMCS pin. If it is 0, addresses below the ROM boundary set by the ROMBR register will cause the ROMCS pin to go Low.

Bit 2 Tri-Muxed Pins Select
The Z80182/Z8L182 has three pins that are triple multiplexed and controlled by bit 2 and bit 1. Table 14 shows the different modes.

Table 14. SCR Control for Triple Multiplexed Pins

Bit 2	Bit 1	System Configuration Register
0	0	/TEND1,TxS,CKS
0	1	/TEND1,TxS,CKS
1	0	/RTSB,(/DTR//REQB),(/W//REQB)
1	1	/HRxRDY,//HTxRDY,HINTR

Bit 1 ESCC™ Channel B/MIMIC
If this bit is 0, Mode 0 is selected.
If this bit is 1, Mode 1 is selected.

Mode 0:
Channel A ESCC Enabled
Channel B ESCC Enabled
PIA Port Enabled
16550 MIMIC Interface Disabled

Mode 1:
Channel A ESCC enabled
Channel B outputs disabled
PIA disabled
16550 MIMIC Interface Enabled

Bit 0 Daisy Chain
This bit is used to set interrupt priority of the ESCC and 16550 MIMIC interface. If it is 0, the ESCC is higher up in the daisy chain than the 16550 MIMIC interface. If it is 1, the 16550 interface is higher up than the ESCC. Note that /INT0 is used for both MIMIC and ESCC Interrupts.

/RAMCS AND /ROMCS REGISTERS

To assist decoding of ROM and RAM blocks of memory, three more registers and two pins have been added to the Z80182/Z8L182. The two pins are /ROMCS and /RAMCS. The three registers are RAMUBR, RAMLBR and ROMBR.

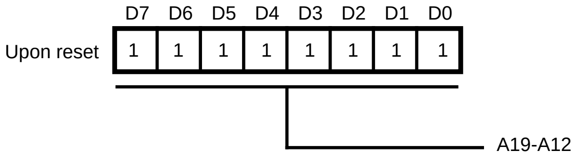


Figure 55. RAMUBR
(Z180 MPU Read/Write, Address xxE6H)

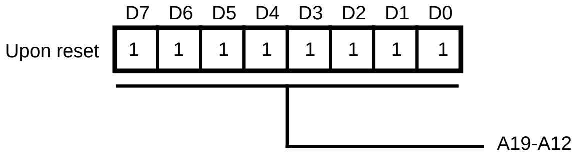


Figure 56. RAMLBR
(Z180 MPU Read/Write, Address xxE7H)

/RAMCS AND /ROMCS REGISTERS (Continued)

RAMUBR, RAMLBR RAM Upper Boundary Range, RAM Lower Boundary Range

These two registers specify the address range for the /RAMCS signal. When accessed memory addresses are less than or equal to the value programmed in the RAMUBR and greater than or equal to the value programmed in the RAMLBR, /RAMCS is asserted. The A18 signal from the CPU is taken before it is multiplexed with T_{OUT}. In the case that these registers are programmed to overlap, /ROMCS takes priority over /RAMCS (/ROMCS is asserted and /RAMCS is inactive).

Chip Select signals are going active for the address range:

/ROMCS: (ROMBR) >= A19-A12 >= 0
/RAMCS: (RAMUBR) >= A19-A12 >= (RAMLBR)

These registers are set to FFH at POR, and the boundary addresses of ROM and RAM are as follows:

ROM lower boundary address
(fixed) = 00000H

ROM upper boundary address
(ROMBR register) = 0FFFFFH

RAM lower boundary address
(RAMLBR register) = 0FFFFFH

RAM upper boundary address
(RAMUBR register) = 0FFFFFH

Because /ROMCS takes priority over /RAMCS, the latter will never be asserted until the value in the ROMBR and RAMLBR registers are re-initialized to lower values.

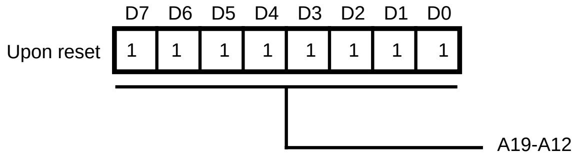


Figure 57. ROMBR
(Z180 MPU Read/Write, Address xxE8H)

ROMBR ROM Address Boundary Register

This register specifies the address range for the /ROMCS signal. When accessed, memory addresses are less than or equal to the value programmed in this register, the /ROMCS signal is asserted.

The A18 signal from the CPU is obtained before it is multiplexed with T_{OUT}. This signal can be forced to a "1" (inactive state) by setting bit 3 in the System Configuration Register, to allow the user to overlay the RAM area over the ROM area.

Z80182 Improvement to the Wait State Generator

A separate Wait State Generator is provided for access memory using /ROMCS and /RAMCS. A single 8-bit register is added to enable/disable this feature as well as provide two 3-bit fields that provide 1 to 8 waits for each chip select.

WSG Chip Select Register (Z80182 address D8H)

Bit 7	/RAMCS Wait State Generator Enable. Disable on power-up or reset.
Bits 6-4	/RAMCS Wait States 1 to 8. Eight wait states on power-up or reset.
Bit 3	/ROMCS Wait State Generator Enable. Disable on power-up or reset.
Bits 2-0	/ROMCS Wait States 1 to 8. Eight wait states on power-up or reset.

There are two wait state generators in the Z182. The actual number of wait states inserted is the greatest number of both the Z180 WSG and the chip select WSG. In order to use the Chip Select WSG, the Z180 WSG should be programmed to 0 wait states.

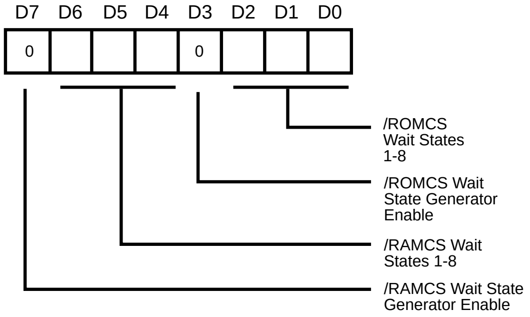

D7
D6
D5
D4
D3
D2
D1
D0
0
0
/ROMCS Wait States 1-8
/ROMCS Wait State Generator Enable
/RAMCS Wait States 1-8
/RAMCS Wait State Generator Enable

Figure 58. WSG Chip Select Register
(Z180 MPU Read/Write, Address xxD8H)

Transmit And Receive Timers (Continued)

When a write from the PC/XT/AT is made to the Transmit Holding Register, an interrupt to the Z180 MPU is generated. The Z180 MPU then reads the data in the Transmit Holding Register. Upon this read, if the Transmitter timer is enabled, the time constant from the Transmitter Time Constant Register is loaded into the Transmitter timer and enables the count. After the timer reaches a count of zero the Transmit Holding Register Empty bit is set. However, the above is only true when the PC/XT/AT is reading the Transmit Holding Register Empty bit. To allow the Z180 MPU to know that it has already read the byte of data, immediately following a read from the Transmit Holding Register, a mirrored Transmit Holding Register, Empty bit is set. This mirrored bit is always read back to the Z180 MPU when it reads the Line Status Register.

If the transmitter timer is not enabled when the Z180 MPU reads the Transmit Holding Register, both Transmit Holding Register Empty bits are set immediately. In FIFO mode of operation, the effect is similar as the status to PC is always delayed such that a PC interrupt for empty FIFO will not occur before the time required for each character read from the FIFO by the Z180 has elapsed. The effect is that the PC will not see data requests from an empty FIFO any faster than would occur with a true UART when the delay feature is enabled. This timer is also used to delay data transfer for TSR buffer to Z80182 THR in double buffer mode.

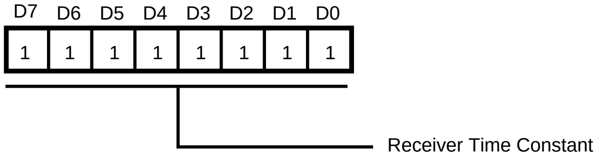


Figure 68. Receive Time Constant Register
(Z180 MPU Read/Write, Address xxFBH)

When the Z180™ MPU writes to the Receive Buffer register and the Receive Timer is enabled, the Receive Timer is loaded with the Receive Time Constant, the timer is enabled and counts down to zero. When the timer reaches zero, the Data Ready bit in the Line Status Register is set. As with the Transmit Timer, the Data Ready bit is also mirrored. Immediately upon a write to the Receive Buffer, the mirrored bit is set to let the Z180 MPU know that the byte has already been written. If the timer is not enabled, then both Data Ready bits are set immediately upon a write to the Receive Buffer. The FIFO mode of operation is similar in that the status to the PC is always delayed by the time required for each character written to the FIFO by the Z180. The effect is that the PC will not see a FIFO trigger level or DMA request faster than would occur with a true UART when the delay feature is enabled.

EMULATION MODES (Continued)

Table 21. Emulation Mode 1

Signal	Normal Mode 0	Emulation Adaptor Mode 1
PHI	Output	Input
/M1	Output	Input
/MREQ,/MRD	Output	Input
/IORQ	Output	Input
/RD	Output	Input
/WR	Output	Input
/RFSH	Output	Input
/HALT	Output	Input
ST	Output	Input
E	Output	Tri-state
/BUSACK	Output	Input
/WAIT	Input	Output
A19,A18/T_{OUT}	Output	Input
A17-A0	Output	Input
D7-D0	Input/Output	Input/Output
TxA0	Output	Tri-state
/RTS0	Output	Tri-state
TxA1	Output	Tri-state
/INT0	Input	Output, Open-Drain

Mode 2 Emulation Probe Mode

In the Emulator Probe Mode all of the Z182 output signals are tri-state. This scheme allows a Z182 emulator probe to grab on to the Z182 package leads on the target system.

Mode 3 RESERVED (for test purposes only)

This mode is reserved for test purpose only, do not use.

Notes:

Z182 has two branches of reset. /RESET controls the Z182 overall configuration, RAM and ROM boundaries, plus the ESCC, Port and the 16550 MIMIC interface. In Normal Mode, a "one shot" circuit samples the input of the /RESET pin to assert the internal reset to its proper duration. In Adapter Mode, this "one shot" circuit is bypassed. Note also that the Z180's crystal oscillator is disabled in Mode 1 and Mode 2.

In Mode 1 the emulator must provide /MREQ on the (/MREQ,/MRD) Z80182/Z8L182 pin (not /MRD); and A18 (not T_{OUT}) on the A18/T_{OUT} pin.

SLEEP, HALT EFFECT ON MIMIC AND 182 SIGNALS

The following Z80182/Z8L182 signals are driven High when Z180™ MPU enters a SLEEP or HALT state:

- /MRD when selected in the Interrupt Edge/Pin MUX Register.
- /MWR when selected in the Interrupt Edge/Pin MUX Register.
- /ROMCS,/RAMCS always High in SLEEP or HALT.

The following signals are High-Z during SLEEP and HALT:

- /IOCS when so selected in the Interrupt Edge/Pin MUX Register.
- /RD and /WR.

A0-A19 (A18 if selected) always High-Z in power down.

D0-D7 always High-Z in power down modes.

The MIMIC logic of the 182 is disabled during power down modes of the Z180.

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS} .... –0.3V to +7.0V
Voltages on all inputs
with respect to V_{SS} .... –0.3V to V_{CC} +0.3V
Operating Ambient Temperature .... 0 to +70°C
Storage Temperature ....–55°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Figure 89).

Available operating temperature range is:
S = 0°C to +70°C

Voltage Supply Range:
$+4.50V \le V_{CC} \le +5.50V$ Z80182
$+3.0V \le V_{CC} \le +3.60V$ Z8L182

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

Note: The ESCC™ Core is only guaranteed to operate at 20 MHz 5.0 volts or 10 MHz 3.3 volts. Upon reset, the Z182 system clock is "divided by one" before clocking the ESCC. When Z182 is operated above 20 MHz 5.0 volts or 10 MHz 3.3 volts, the ESCC should be programmed to "divide-by-two" mode.

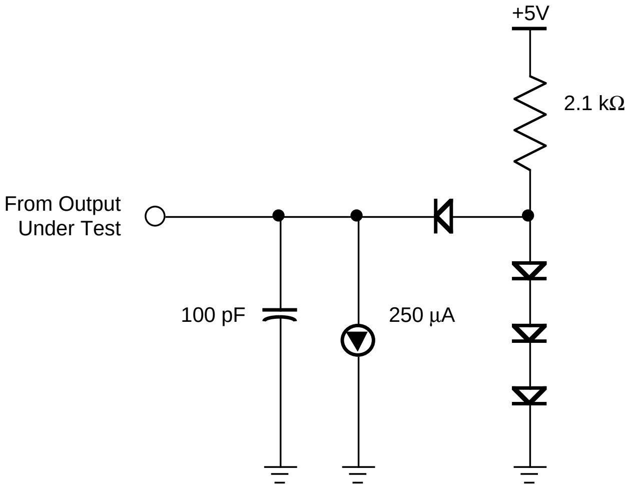


Figure 89. Test Load Diagram

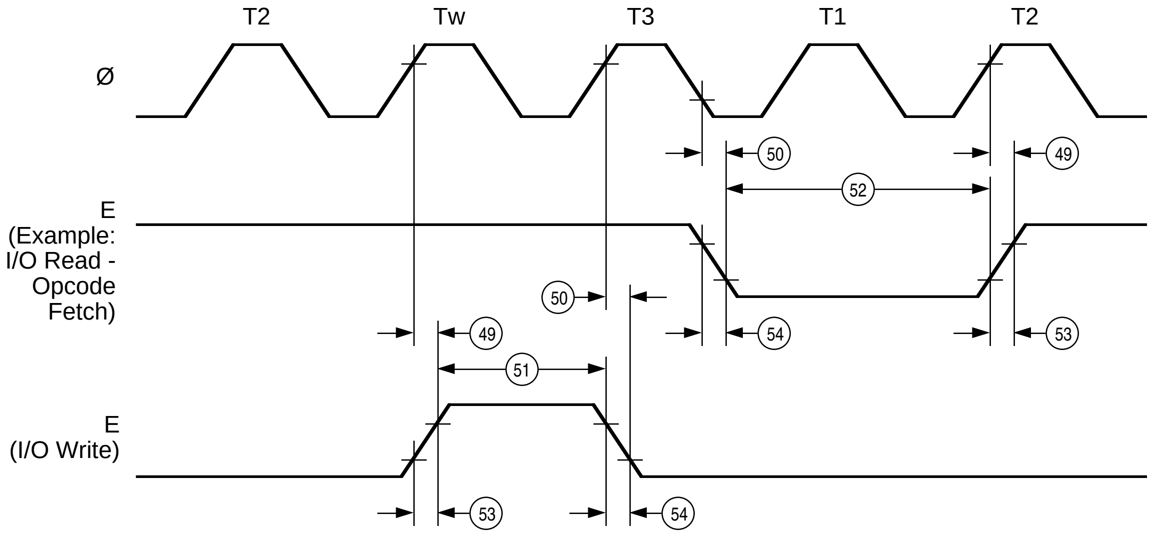

T2
Tw
T3
T1
T2
Ø
E
(Example:
I/O Read -
Opcode
Fetch)
E
(I/O Write)
49
50
51
52
53
54
50
49
54
53
53
54

Figure 96. E Clock Timing
(Minimum timing example
of PWEL and PWEH)

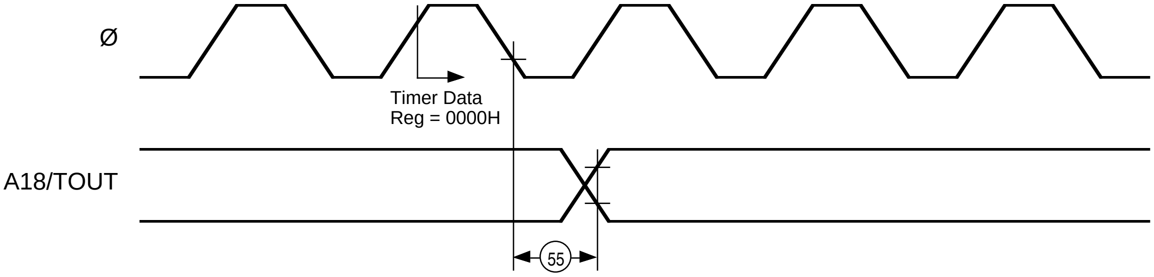

Ø
Timer Data
Reg = 0000H
A18/TOUT
55

Figure 97. Timer Output Timing

AC CHARACTERISTICS (Continued)

Z85230 General Timing Diagram

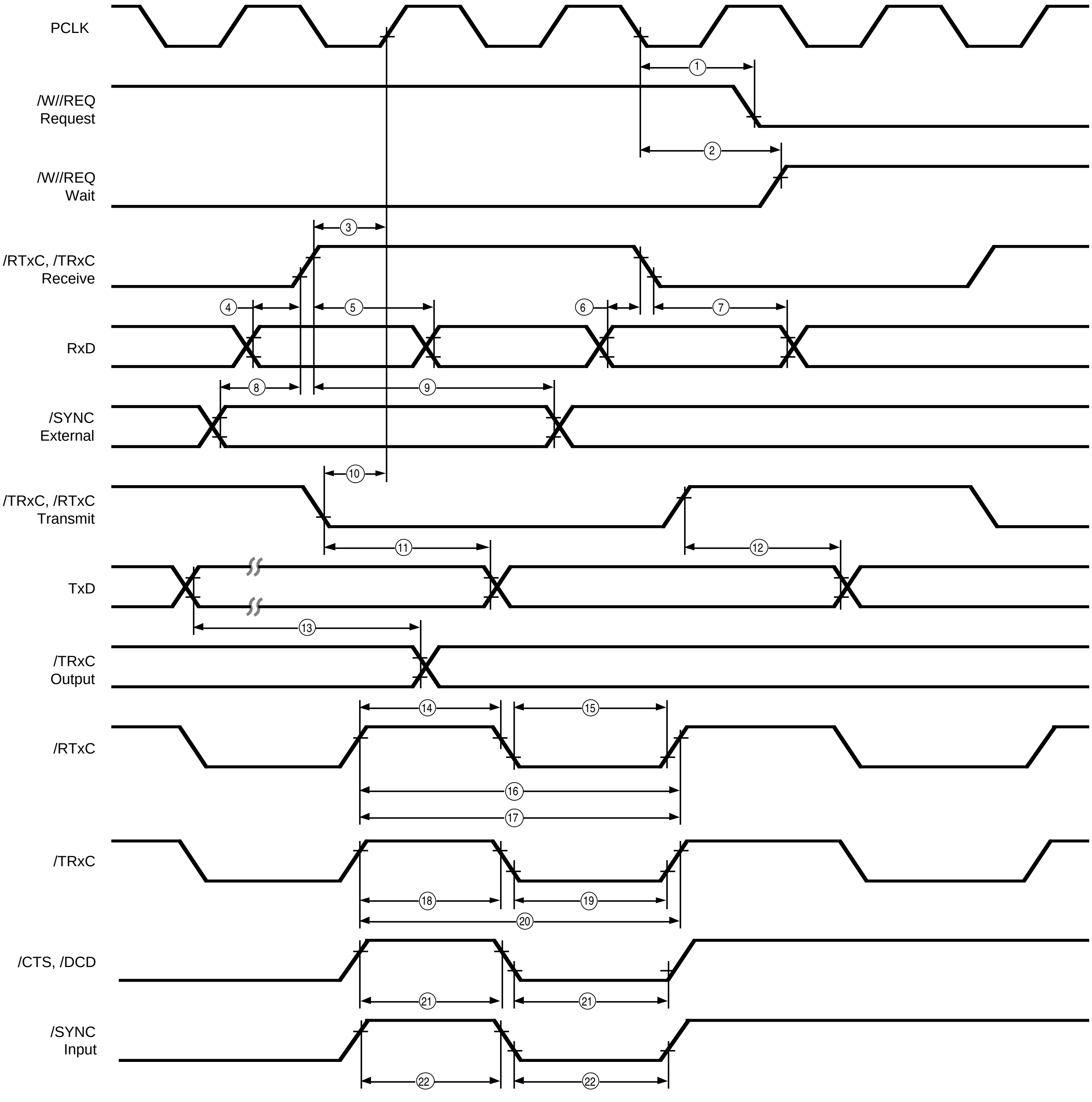

PCLK
/W//REQ Request
/W//REQ Wait
/RTxC, /TRxC Receive
RxD
/SYNC External
/TRxC, /RTxC Transmit
TxD
/TRxC Output
/RTxC
/TRxC
/CTS, /DCD
/SYNC Input
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
21
22
22

Figure 105. General Timing Diagram

AC CHARACTERISTICS (Continued)

Z85230 System Timing Diagram

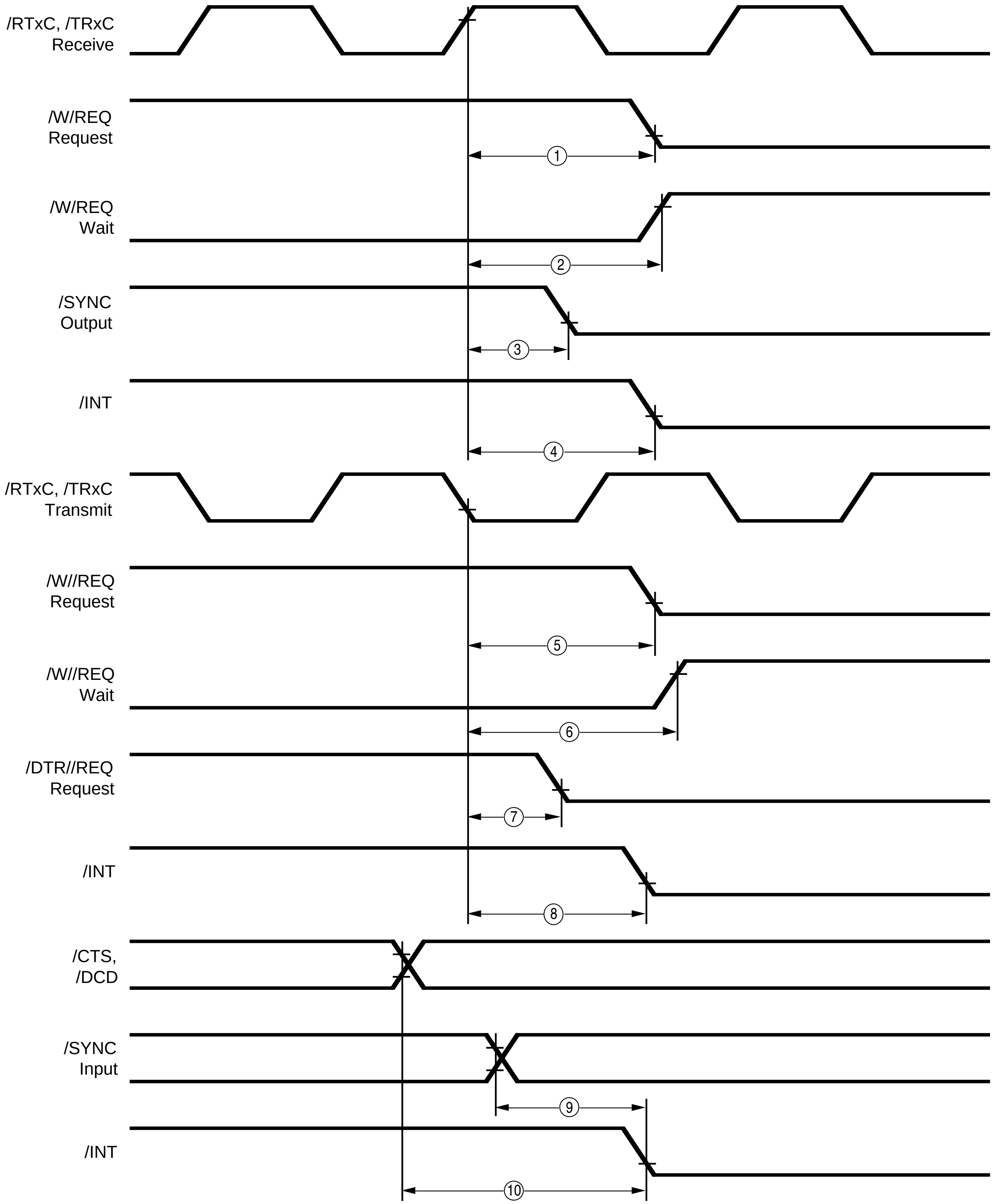

/RTxC, /TRxC Receive
/W/REQ Request
①
/W/REQ Wait
②
/SYNC Output
③
/INT
④
/RTxC, /TRxC Transmit
/W//REQ Request
⑤
/W//REQ Wait
⑥
/DTR//REQ Request
⑦
/INT
⑧
/CTS, /DCD
/SYNC Input
⑨
/INT
⑩

Figure 106. Z85230 System Timing