Zilog - Z8L18220FSC Datasheet

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	Z8S180
Number of Cores/Bus Width	1 Core, 8-Bit
Speed	20MHz
Co-Processors/DSP	-
RAM Controllers	DRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	100-QFP
Supplier Device Package	100-QFP
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8l18220fsc

Z180 MPU DMA SIGNALS

/TEND0. *Transfer End 0 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND0 is multiplexed with CKA1 on the CKA1//TEND0 pin.

/TEND1. *Transfer End 1 (output, active Low).* This output is asserted active during the last write cycle of a DMA operation. It is used to indicate the end of the block transfer. /TEND1 is multiplexed with the ESCC signal /RTSB and the 16550 MIMIC interface signal /HRxRDY on the /TEND1//RTSB//HRxRDY pin.

/DREQ0. *DMA request 0 (input, active Low).* /DREQ0 is used to request a DMA transfer from DMA channel 0. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed. /DREQ0 is multiplexed with CKA0 on the CKA0//DREQ0 pin.

/DREQ1. *DMA request 1 (input, active Low).* /DREQ1 is used to request a DMA transfer from DMA channel 1. The DMA channel monitors the input to determine when an external device is ready for a read or write operation. This input can be programmed to be either level or edge sensed.

Z180™ MPU TIMER SIGNALS

$T_{OUT.}$ *Timer Out (output, active High).* T_{OUT} is the pulse output from PRT channel 1. This line is multiplexed with A18 of the address bus on the A18/T_{OUT} pin.

Z85230 ESCC™ SIGNALS

TxDA. *Transmit Data (output, active High).* This output signal transmits channel A's serial data at standard TTL levels. This output can be tri-stated during power down modes.

TxDB. *Transmit Data (output, active High).* This output signal transmits channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1, TxDB is multiplexed with the 16550 MIMIC interface /HDDIS signal on the TxDB//HDDIS pin.

RxDA. *Receive Data (inputs, active High).* These inputs receive channel A's serial data at standard TTL levels.

RxDB. *Receive Data (input, active High).* These inputs receive channel B's serial data at standard TTL levels. In Z80182/Z8L182 mode 1 RxDB is multiplexed with the 16550 MIMIC HA1 input on the RxDB/HA1 pin.

/TRxCA. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel A program control. /TRxCA may supply the receive clock or the transmit clock in the Input mode or supply the output of the digital phase-locked loop, the crystal oscillator, the baud rate generator, or the transmit clock in the output mode.

/TRxCB. *Transmit/Receive Clock (input or output, active Low).* The functions of this pin are under channel B program control. /TRxCB may supply the receive clock or the transmit clock in the input mode or supply the output of the Digital Phase-Locked Loop (DPLL), the crystal oscillator, the baud rate generator, or the transmit clock in output mode. In Z80182/Z8L182 mode 1 /TRxCB is multiplexed with the 16550 MIMIC interface HA0 input on the /TRxCB/HA0 pin.

/RTxCA. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel A program control. In channel A, /RTxCA may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCA pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode.

/RTxCB. *Receive/Transmit Clock (input, active Low).* The functions of this pin are under channel B program control. In channel B, /RTxCB may supply the receive clock, the transmit clock, the clock for the baud rate generator, or the clock for the DPLL. This pin can also be programmed for use by the /SYNCB pin as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in asynchronous mode. In Z80182/Z8L182 mode 1 the /RTxCB signal is multiplexed with 16550 MIMIC interface HA2 input on the /RTxCB/HA2 pin.

Z85230 ESCC SIGNALS (Continued)

/SYNCA, /SYNCB. *Synchronization (inputs/outputs, active Low).* These pins can act as either inputs, outputs, or as part of the crystal oscillator circuit. In the Asynchronous Receive mode (crystal oscillator option not selected), these pins are inputs similar to /CTS and /DCD. In this mode, transitions on these lines affect the state of the Sync /Hunt status bits in Read Register 0, but have no other function. /SYNCA is also multiplexed with PC4 (parallel Port C, bit 4) on the /SYNCA/PC4 pin.

In External Synchronization mode with the crystal oscillator not selected, these lines also act as inputs. In this mode /SYNC must be driven Low two receive clock cycles after the last bit in the sync character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of /SYNC.

In the Internal Synchronization mode, (Monosync and Bisync) with the crystal oscillator not selected, these pins act as outputs and are active only during the part of the receive clock cycle in which sync characters are recognized. The sync condition is not latched, so these outputs are active each time a sync character is recognized (regardless of the character boundaries). In SDLC mode, these pins act as outputs and are valid on receipt of a flag. In Z80182/Z8L182 mode 1 the /SYNCB signal is multiplexed with the 16550 MIMIC interface /HCS input on the /SYNCB //HCS pin.

/CTSA. *Clear To Send (input, active Low).* If this pin is programmed as auto enable, a Low on this input enables the channel A transmitter. If not programmed as auto enable, it may be used as a general-purpose input. The input is Schmitt-trigger buffered to accommodate slow rise-time input. The ESCC™ detects transitions on this input and can interrupt the Z180™ MPU on either logic level transitions. /CTSA is multiplexed with PC1 (parallel Port C, bit 1) on the /CTSA/PC1 pin.

/CTSB. *Clear To Send (input, active Low).* This pin is similar to /CTSA's functionality but is applicable to the channel B transmitter. In Z80182/Z8L182 mode, the /CTSB signal is multiplexed with the 16550 MIMIC interface /HWR input on the /CTSB //HWR pin.

/DCDA. *Data Carrier Detect (input, active Low).* This pin functions as receiver enables if it is programmed as an auto enable bit; otherwise, it may be used as a general-purpose input pin. The pin is Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects transitions on this pin and can interrupt the Z180 MPU on either logic level transitions. /DCDA is also multiplexed with PC0 (parallel Port C, bit 0) on the /DCDA/PC0 pin.

/DCDB. *Data Carrier Detect (input, active Low).* This pin's functionality is similar to /DCDA but applicable to the channel B receiver. In Z80182/Z8L182 mode 1, /DCDB is multiplexed with the 16550 MIMIC interface /HRD input on the /DCDB//HRD pin.

/RTSA. *Request to Send (output, active Low).* When the Request to Send (RTS) bit in Write Register 5 channel A is set, the /RTSA signal goes Low. When the RTS bit is reset in the Asynchronous mode and auto enables is on, the signal goes High after the transmitter is empty. In Synchronous mode or in Asynchronous mode with auto enables off, the /RTSA pin strictly follows the state of the RTS bit. The pin can be used as general-purpose output. /RTSA is multiplexed with PC2 (parallel Port C bit 2). This /RTSA or PC2 combination is pin multiplexed with /MWR (active when both the internal /MREQ and /WR are active) on the /MWR/PC2//RTSA pin. The default function of this pin on power-up is /MWR which may be changed by programming bit 3 in the Interrupt Edge/Pin MUX Register (xxDFH).

/RTSB. *Request to Send (output, active Low).* This pin is similar in functionality as /RTSA but is applicable on channel B. The /RTSB signal is multiplexed with the Z180 MPU /TEND1 signal and the 16550 MIMIC interface /HRxRDY signal on the /TEND1//RTSB//HRxRDY pin.

/DTR//REQA. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. /DTR//REQA is also multiplexed with PC3 (parallel Port C, bit 3) on the /DTR//REQA /PC3 pin.

/DTR//REQB. *Data Terminal Ready (output, active Low).* This pin functions as it is programmed into the DTR bit. It can also be used as general-purpose output (transmit) or as request lines for the DMA controller. The ESCC allows full duplex DMA transfers. The /DTR//REQB signal is multiplexed with the Z180 MPU TxS signal and the 16550 MIMIC interface HINTR signal on the /TxS//DTR//REQB //HINTR pin.

/W//REQA. *Wait/Request (output, open drain when programmed for the Wait function, driven High or Low when programmed for a Request function).* This dual-purpose output can be programmed as Request (receive) lines for a DMA controller or as Wait lines to synchronize the Z180 MPU to the ESCC data rate. The reset state is Wait. The ESCC allows full duplex DMA transfers. /W//REQA is also multiplexed with PC5 (parallel Port C, bit 5) on the /W//REQA/PC5 pin.

EMULATION SIGNALS

EV1, EV2. *Emulation Select (input).* These two pins determine the emulation mode of the Z180 MPU (Table 1).

Table 1. Evaluation Modes

Mode	EV2	EV1	Description
0	0	0	Normal mode, on-chip Z180 bus master
1	0	1	Emulation Adapter Mode
2	1	0	Emulator Probe Mode
3	1	1	Reserved for Test

SYSTEM CONTROL SIGNALS

ST. *Status (output, active High).* This signal is used with the /M1 and /HALT output to decode the status of the CPU machine cycle. If unused, this pin should be pulled to V_{DD}.

/RESET. *Reset Signal (input, active Low).* /RESET signal is used for initializing the MPU and other devices in the system. It must be kept in the active state for a period of at least three system clock cycles.

IEI. *Interrupt Enable Signal (input, active High).* IEI is used with the IEO to form a priority daisy chain when there is more than one interrupt-driven peripheral.

IEO. *Interrupt Enable Output Signal (output, active High).* In the daisy-chain interrupt control, IEO controls the interrupt of external peripherals. IEO is active when IEI is 1 and the CPU is not servicing an interrupt from the on-chip peripherals. This pin is multiplexed with /IOCS on the /IOCS/IEO pin. The /IOCS function is the default on Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/IOCS. *Auxiliary Chip Select Output Signal (output, active Low).* This pin is multiplexed with /IEO on the /IOCS/IEO pin. /IOCS is an auxiliary chip select that decodes A7, A6, /IORQ, /M1 and effectively decodes the address space xx80H to xxBFH for I/O transactions. A15 through A8 are not decoded so that the chip select is active in all pages of I/O address space. The /IOCS function is the default on the /IOCS/IEO pin after Power On or Reset conditions and is changed by programming bit 2 in the Interrupt Edge/Pin MUX Register.

/RAMCS. *RAM Chip Select (output, active Low).* Signal used to access RAM based upon the Address and the RAMLBR and RAMUBR registers and /MREQ.

/ROMCS. *ROM Chip Select (output, active Low).* Signal used to access ROM based upon the address and the ROMBR register and /MREQ.

E. *Enable Clock (output, active High).* Synchronous machine cycle clock output during bus transactions.

XTAL. *Crystal (input, active High).* Crystal oscillator connection. This pin should be left open if an external clock is used instead of a crystal. The oscillator input is not a TTL level (reference DC characteristics).

EXTAL. *External Clock/Crystal (input, active High).* Crystal oscillator connections to an external clock can be input to the Z80180 on this pin when a crystal is not used. This input is Schmitt triggered.

PHI. *System Clock (output, active High).* The output is used as a reference clock for the MPU and the external system. The frequency of this output is reflective of the functional speed of the processor. In clock divide-by-two mode, the pHI frequency is half that of the crystal or input clock. If divide-by-one mode is enabled, the PHI frequency is equivalent to that of crystal or input frequency. The PHI frequency is also fed to the ESCC core. If running over 20 MHz (5V) or 10 MHz (3V) the PHI-ESCC frequency divider should be enabled to divide the PHI clock by two prior to feeding into the ESCC core.

Ports B and C Multiplexed Pin Descriptions

Ports B and C are pin multiplexed with the Z180 ASCI functions and part of ESCC channel A. The MUX function is controlled by bits 7-5 in the System Configuration Register. The MUX is organized as shown in Table 4.

Table 4. Multiplexed Port Pins

Port Mode Function	ASCI/ESCC Mode Function
PB7	RxS,/CTS1
PB6 Select with bit 6=1	RxA1
PB5 System Config Reg.	TxA1
PB4	RxA0
PB3	TxA0
PB2 Select with bit 5=1	/DCD0
PB1 System Config Reg.	/CTS0 (Note 1)
PB0	/RTS0
PC7	Always Reads /INT2 Ext. Status
PC6	Always Reads /INT1 Ext. Status
PC5	/W//REQA
PC4	/SYNCA
PC3 Select with bit 7=1	/DTR//REQA
PC2 System Config Reg.	/RTSA (Note 2)
PC1	/CTSA
PC0	/DCDA

Note 1:
When the Port function (PB1) is selected, the internal Z180/CTS0 is always driven Low. This ensures that the ASCI channel 0 of the Z180™ MPU is enabled to transmit data.

Note 2:
Interrupt Edge /Pin MUX register, bit 3 chooses between the /MWR or PC2//RTSA combination; the System Configuration Register bit 7 chooses between PC2 and /RTSA.

Refer to Table 5 for the 1st, 2nd and 3rd pin functions.

Z80182 MIMIC DOUBLE BUFFERING FOR THE TRANSMITTER

The Z80182 Rev DA implements double buffering for the transmitter in 16450 mode and sets the TEMT bit in the LSR Register automatically.

When this feature is enabled and character delay emulation is being used (see Figure 9):

1. The PC THRE bit in the LSR Register is set when the THR Register is empty;
2. PC Host writes to the 16450 THR Register;
3. Whenever the Z80182 TSR buffer is empty and one character delay timer is in a timed-out state, the byte from the THR Register is transferred to the TSR buffer; the timer is in timed-out state after FIFO Reset or after Host TEMT is set. This allows a dual write to THR when Host TEMT is set.
4. Restart character delay timer (timer reloads and counts down) with byte transfer from THR Register to the TSR buffer;
5. Whenever the TSR buffer is full, the TEMT bit in MPU LSR Register is reset with no delay;
6. MPU reads TSR buffer;
7. TEMT bit in LSR Register for MPU is set with no delay whenever the TSR buffer is empty;
8. When the TSR buffer is read by MPU and THR Register is empty and one character delay timer reaches zero, the TEMT bit in the LSR Register for Host is set from 0 to 1.

The PC THRE bit in the LSR Register is reset whenever the THR Register is full and set whenever THR Register is empty.

MPU IREQ and DMA Request for the transmit data is trigger whenever TSR buffer is full and cleared whenever TSR buffer is empty.

If character delay emulation is not used the TEMT bit in the LSR Register is set whenever both the THR Register and the TSR buffer are both empty. The Host TEMT bit is clear if there is data in either the TSR buffer of THR Register.

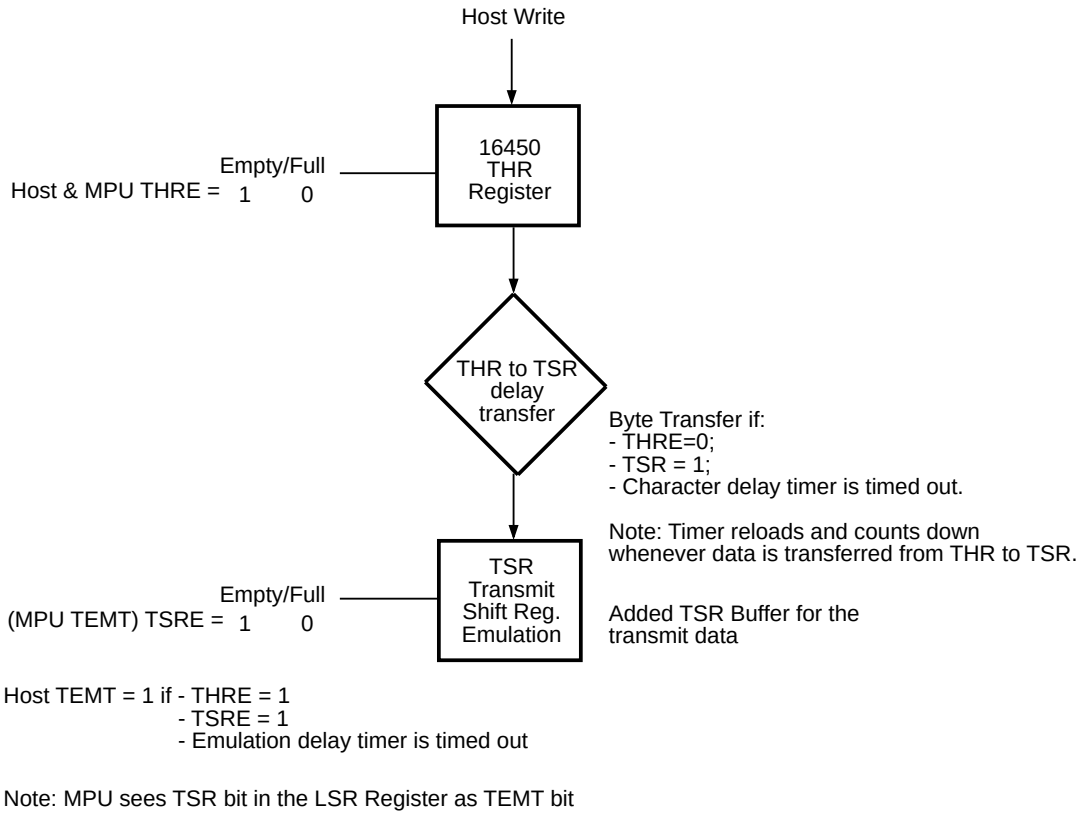
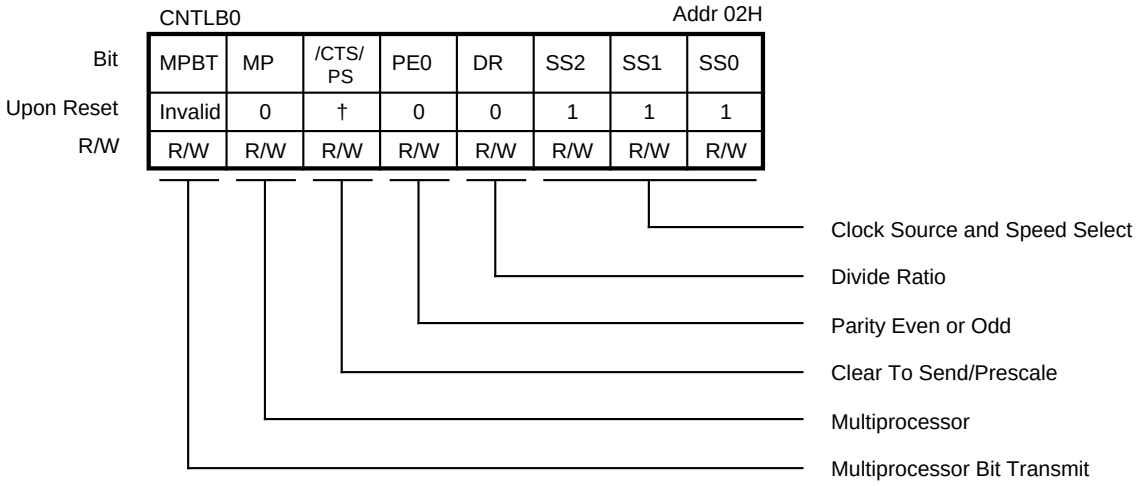


Figure 9. TEMT Emulation Logic Implementation



† /CTS - Depending on the condition of /CTS pin.
PS - Cleared to 0.

General Divide Ratio	PS = 0 (Divide Ratio = 10)		PS = 1 (Divide Ratio = 30)	
SS, 2, 1, 0	**DR = 0 (x16)**	**DR = 1 (x64)**	**DR = 0 (x16)**	**DR = 1 (x64)**
000	Ø ÷ 160	Ø ÷ 640	Ø ÷ 480	Ø ÷ 1920
001	Ø ÷ 320	Ø ÷ 1280	Ø ÷ 960	Ø ÷ 3840
010	Ø ÷ 640	Ø ÷ 2580	Ø ÷ 1920	Ø ÷ 7680
011	Ø ÷ 1280	Ø ÷ 5120	Ø ÷ 3840	Ø ÷ 15360
100	Ø ÷ 2560	Ø ÷ 10240	Ø ÷ 7680	Ø ÷ 30720
101	Ø ÷ 5120	Ø ÷ 20480	Ø ÷ 15360	Ø ÷ 61440
110	Ø ÷ 10240	Ø ÷ 40960	Ø ÷ 30720	Ø ÷ 122880
111	External Clock (Frequency < Ø ÷ 40)			

Figure 11. ASCI Control Register B (Ch. 0)

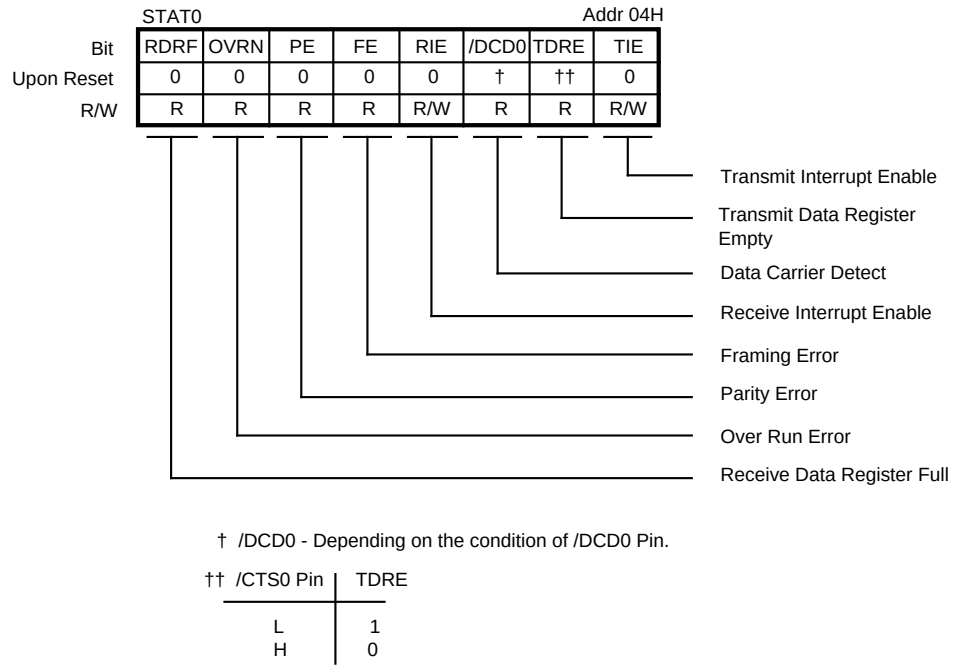


Figure 13. ASCI Status Register

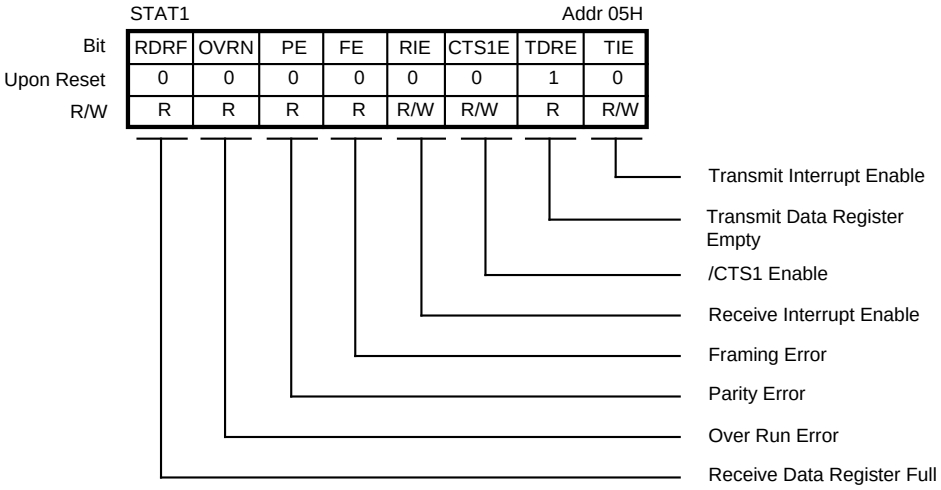


Figure 14. ASCI Status Register (Ch. 1)

ASCI CHANNELS CONTROL REGISTERS (Continued)

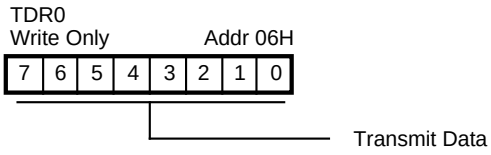


Figure 15. ASCI Transmit Data Register (Ch. 0)

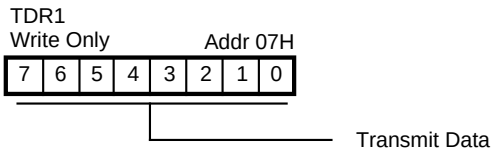


Figure 16. ASCI Transmit Data Register (Ch. 1)

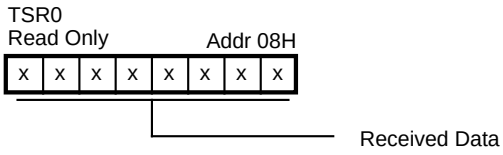


Figure 17. ASCI Receive Data Register (Ch. 0)

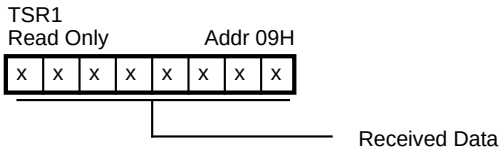


Figure 18. ASCI Receive Data Register (Ch. 1)

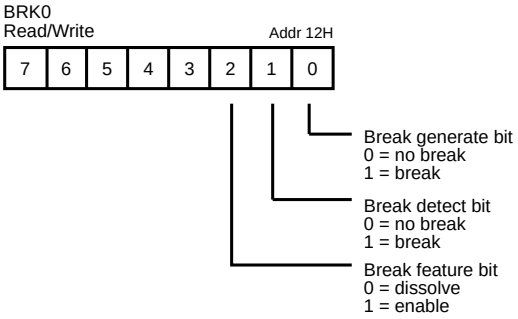


Figure 19. ASCI Break Control Register (Ch. 0)

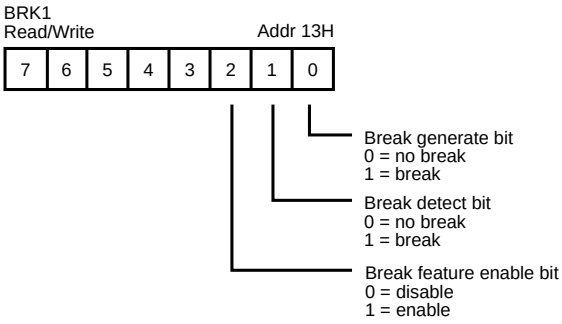


Figure 20. ASCI Break Control Register (Ch. 1)

Z85230 ESCC™ CONTROL REGISTERS

See Figures 52 and 53 for the ESCC Control registers. For additional information, refer to the ESCC Product Specification /Technical Manual.

The Z80182/Z8L182 has two ESCC channels. They can be accessed in any page of I/O space since only the lowest eight address lines are decoded for access. Their Z180™ MPU Address locations are shown in Table 11.

When the 16550 MIMIC interface is enabled, ESCC channel B is disconnected from the output pins. The channel B /TRxCB clock is connected to the Transmit and Receive timers of the 16550 MIMIC interface. ***It is recommended that /TRxCB be programmed as an output with proper baud rate values to timeout the transmitter and receiver of the 16550 MIMIC interface.***

Table 11. ESCC Control and Data Map

ESCC Channel A	Control	Z180 MPU Address xxE0H
	Data	Z180 MPU Address xxE1H
ESCC Channel B	Control	Z180 MPU Address xxE2H
	Data	Z180 MPU Address xxE3H

CONTROL REGISTERS (Continued)

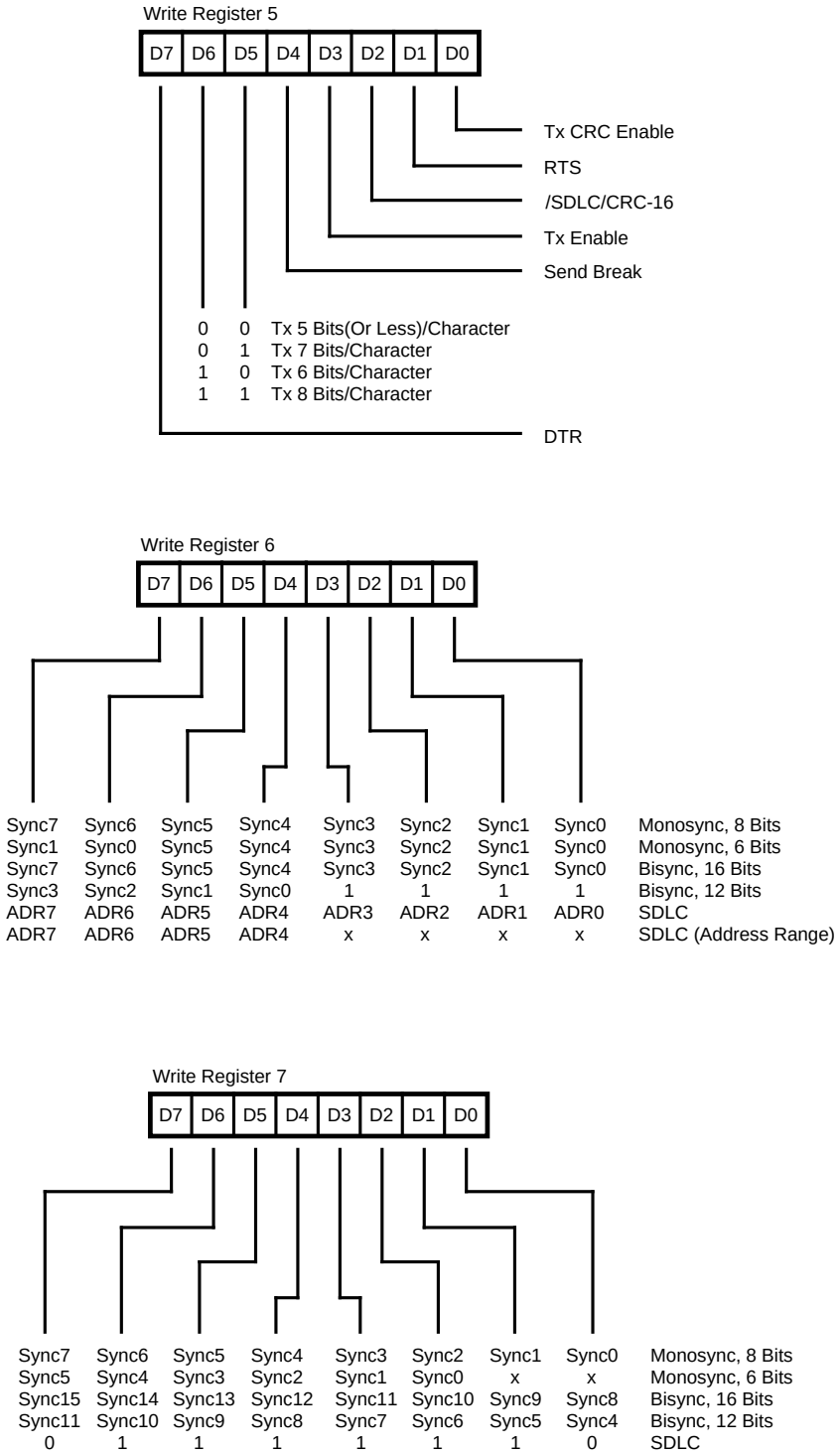


Figure 52. Write Register Bit Functions (Continued)

Bit 0 16450 MIMIC Mode Enable
(Reset value=0) This bit = 1 will force the mimic into 16450 mode. Bit 0 in the FCR reg is forced to zero as well as the mimic internal FIFO enable. When used, this bit should be programmed at MIMIC initialization and not modified afterwards.

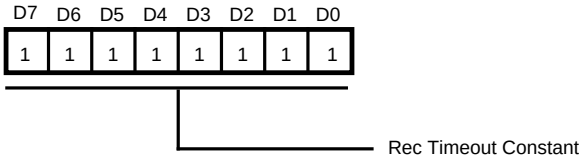


Figure 65. Receive Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEAH)

This register contains an 8-bit constant for emulation of the 16550 four character timeout feature. Software must determine the value to load into this register based on the bit rate and word length specified by the MIMIC interface with the PC. This timer receives its input from the /TRxCB Clock of the ESCC. This timer is enabled to down count when the enable bit in the FSR register is set and the trigger level interrupt has not been activated on the RCVR FIFO. The counter reloads and counts down each time there is a read or write to the RCVR FIFO.

The receive timeout timer is enhanced to emulate the actual 16550 when bit 1 of the FIFO status and control register is enabled. Under most circumstances, this register should be programmed for four character timers (40d, 8-N-1).

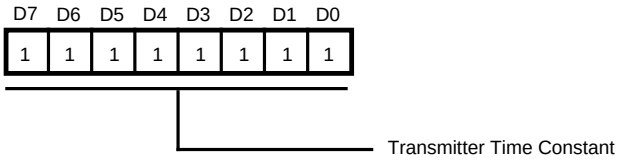


Figure 66. Transmit Timeout Timer Constant
(Z180 MPU Read/Write, Address xxEBH)

This register contains an 8-bit constant for determining the interval for the Transmit Timeout Timer. If allowed to decrement to zero, this timer interrupts the MPU by setting the THR bit in the IUS/IP register. This timer receives its input from the /TRxCB Clock of the SCC. The timer is enabled to down count when the enable bit in the FSR register is set and the trigger level has not been reached on the XMIT FIFO. The counter reloads each time there is a read or write to the XMIT FIFO.

Transmit And Receive Timers

Because of the speed at which data transfers can take place between the Z180™ MPU and the PC/XT/AT, two timers have been added to alleviate any software problems that a high speed parallel data transfer might cause. These timers allow the programmer to slow down the data transfer just as if the 16550 MIMIC interface had to shift the data in and out serially. The Timers receive their input from the /TRxCB Clock since, in 16550 MIMIC mode, the ESCC channel B is disabled. For example, the clock source for the 8-bit registers: RTTC (Receive Timeout Time Constant, xxEAH), TTTC (Transmit Timeout Time Constant, xxEBH), TTCR (Transmit Time Constant Register, xxFAH) and RTCR (Receive Time Constant Register, xxFBH) uses the /TRxCB Clock output. The /TRxCB Clock output needs to be generated by the ESCC's channel B's 16-bit BRG as its clock source, thus allowing the programmer to access a total of 24 bits as a timer to slow down the data transfer.

In most cases, ESCC Ch. B BRG should be programmed to output at a frequency equivalent to the desired serial transfer rate. The output of the BRG should be routed to the /TRxCB pin.

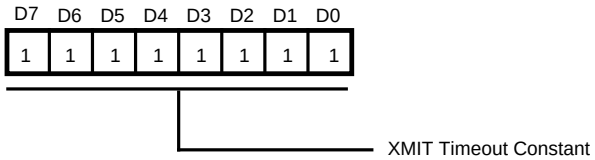


Figure 67. Transmitter Time Constant Register
(Z180 MPU Read/Write, Address xxFAH)

16550 MIMIC REGISTERS (Continued)

FIFO Control Register

Bit 6 and Bit 7 RCVR trigger LSB and MSB bits
This 2-bit field determines the number of available bytes in the receiver FIFO before an interrupt to the PC occurs (see Table 18).

Bit 4 and Bit 5
Reserved for future use (PC side). Note: From the MPU side, bit 4 and bit 5 flags two sources of interrupts. Bit 5 is a FIFO interrupt indicating that the FCR had changed; bit 4 is a Tx overrun interrupt, indicating transmit overrun. A read of the FCR from the MCU side will clear a previously set bit 4 or bit 5.

Bit 3 DMA mode select
Setting this bit to 1 will cause the MIMIC DMA mode to change from mode 0 to mode 1 (if bit 0 is 1, FIFO mode is enabled). This affects the DMA mode of the FIFO. A 1 in this bit enables multi-byte DMA).

Bit 2 XMIT FIFO Reset
Setting this bit to 1 will cause the transmitter FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing; however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 1 RCVR FIFO Reset
Setting this bit to 1 will cause the receiver FIFO pointer logic to be reset; any data in the FIFO will be lost. This bit is self clearing, however a shadow bit exists that is cleared only when read by the Z180 MPU, allowing the MPU to monitor a FIFO reset by the PC.

Bit 0 FIFO Enable
The PC writes this bit to logic 1 to put the 16550 MIMIC into FIFO mode. This bit must be 1 when writing to the other bits in this register or they will not be programmed. When this bit changes state, any data in the FIFO's or transmitter holding and Receive Buffer Registers is lost and any pending interrupts are cleared. This feature can be forced in a disabled state by the MPU.

Table 18. Receive Trigger Level

b7	b6	Trigger Level, Number of Bytes
0	0	1
0	1	4
1	0	8
1	1	14

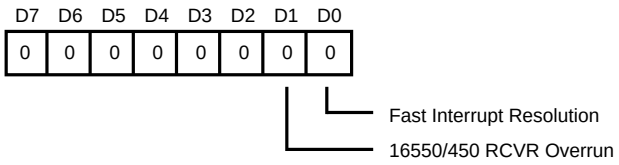


Figure 72. MIMIC Modification Register
(Z180 MPU Write only, Address xxE9h)

Bit 7-2 Reserved. Program to zero.

Bit 1 RCVR Overrun Modification
The actual 16450/16550 device allows the last position in FIFO to be overwritten by DCE during receiver overrun condition. When this bit is enabled (programmed to 1) the last position in FIFO can be overwritten by Z180 during receiver overrun. This feature is disabled by default. When this modification is not enabled, the MIMIC will ignore any write to RBR during an overrun condition.

Bit 0 Fast MIMIC-ESCC Interrupt Resolution
When enabling this modification, the internal MIMIC IEO signal into the ESCC IEI input is forced Low when the MIMIC Interrupt line becomes active. This is required to prevent the ESCC from putting it's vector on the databus during an INTACK cycle (given that the MIMIC is programmed to have higher interrupt priority).

When disabled, the internal MIMIC IEO becomes deasserted only after an interrupt acknowledge cycle. In this case, it is possible for the ESCC to force it's interrupt vector onto the data bus even when the MIMIC has a pending interrupt and is higher in priority.

16550 MIMIC REGISTERS (Continued)

Line Status Register

Bit 7 Error in RCVR FIFO
In 16450 mode, this bit will read logic 0. In 16550 mode this bit is set if at least one data byte is available in the FIFO with one of its associated error bits set. This bit will clear when there are no more errors (or break detects) in the FIFO.

Bit 6 Transmitter Empty
This bit must be set or reset by the MPU by a write to this register bit. If Double Buffer Mode is enabled, the TEMT bit is set/reset automatically. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 5 Transmit Holding Register Empty, THRE
This bit is set to 1 when either the THR has been read (emptied) by the MPU (16450 mode) or the XMIT FIFO is empty (16550 mode). This bit is set to 0 when either the THR or XMIT FIFO become non-empty. A shadow bit exists so that the register bit setting to 1 is delayed by the Transmitter Timer if enabled. The MPU when reading this bit will not see the delay. Both shadow and register bits are cleared when the PC writes to the THR of XMIT FIFO. The function of this bit is modified when TEMT/Double Buffer enhancement is selected. Refer to page 3-26 for TEMT/Double Buffer information.

Bit 2, 3, 4 Parity Error, Framing Error, Break Detect
These bits are written, indirectly, by the MPU as follows: The bits are first written to shadow bit locations when the MPU write accesses the LSR. When the next character is written to the Receive Buffer or RCVR FIFO, the data in the shadow bits is then copied to the LSR (16450 mode) or FIFO RAM (16550 mode). In FIFO mode bits become available to the PC when the data byte associated with the bits is next to be read (top of FIFO). In FIFO mode, with successive reads of the receiver, the status bits will be set if an error occurs on any byte. Once the MPU writes to the Receive Buffer or RCVR FIFO, the shadow bits are auto cleared. The register bits are cleared upon the PC reading the LSR. In FIFO mode these bits will be set if any byte has the respective error bit set while the PC reads multiple characters from the FIFO.

Bit 1 Overrun Error
This bit is set if the Z180 MPU makes a second write to the Receive Buffer before the PC reads the data in the Buffer (16450 mode) or with a full RCVR FIFO (16550 mode.) No data will be transferred to the RCVR FIFO under these circumstances. This bit is reset when the PC reads the Line Status Register.

Bit 0 Data Ready
This bit is set to 1 when received data is available, either in the RCVR FIFO (16550 mode) or Receive Buffer Register (16450 mode). This bit is set immediately upon the MPU writing data to the Receive Buffer or FIFO if the Receive Timer is not enabled but is delayed by the timer interval if the Receive Timer is enabled. For MPU read access a shadow bit exists so that the MPU does not see the delay the PC does. Both bits are cleared to logic zero immediately upon reading all the data in either the Receive Buffer or FIFO.

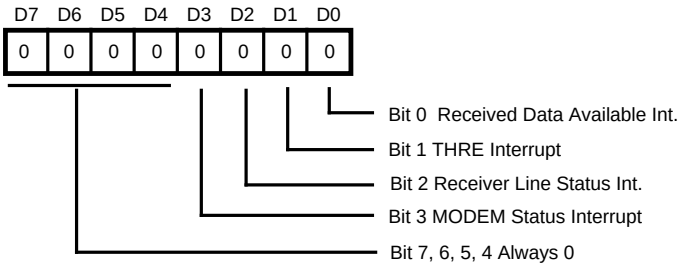


Figure 75. Interrupt Enable Register
(PC Read/Write, Address 01H)
(Z180 MPU Read Only, Address xxF1H)

Interrupt Enable Register

Bits 7, 6, 5, 4 Reserved
These bits will always read 0 (PC and MPU).

Bit 3 Modem Status IRQ
If bits 0, 1, 2 or 3 of the Modem Status Register are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 2 Receive Line Status IRQ
If bits 1, 2, 3 or 4 of the LSR are set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 1 Transmit Holding Register Empty IRQ
If bit 5 of the LSR is set and this enable bit is a logic 1, then an interrupt to the PC is generated.

Bit 0 Received Data Available IRQ
If bit 0 of the LSR is set or a Receive Timeout occurs and this enable bit is a logic 1, then an interrupt to the PC is generated.

The data direction register determines which are inputs and outputs in the PC Data Register. When a bit is set to 1 the corresponding bit in the PC Data Register is an input. If the bit is 0, then the corresponding bit is an output.

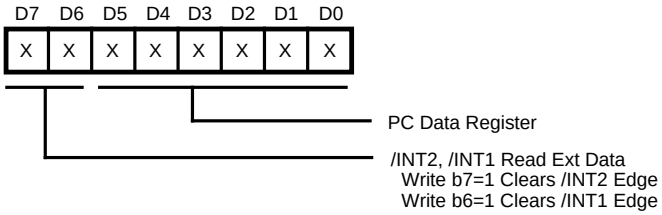


Figure 88. PC, Port C, Data Register
(Z180 MPU Read/Write, Address xxDEH)

When the Z180 MPU writes to the PC Data Register, the data is stored in the internal buffer. The values of Port C data register are undefined after reset. Any bits that are output are then sent on to the output buffers.

When the Z180 MPU reads the PC Data Register, the data on the external pins is returned.

Bits 6 and 7 serve the special function of reading the value of the external /INT2 and /INT1 lines. When operating either /INT2 or /INT1 in edge detection mode, the edge detect latch is reset by writing a 1 to bit 6 or 7 respectively. Writing a 0 has no effect. ***These latches should be reset at the end of an /INT1 or /INT2 interrupt service routine when using edge-triggered interrupt modes.***

16550 MIMIC INTERFACE DMA

The 16550 MIMIC is also able to do direct DMA with the PC/XT/AT. DMA is enabled by setting bits 3, 4 and 5 of the Master Control Register. DMA is accomplished by using the two DMA pins and the Transmitter Holding and Receive Data Registers.

If bit 5 is 1, the /HTxRDY pin is equal to the complement of the Transmit Holding Register Empty bit. If bit 5 is 1 and bit 3 is 0 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement of the Transmit Holding Register Empty Shadow bit. If bit 5 is 1 and bit 3 is 1 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Transmit Holding Register Empty Shadow bit.

If bit 4 is 1, then the /HRxRDY pin is equal to the complement of the Data Ready bit. If bit 4 is 1 and bit 3 is 0 the external /DREQ0 pin of the Z180 MPU is disabled and the internal /DREQ0 is equal to the complement of the Data Ready Shadow bit. If bit 4 is 1 and bit 3 is 1 the external /DREQ1 pin of the Z180 MPU is disabled and the internal /DREQ1 is equal to the complement or the Data Ready Shadow bit.

Z80182/Z8L182 MIMIC DMA CONSIDERATIONS

For the PC Interface, the 16550 device has two modes of operation that need to be supported by the MIMIC. In single transfer mode, the DMA request line for the receiver goes active whenever there is at least one character in the RCVR FIFO. For the transmitter, the DMA request line is active on an empty XMIT FIFO and inactive on non-empty.

In multi-transfer mode, the RCVR DMA goes active at the trigger level and inactive on RCVR FIFO empty. The XMIT DMA is active on non-full XMIT FIFO and inactive on a full XMIT FIFO.

Bit 3 in the FCR controls the DMA mode for the PC interface. If a 1 is programmed into this bit, multi-byte DMA is enabled. A 0 in this bit (default) enables single byte DMA.

As specified, the 16550 does not have any means of handling the error status bits in the FIFO in this multi-transfer mode. Such DMA transfers would require blocks with some checksum or other error checking scheme.

For the MPU interface, the DMA is controlled by a non-empty transmit FIFO and by a non-full receive FIFO conditions (THRE and the DR bits in the LSR). If the delay timers are enabled, the respective shadow bits are used for DMA control. The effect of the DMA logic is to request DMA service when at least one byte of data is available to be read or written to the FIFO's by the Z180. The Z180's DMA channel can be programmed to trigger on edge or on level.

EMULATION MODES

The Z80182/Z8L182 provides four modes of operation. The modes are selected by the EV1 and EV2 pins. These four modes allow the system development and commercial production to be done with the same device. The four emulation modes are shown in Table 20.

Table 20. EV2 and EV1, Emulation Mode Control

	EV2	EV1	EV Description
Mode 0	0	0	Normal Mode, on-chip Z180 bus master
Mode 1	0	1	Emulation Adapter Mode
Mode 2	1	0	Emulator Probe Mode
Mode 3	1	1	RESERVED, for Test Use Only

Mode 0 Normal Mode

This is the normal operating mode for the Z80182/Z8L182.

Mode 1 Emulation Adapter Mode

The Emulation Adaptor Mode enables system development for the Z182 with a readily available Z180 emulator. The Emulator provides the Z180™ MPU and Z180 peripheral functions to the target system, with their signals passing through the emulation adapter. In Emulation Adaptor Mode the Z182s, Z180 MPU and Z180 peripheral signals are tri-state or physically disconnected. The Z182 continues to provide its ESCC, MIMIC, chip select, and Port functions and signals to the target system. The Mode 1 effects on the Z182 are shown in Table 21. Note that INT1-2 Edge Detect Logic cannot be used in Emulation Adaptor EV Mode 2.

ABSOLUTE MAXIMUM RATINGS

Voltage on V_{CC} with respect to V_{SS} ..... –0.3V to +7.0V
Voltages on all inputs
with respect to V_{SS} ..... –0.3V to V_{CC} +0.3V
Operating Ambient Temperature ..... 0 to +70°C
Storage Temperature .....–55°C to +150°C

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

The DC Characteristics and capacitance sections below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND (0V). Positive current flows into the referenced pin (Figure 89).

Available operating temperature range is:
S = 0°C to +70°C

Voltage Supply Range:
+4.50V ≤ V_{CC} ≤ + 5.50V Z80182
+3.0V ≤ V_{CC} ≤ + 3.60V Z8L182

All AC parameters assume a load capacitance of 100 pF. Add 10 ns delay for each 50 pF increase in load up to a maximum of 150 pF for the data bus and 100 pF for address and control lines. AC timing measurements are referenced to 1.5 volts (except for clock, which is referenced to the 10% and 90% points). Maximum capacitive load for CLK is 125 pF.

Note: The ESCC™ Core is only guaranteed to operate at 20 MHz 5.0 volts or 10 MHz 3.3 volts. Upon reset, the Z182 system clock is "divided by one" before clocking the ESCC. When Z182 is operated above 20 MHz 5.0 volts or 10 MHz 3.3 volts, the ESCC should be programmed to "divide-by-two" mode.

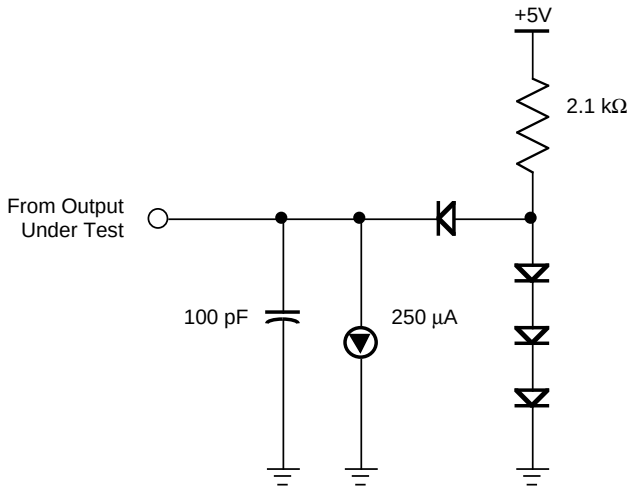


Figure 89. Test Load Diagram

DC CHARACTERISTICS

Z80182/Z8L182

(V_{CC} = 3.3V ±10%, V_{SS} = 0V, over specified temperature range unless otherwise notes.)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
V_{IH1}	Input H Voltage /RESET, EXTAL, NMI	V_{CC} –0.6		V_{CC} +0.3	V	
V_{IH2}	Input H Voltage Except /RESET, EXTAL, NMI	2.0		V_{CC} +0.3	V	
V_{IL1}	Input L Voltage /RESET, EXTAL, NMI	–0.3		0.6	V	
V_{IL2}	Input L Voltage Except /RESET, EXTAL, NMI	–0.3		0.8	V	
V_{OH1}	Output H Voltage All outputs	2.15			V	I_{OH} = –200 µA
V_{OH2}	Output H PHI	V_{CC} –0.6			V	I_{OH}= –200 µA
V_{OL1}	Output L Voltage All outputs			0.40	V	I_{OL} = 2.2 mA
V_{OL2}	Output L PHI			0.40	V	I_{OL}= 2.2 mA
I_{IL}	Input Leakage Current All Inputs Except XTAL, EXTAL			10	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{TL}	Tri-state Leakage Current			10	µA	V_{IN} = 0.5 - V_{CC} –0.5
I_{CC}*	Power Dissipation* (Normal Operation)		40	80	mA	f = 20 MHz
	Power Dissipation* (SLEEP)		TBD	TBD	mA	f= 20 MHz
	Power Dissipation* (I/O STOP)		TBD	TBD	mA	f= 20 MHz
	Power Dissipation* (SYSTEM STOP mode)		4	8	mA	f = 20 MHz
	IDLE Mode		TBD	TBD	mA	f = 20 MHz
	STANDBY Mode		50		µA	f = 0 MHz †
Cp	Pin Capacitance			12	pF	V_{IN} = 0V, f = 1 MHz T_A = 25°C

Notes:

These I_{CC} values are preliminary and subject to change without notice.

* V_{IH} Min = V_{CC} -1.0V, V_{IL} Max = 0.8V (all output terminals are at no load)
V_{CC} = 3.3V

† Device may take up to two seconds before stabilizing to steady state current.

TIMING DIAGRAMS (Continued)

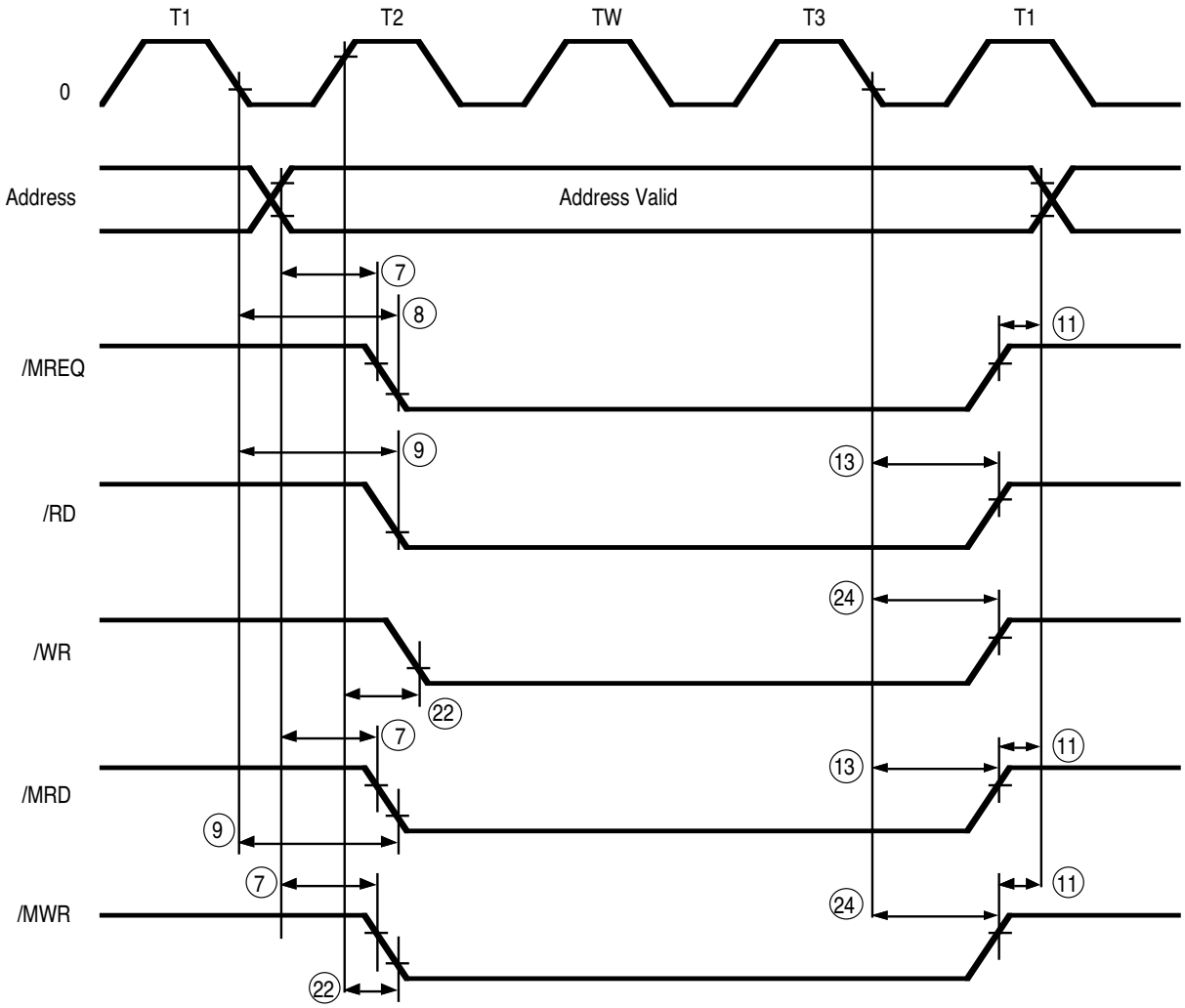


Figure 101. /MWR and /MRD Timing

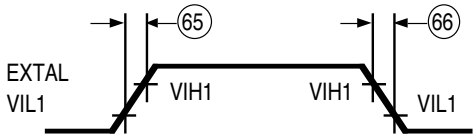


Figure 102. External Clock Rise Time and Fall Time

Figure 103. Input Rise and Fall Time
(Except EXTAL, /RESET)

Read Write External Bus Master Timing

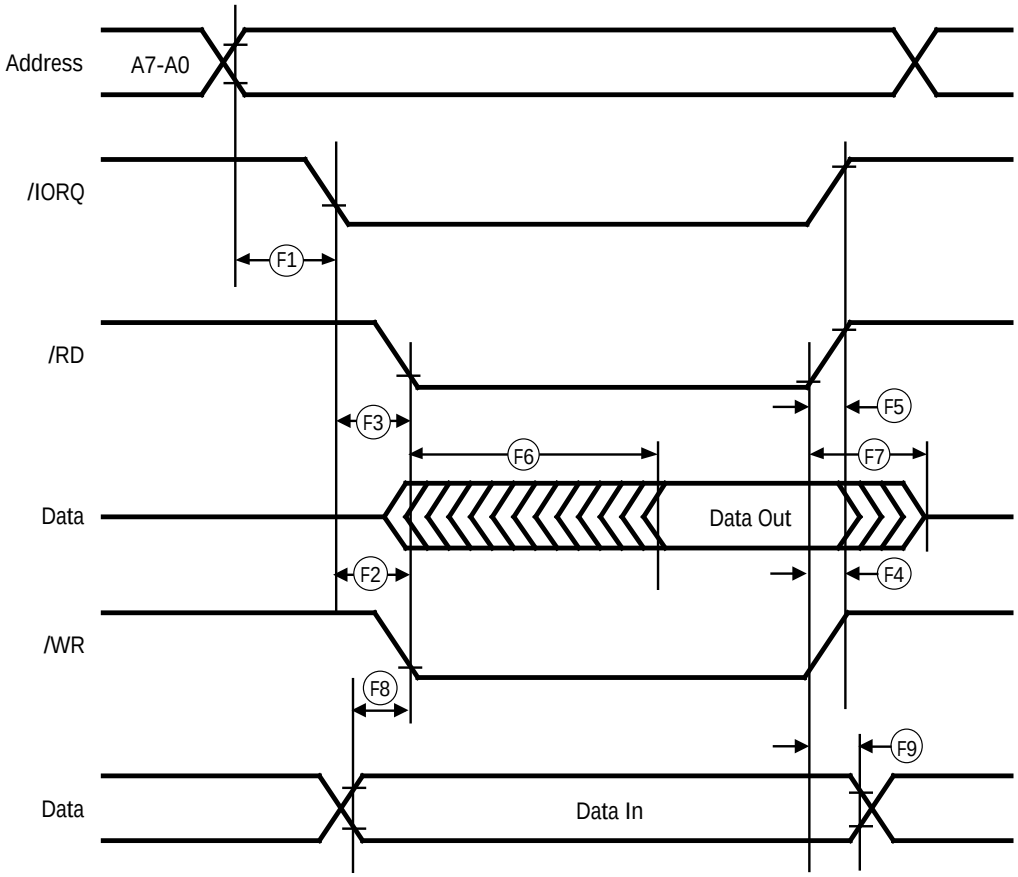


Figure 108. Read/Write External Bus Master Timing

16550 MIMIC TIMING (Continued)

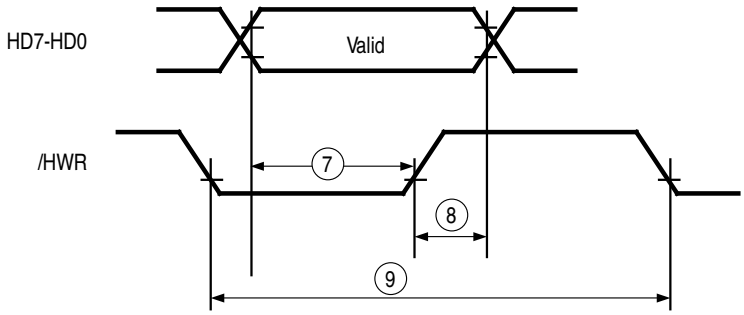


Figure 111. Data Setup and Hold, Output Delay, Write Cycle

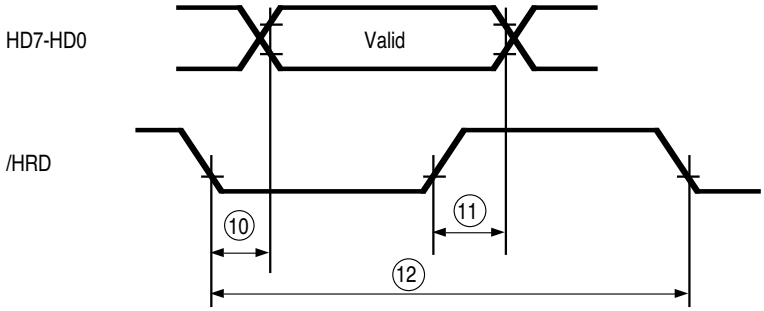


Figure 112. Data Setup and Hold, Output Delay, Read Cycle

Table I. Data Setup and Hold, Output Delay, Read Cycle

			Z8L182 20 MHz		Z80182 33 MHz		
No.	**Sym**	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
7	tDs	Data Setup Time	30		30		ns
8	tDh	Data Hold Time	30		30		ns
9	tWc	Write Cycle Delay	2.5 MPU Clock Cycles		2.5 MPU Clock Cycles		ns
10	tRvD	Delay from /HRD to Data		125		125	ns
11	tHz	/HRD to Floating Delay		100		100	ns
12	tRc	Read Cycle Delay	125		125		ns

Note:
These AC parameter values are preliminary and are subject to change without notice.