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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 64 |
| Number of Logic Elements/Cells | 256 |
| Total RAM Bits | - |
| Number of I/O | 65 |
| Number of Gates | 3000 |
| Voltage - Supply | 4.75V ~ 5.25V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 84-LCC (J-Lead) |
| Supplier Device Package | 84-PLCC (29.31x29.31) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc5202-6pc84c |

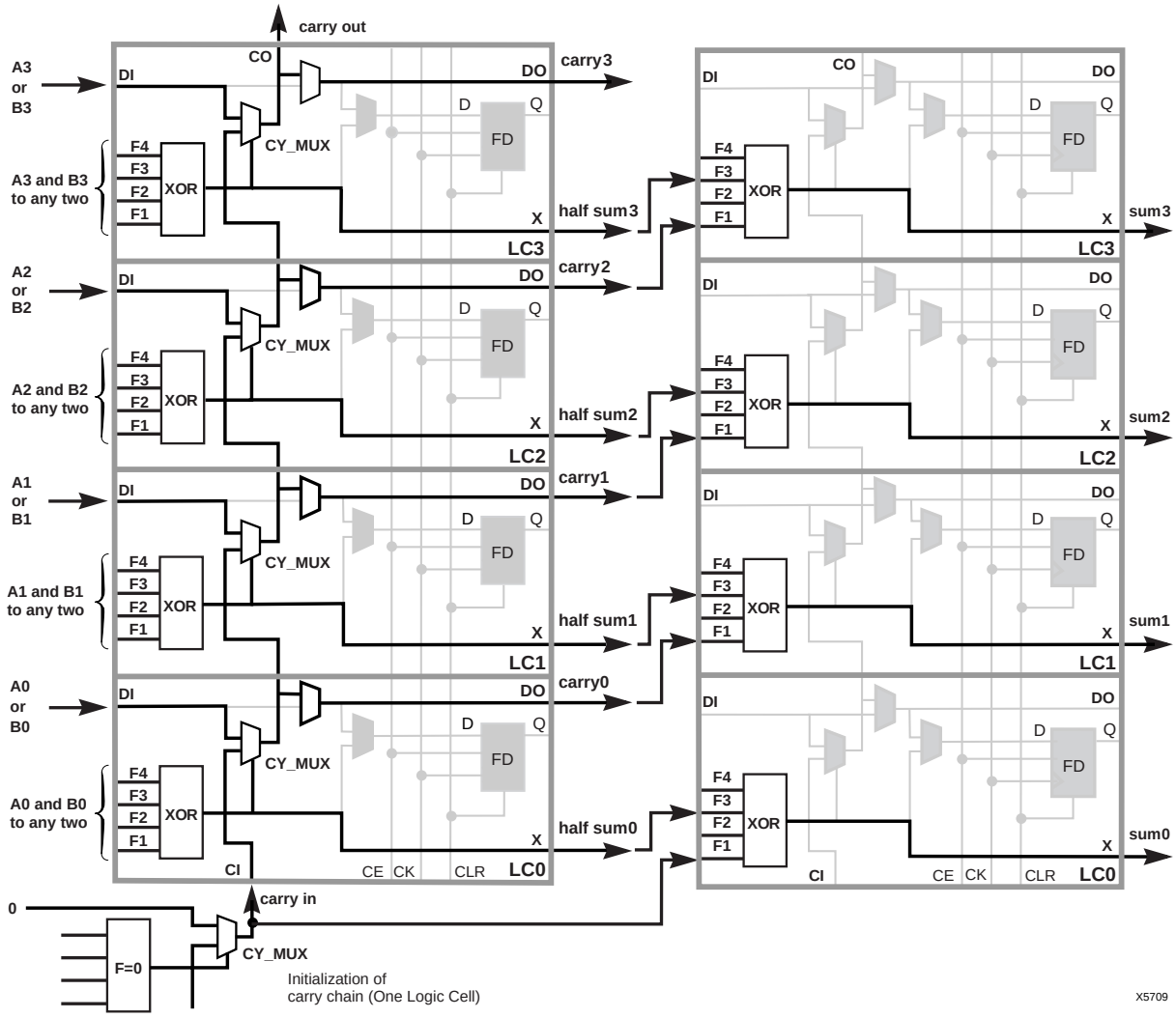



**Figure 6: XC5200 CY_MUX Used for Adder Carry Propagate**

## Carry Function

The XC5200 family supports a carry-logic feature that enhances the performance of arithmetic functions such as counters, adders, etc. A carry multiplexer (CY_MUX) symbol is used to indicate the XC5200 carry logic. This symbol represents the dedicated 2:1 multiplexer in each LC that performs the one-bit high-speed carry propagate per logic cell (four bits per CLB).

While the carry propagate is performed inside the LC, an adjacent LC must be used to complete the arithmetic function. Figure 6 represents an example of an adder function. The carry propagate is performed on the CLB shown, which also generates the half-sum for the four-bit adder. An adjacent CLB is responsible for XORing the half-sum with the corresponding carry-out. Thus an adder or counter requires two LCs per bit. Notice that the carry chain requires an initialization stage, which the XC5200 family accomplishes using the carry initialize (CY_INIT) macro and one additional LC. The carry chain can propagate vertically up a column of CLBs.

The XC5200 library contains a set of Relationally-Placed Macros (RPMs) and arithmetic functions designed to take advantage of the dedicated carry logic. Using and modifying these macros makes it much easier to implement cus-

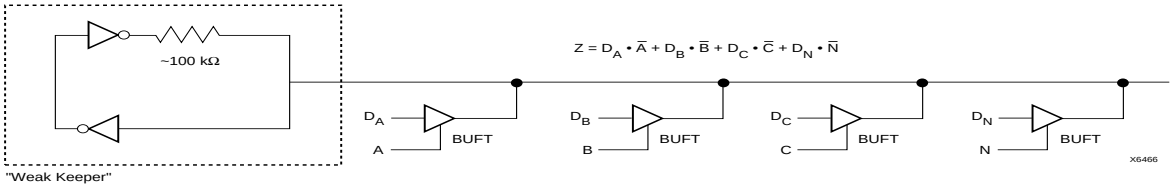



**Figure 10: 3-State Buffers Implement a Multiplexer**

## Input/Output Blocks

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

The I/O block, shown in Figure 11, consists of an input buffer and an output buffer. The output driver is an 8-mA full-rail CMOS buffer with 3-state control. Two slew-rate control modes are supported to minimize bus transients. Both the output buffer and the 3-state control are invertible. The input buffer has globally selected CMOS or TTL input thresholds. The input buffer is invertible and also provides a programmable delay line to assure reliable chip-to-chip set-up and hold times. Minimum ESD protection is 3 KV using the Human Body Model.

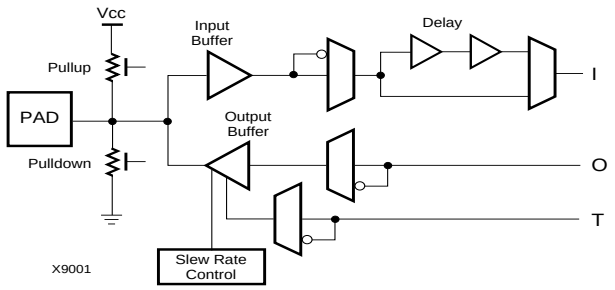



**Figure 11: XC5200 I/O Block**

### IOB Input Signals

The XC5200 inputs can be globally configured for either TTL (1.2V) or CMOS thresholds, using an option in the bitstream generation software. There is a slight hysteresis of about 300mV.

The inputs of XC5200-Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC5200-Series device inputs are shown in Table 5.

**Table 5: Supported Sources for XC5200-Series Device Inputs**

| Source | XC5200 Input Mode | |
|---|---|---|
| | 5 V, TTL | 5 V, CMOS |
| Any device, Vcc = 3.3 V, CMOS outputs | √ | **Unreliable Data** |
| Any device, Vcc = 5 V, TTL outputs | √ | |
| Any device, Vcc = 5 V, CMOS outputs | √ | √ |

### Optional Delay Guarantees Zero Hold Time

XC5200 devices do not have storage elements in the IOBs. However, XC5200 IOBs can be efficiently routed to CLB flip-flops or latches to store the I/O signals.

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the CLB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the CLB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the software default.

The XC5200 IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC5200 global clock buffers. (See "Global Lines" on page 96 for a description of the global clock buffers in the XC5200.) For a shorter input register setup time, with

senting the decoding of the corresponding state of the boundary-scan internal state machine.

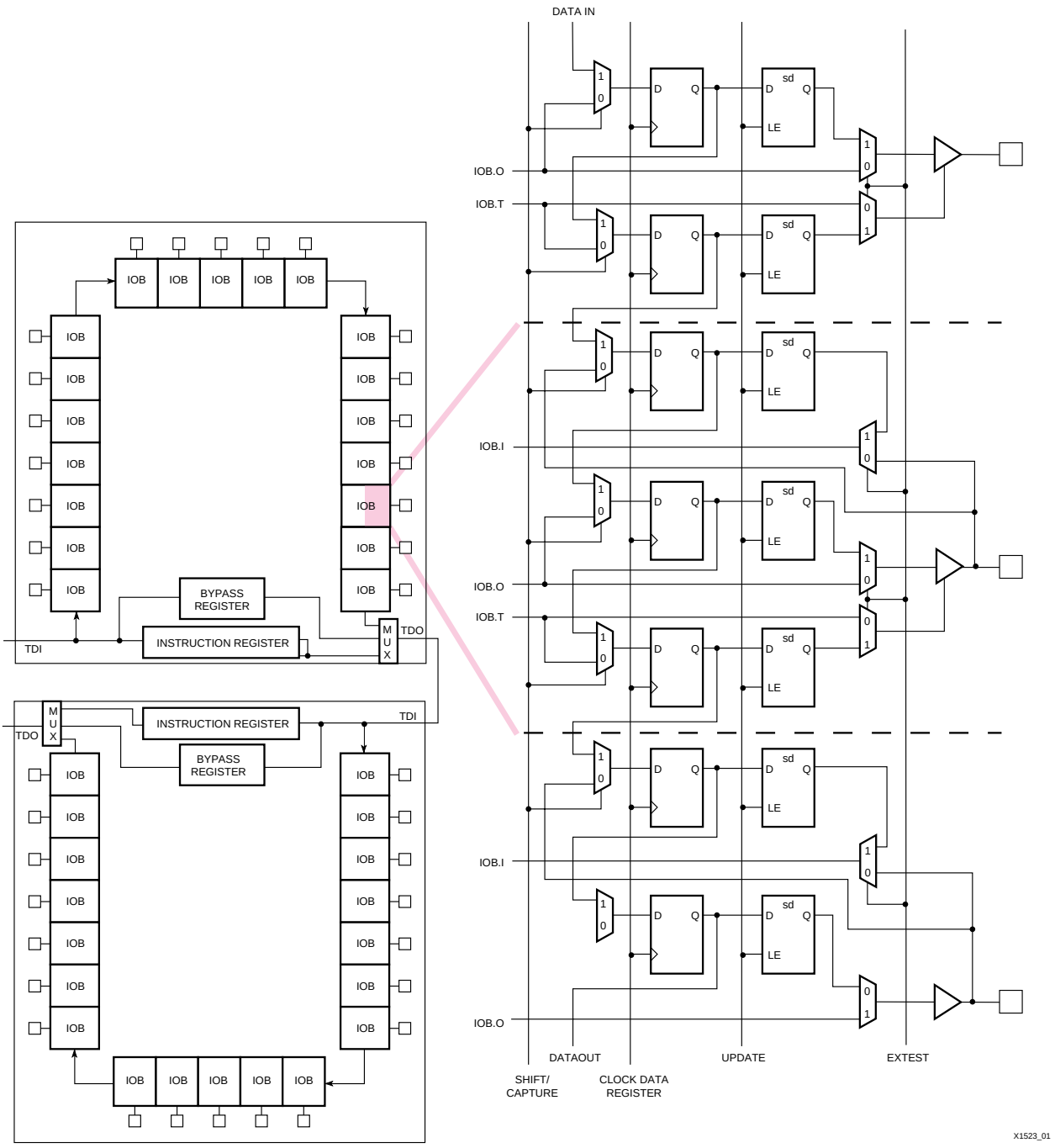



**Figure 19: XC5200-Series Boundary Scan Logic**

XC5200-Series devices can also be configured through the boundary scan logic. See XAPP 017 for more information.

## Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-State Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-State pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions, USER1 and USER2. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

## Instruction Set

The XC5200-Series boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 7.

**Table 7: Boundary Scan Instructions**

| Instruction I2 | I1 | I0 | Test Selected | TDO Source | I/O Data Source |
|---|---|---|---|---|---|
| 0 | 0 | 0 | EXTEST | DR | DR |
| 0 | 0 | 1 | SAMPLE/PRELOAD | DR | Pin/Logic |
| 0 | 1 | 0 | USER 1 | BSCAN.TDO1 | User Logic |
| 0 | 1 | 1 | USER 2 | BSCAN.TDO2 | User Logic |
| 1 | 0 | 0 | READBACK | Readback Data | Pin/Logic |
| 1 | 0 | 1 | CONFIGURE | DOUT | Disabled |
| 1 | 1 | 0 | Reserved | — | — |
| 1 | 1 | 1 | BYPASS | Bypass Register | — |

## Bit Sequence

The bit sequence within each IOB is: 3-State, Out, In. The data-register cells for the TAP pins TMS, TCK, and TDI have an OR-gate that permanently disables the output buffer if boundary-scan operation is selected. Consequently, it is impossible for the outputs in IOBs used by TAP inputs to conflict with TAP operation. TAP data is taken directly from the pin, and cannot be overwritten by injected boundary-scan data.

The primary global clock inputs (PGCK1-PGCK4) are taken directly from the pins, and cannot be overwritten with boundary-scan data. However, if necessary, it is possible to drive the clock input from boundary scan. The external clock source is 3-stated, and the clock net is driven with boundary scan data through the output driver in the clock-pad IOB. If the clock-pad IOBs are used for non-clock signals, the data may be overwritten normally.

Pull-up and pull-down resistors remain active during boundary scan. Before and during configuration, all pins are pulled up. After configuration, the choice of internal pull-up or pull-down resistor must be taken into account when designing test vectors to detect open-circuit PC traces.

From a cavity-up view of the chip (as shown in XDE or Epic), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Table 8. The device-specific pinout tables for the XC5200 Series include the boundary scan locations for each IOB pin.

**Table 8: Boundary Scan Bit Sequence**

| Bit Position | I/O Pad Location |
|---|---|
| Bit 0 (TDO) | Top-edge I/O pads (right to left) |
| Bit 1 | ... |
| ... | Left-edge I/O pads (top to bottom) |
| ... | Bottom-edge I/O pads (left to right) |
| ... | Right-edge I/O pads (bottom to top) |
| Bit N (TDI) | BSCANT.UPD |

BSDL (Boundary Scan Description Language) files for XC5200-Series devices are available on the Xilinx web site in the File Download area.

## Including Boundary Scan

If boundary scan is only to be used during configuration, no special elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, include the BSCAN library symbol and connect pad symbols to the TDI, TMS, TCK and TDO pins, as shown in Figure 20.

tions During Configuration" on page 124, in the "Configuration Timing" section.

**Table 9: Pin Descriptions**

| Pin Name | I/O During Config. | I/O After Config. | Pin Description |
|---|---|---|---|
| **Permanently Dedicated Pins** | | | |
| VCC | I | I | Five or more (depending on package) connections to the nominal +5 V supply voltage. All must be connected, and each must be decoupled with a 0.01 - 0.1 µF capacitor to Ground. |
| GND | I | I | Four or more (depending on package type) connections to Ground. All must be connected. |
| CCLK | I or O | I | During configuration, Configuration Clock (CCLK) is an output in Master modes or Asynchronous Peripheral mode, but is an input in Slave mode, Synchronous Peripheral mode, and Express mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High time restriction on XC5200-Series devices, except during Readback. See "Violating the Maximum High and Low Time Specification for the Readback Clock" on page 113 for an explanation of this exception. |
| DONE | I/O | O | DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs.<br>The exact timing, the clock source for the Low-to-High transition, and the optional pull-up resistor are selected as options in the program that creates the configuration bitstream. The resistor is included by default. |
| $\overline{\text{PROGRAM}}$ | I | I | $\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA executes a complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$.<br>The $\overline{\text{PROGRAM}}$ pin has an optional weak pull-up after configuration. |
| **User I/O Pins That Can Have Special Functions** | | | |
| RDY/$\overline{\text{BUSY}}$ | O | I/O | During Peripheral mode configuration, this pin indicates when it is appropriate to write another byte of data into the FPGA. The same status is also available on D7 in Asynchronous Peripheral mode, if a read operation is performed when the device is selected. After configuration, RDY/$\overline{\text{BUSY}}$ is a user-programmable I/O pin.<br>RDY/$\overline{\text{BUSY}}$ is pulled High with a high-impedance pull-up prior to $\overline{\text{INIT}}$ going High. |
| $\overline{\text{RCLK}}$ | O | I/O | During Master Parallel configuration, each change on the A0-A17 outputs is preceded by a rising edge on $\overline{\text{RCLK}}$, a redundant output signal. $\overline{\text{RCLK}}$ is useful for clocked PROMs. It is rarely used during configuration. After configuration, $\overline{\text{RCLK}}$ is a user-programmable I/O pin. |
| M0, M1, M2 | I | I/O | As Mode inputs, these pins are sampled before the start of configuration to determine the configuration mode to be used. After configuration, M0, M1, and M2 become user-programmable I/O.<br>During configuration, these pins have weak pull-up resistors. For the most popular configuration mode, Slave Serial, the mode pins can thus be left unconnected. A pull-down resistor value of 3.3 kΩ is recommended for other modes. |
| TDO | O | O | If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output, after configuration is completed.<br>This pin can be user output only when called out by special schematic definitions. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used. |

Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as 1 MHz (default), 6 MHz, or 12 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +50%.

### *Peripheral Modes*

The two Peripheral modes accept byte-wide data from a bus. A RDY/BUSY status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

### *Slave Serial Mode*

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

#### Serial Daisy Chain

Multiple devices with different configurations can be connected together in a “daisy chain,” and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 28 on page 114. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. Figure 25 on page 109 shows the start-up timing for an XC5200-Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

#### Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, XC4000, and XC5200 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. If the chain contains XC5200-Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in Figure 25 on page 109. Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of Figure 25. The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC5200-Series device, not reaching F means that readback cannot be initiated and most boundary scan instructions cannot be used.

The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using options in the bitstream generation software.

XC5200 devices always have the same number of CCLKs in the power up delay, independent of the configuration mode, unlike the XC3000/XC4000 Series devices. To guarantee all devices in a daisy chain have finished the power-up delay, tie the INIT pins together, as shown in Figure 27.

#### XC3000 Master with an XC5200-Series Slave

Some designers want to use an XC3000 lead device in peripheral mode and have the I/O pins of the XC5200-Series devices all available for user I/O. Figure 22 provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC5200-Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.

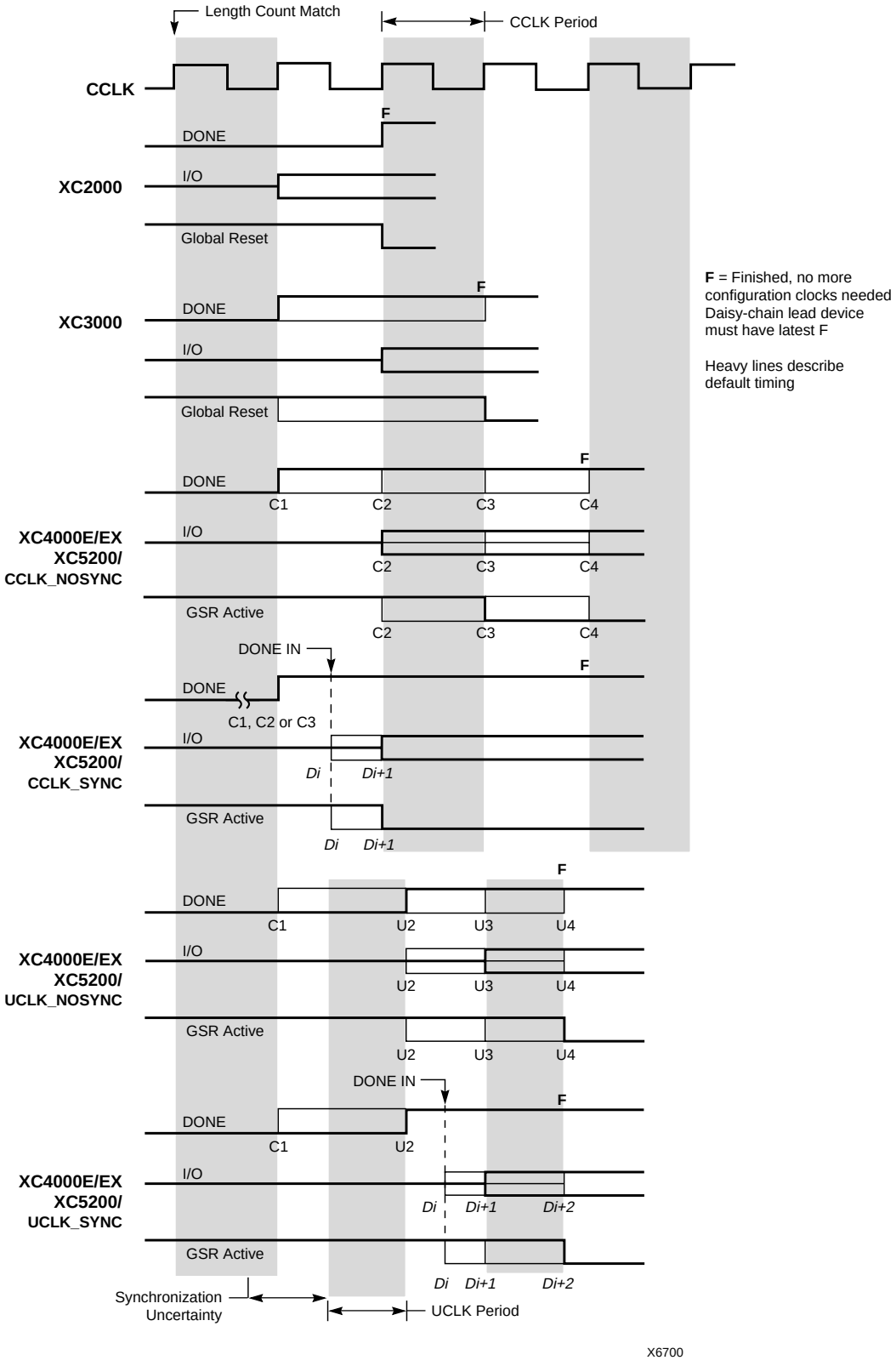



**Figure 25: Start-up Timing**

## Configuration

The length counter begins counting immediately upon entry into the configuration state. In slave-mode operation it is important to wait at least two cycles of the internal 1-MHz clock oscillator after $\overline{\text{INIT}}$ is recognized before toggling CCLK and feeding the serial bitstream. Configuration will not begin until the internal configuration logic reset is released, which happens two cycles after $\overline{\text{INIT}}$ goes High. A master device's configuration is delayed from 32 to 256 µs to ensure proper operation with any slave devices driven by the master device.

The 0010 preamble code, included for all modes except Express mode, indicates that the following 24 bits represent the length count. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to all devices in the daisy chain, DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain $\overline{\text{INIT}}$ pin Low. After all configuration frames have been loaded into an FPGA, DOUT again follows the input data so that the remaining data is passed on to the next device. In Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

### *Delaying Configuration After Power-Up*

To delay master mode configuration after power-up, pull the bidirectional $\overline{\text{INIT}}$ pin Low, using an open-collector (open-drain) driver. (See Figure 12.)

Using an open-collector or open-drain driver to hold $\overline{\text{INIT}}$ Low before the beginning of master mode configuration causes the FPGA to wait after completing the configuration memory clear operation. When $\overline{\text{INIT}}$ is no longer held Low externally, the device determines its configuration mode by capturing its mode pins, and is ready to start the configuration process. A master device waits up to an additional 250 µs to make sure that any slaves in the optional daisy chain have seen that $\overline{\text{INIT}}$ is High.

### *Start-Up*

Start-up is the transition from the configuration process to the intended user operation. This transition involves a change from one clock source to another, and a change from interfacing parallel or serial configuration data where most outputs are 3-stated, to normal operation with I/O pins active in the user-system. Start-up must make sure that the user-logic 'wakes up' gracefully, that the outputs become active without causing contention with the configuration signals, and that the internal flip-flops are released from the global Reset at the right time.

Figure 25 describes start-up timing for the three Xilinx families in detail. Express mode configuration always uses either CCLK_SYNC or UCLK_SYNC timing, the other configuration modes can use any of the four timing sequences.

To access the internal start-up signals, place the STARTUP library symbol.

#### Start-up Timing

Different FPGA families have different start-up sequences.

The XC2000 family goes through a fixed sequence. DONE goes High and the internal global Reset is de-activated one CCLK period after the I/O become active.

The XC3000A family offers some flexibility. DONE can be programmed to go High one CCLK period before or after the I/O become active. Independent of DONE, the internal global Reset is de-activated one CCLK period before or after the I/O become active.

The XC4000/XC5200 Series offers additional flexibility. The three events — DONE going High, the internal Reset being de-activated, and the user I/O going active — can all occur in any arbitrary sequence. Each of them can occur one CCLK period before or after, or simultaneous with, any of the others. This relative timing is selected by means of software options in the bitstream generation software.

The default option, and the most practical one, is for DONE to go High first, disconnecting the configuration data source and avoiding any contention when the I/Os become active one clock later. Reset is then released another clock period later to make sure that user-operation starts from stable internal conditions. This is the most common sequence, shown with heavy lines in Figure 25, but the designer can modify it to meet particular requirements.

Normally, the start-up sequence is controlled by the internal device oscillator output (CCLK), which is asynchronous to the system clock.

XC4000/XC5200 Series offers another start-up clocking option, UCLK_NOSYNC. The three events described above need not be triggered by CCLK. They can, as a configuration option, be triggered by a user clock. This means that the device can wake up in synchronism with the user system.

When the UCLK_SYNC option is enabled, the user can externally hold the open-drain DONE output Low, and thus stall all further progress in the start-up sequence until DONE is released and has gone High. This option can be used to force synchronization of several FPGAs to a common user clock, or to guarantee that all devices are successfully configured before any I/Os go active.

If either of these two options is selected, and no user clock is specified in the design or attached to the device, the chip could reach a point where the configuration of the device is complete and the Done pin is asserted, but the outputs do not become active. The solution is either to recreate the bitstream specifying the start-up clock as CCLK, or to supply the appropriate user clock.

### Start-up Sequence

The Start-up sequence begins when the configuration memory is full, and the total number of configuration clocks received since $\overline{\text{INIT}}$ went High equals the loaded value of the length count.

The next rising clock edge sets a flip-flop Q0, shown in Figure 26. Q0 is the leading bit of a 5-bit shift register. The outputs of this register can be programmed to control three events.

- The release of the open-drain DONE output
- The change of configuration-related pins to the user function, activating all IOBs.
- The termination of the global Set/Reset initialization of all CLB and IOB storage elements.

The DONE pin can also be wire-ANDed with DONE pins of other FPGAs or with other external signals, and can then be used as input to bit Q3 of the start-up register. This is called “Start-up Timing Synchronous to Done In” and is selected by either CCLK_SYNC or UCLK_SYNC.

When DONE is not used as an input, the operation is called “Start-up Timing Not Synchronous to DONE In,” and is selected by either CCLK_NOSYNC or UCLK_NOSYNC.

As a configuration option, the start-up control register beyond Q0 can be clocked either by subsequent CCLK pulses or from an on-chip user net called STARTUP.CLK. These signals can be accessed by placing the STARTUP library symbol.

### Start-up from CCLK

If CCLK is used to drive the start-up, Q0 through Q3 provide the timing. Heavy lines in Figure 25 show the default timing, which is compatible with XC2000 and XC3000 devices using early DONE and late Reset. The thin lines indicate all other possible timing options.

### Start-up from a User Clock (STARTUP.CLK)

When, instead of CCLK, a user-supplied start-up clock is selected, Q1 is used to bridge the unknown phase relationship between CCLK and the user clock. This arbitration causes an unavoidable one-cycle uncertainty in the timing of the rest of the start-up sequence.

## *DONE Goes High to Signal End of Configuration*

In all configuration modes except Express mode, XC5200-Series devices read the expected length count from the bitstream and store it in an internal register. The length count varies according to the number of devices and the composition of the daisy chain. Each device also counts the number of CCLKs during configuration.

Two conditions have to be met in order for the DONE pin to go high:

- the chip's internal memory must be full, and
- the configuration length count must be met, *exactly*.

This is important because the counter that determines when the length count is met begins with the very first CCLK, not the first one after the preamble.

Therefore, if a stray bit is inserted before the preamble, or the data source is not ready at the time of the first CCLK, the internal counter that holds the number of CCLKs will be one ahead of the actual number of data bits read. At the end of configuration, the configuration memory will be full, but the number of bits in the internal counter will not match the expected length count.

As a consequence, a Master mode device will continue to send out CCLKs until the internal counter turns over to zero, and then reaches the correct length count a second time. This will take several seconds [$2^{24} * $ CCLK period] — which is sometimes interpreted as the device not configuring at all.

If it is not possible to have the data ready at the time of the first CCLK, the problem can be avoided by increasing the number in the length count by the appropriate value.

In Express mode, there is no length count. The DONE pin for each device goes High when the device has received its quota of configuration data. Wiring the DONE pins of several devices together delays start-up of all devices until all are fully configured.

Note that DONE is an open-drain output and does not go High unless an internal pull-up is activated or an external pull-up is attached. The internal pull-up is activated as the default by the bitstream generation software.

## *Release of User I/O After DONE Goes High*

By default, the user I/O are released one CCLK cycle after the DONE pin goes High. If CCLK is not clocked after DONE goes High, the outputs remain in their initial state — 3-stated, with a 20 kΩ - 100 kΩ pull-up. The delay from

DONE High to active user I/O is controlled by an option to the bitstream generation software.

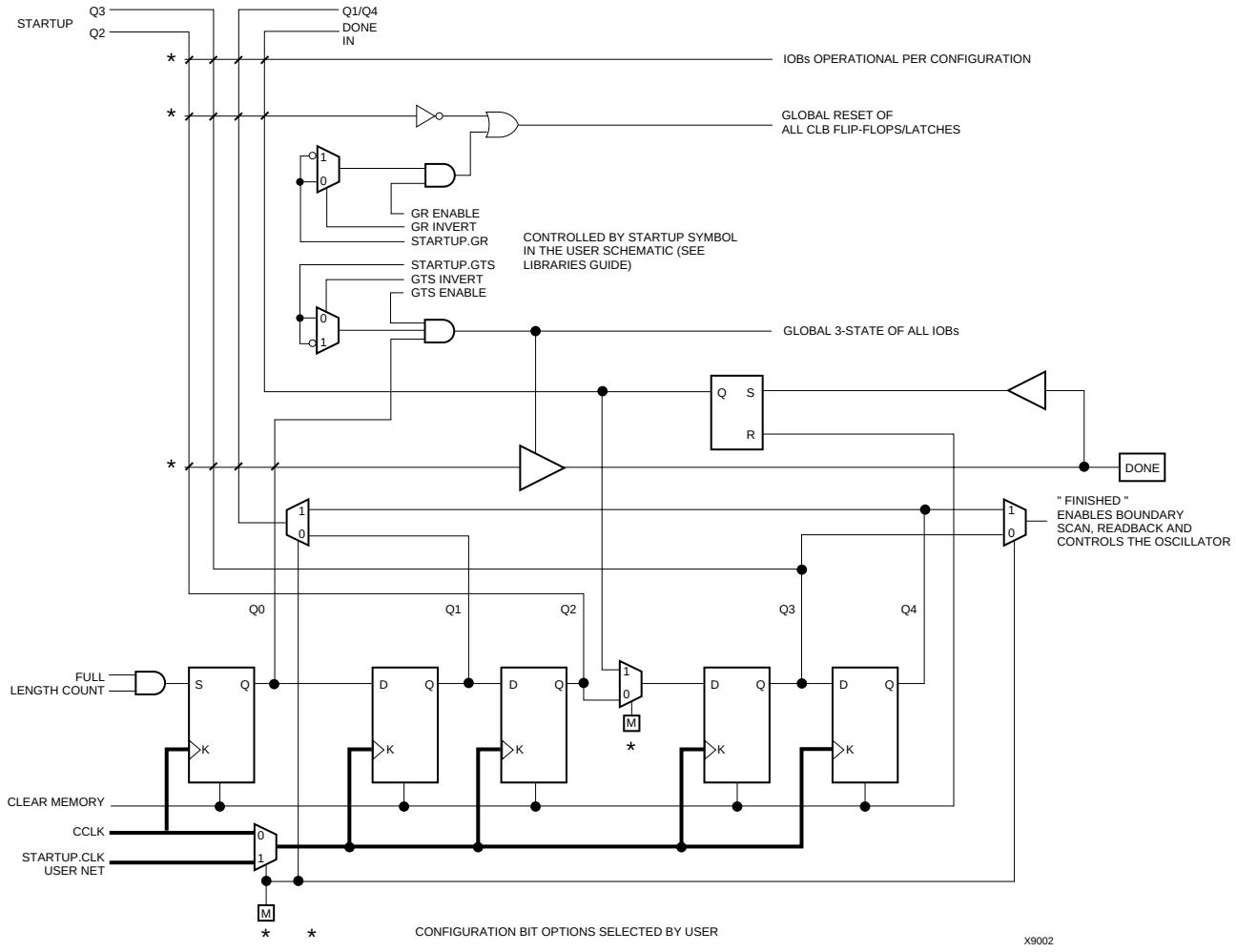



**Figure 26: Start-up Logic**

### *Release of Global Reset After DONE Goes High*

By default, Global Reset (GR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial reset state. The delay from DONE High to GR inactive is controlled by an option to the bitstream generation software.

### *Configuration Complete After DONE Goes High*

Three full CCLK cycles are required after the DONE pin goes High, as shown in Figure 25 on page 109. If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

## Configuration Through the Boundary Scan Pins

XC5200-Series devices can be configured through the boundary scan pins.

For detailed information, refer to the Xilinx application note XAPP017, "*Boundary Scan in XC4000 and XC5200 Devices*."

## Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs.

## Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

### Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin.

There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 28 shows a full master/slave system. An XC5200-Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

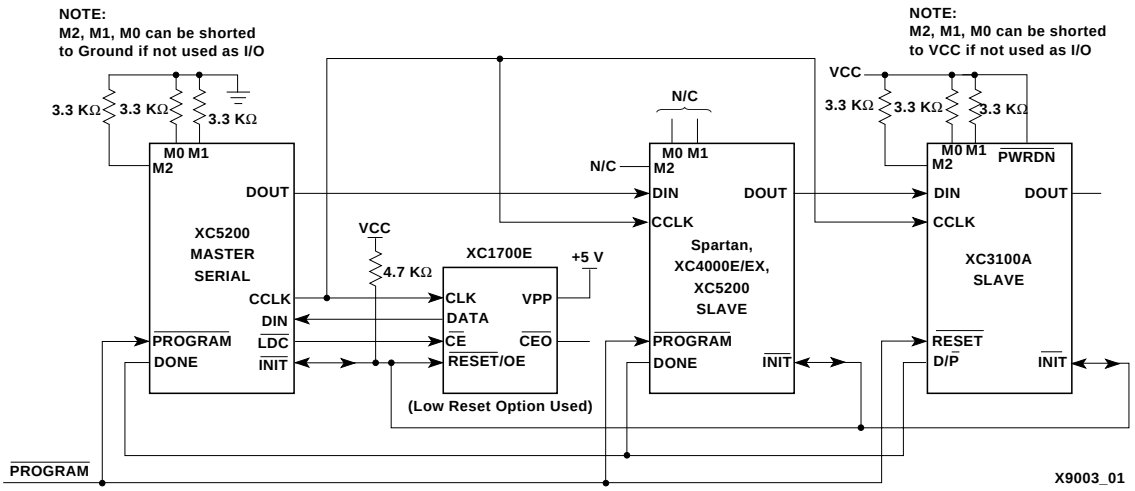
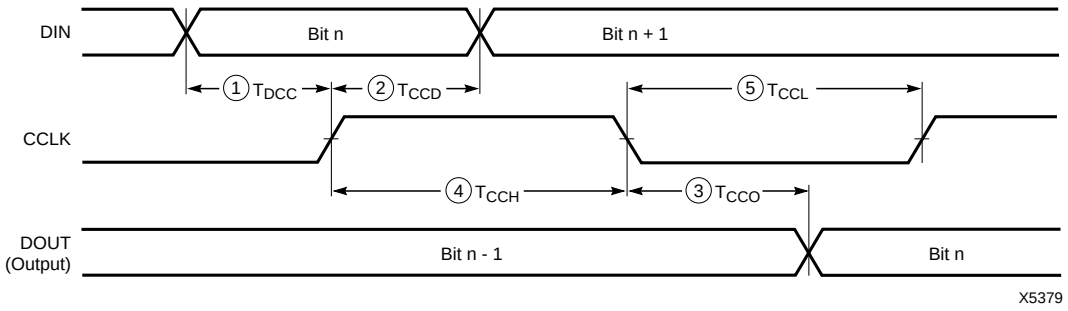



**Figure 28: Master/Slave Serial Mode Circuit Diagram**




| | Description | Symbol | | Min | Max | Units |
|---|---|---|---|---|---|---|
| CCLK | DIN setup | 1 | $T_{DCC}$ | 20 | | ns |
| | DIN hold | 2 | $T_{CCD}$ | 0 | | ns |
| | DIN to DOUT | 3 | $T_{CCO}$ | | 30 | ns |
| | High time | 4 | $T_{CCH}$ | 45 | | ns |
| | Low time | 5 | $T_{CCL}$ | 45 | | ns |
| | Frequency | | $F_{CC}$ | | 10 | MHz |

**Note:** Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

**Figure 29: Slave Serial Mode Programming Switching Characteristics**

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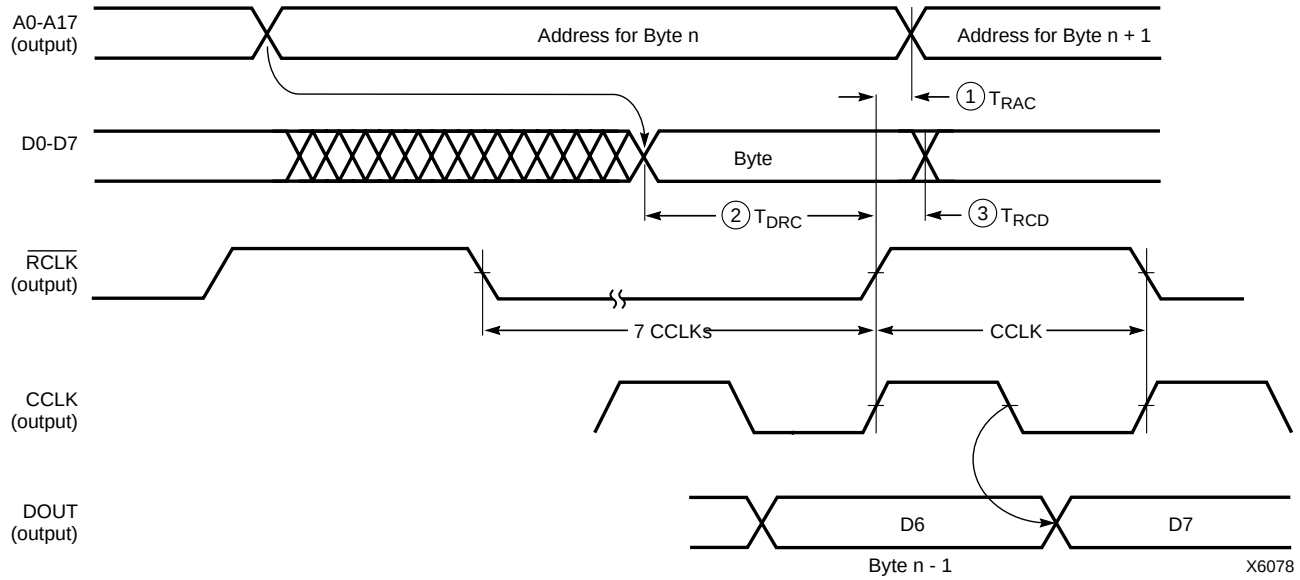



| | Description | Symbol | | Min | Max | Units |
|---|---|---|---|---|---|---|
| CCLK | Delay to Address valid | 1 | $T_{RAC}$ | 0 | 200 | ns |
| | Data setup time | 2 | $T_{DRC}$ | 60 | | ns |
| | Data hold time | 3 | $T_{RCD}$ | 0 | | ns |

Note: 1. At power-up, $V_{CC}$ must rise from 2.0 V to $V_{CC}$ min in less then 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until $V_{CC}$ is Valid.
2. The first Data byte is loaded and CCLK starts at the end of the first $\overline{\text{RCLK}}$ active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

**Figure 32: Master Parallel Mode Programming Switching Characteristics**

## Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/BUSY output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/BUSY is pulled High with a high-impedance pullup prior to INIT going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

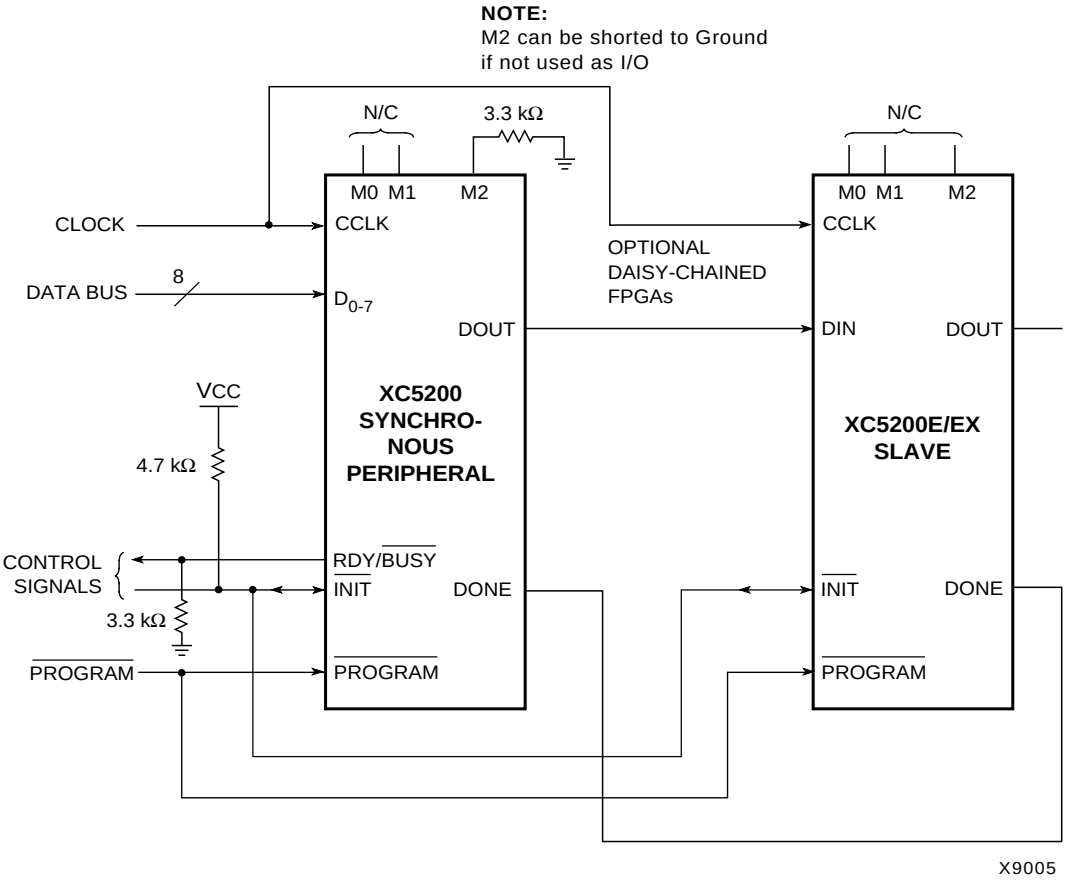
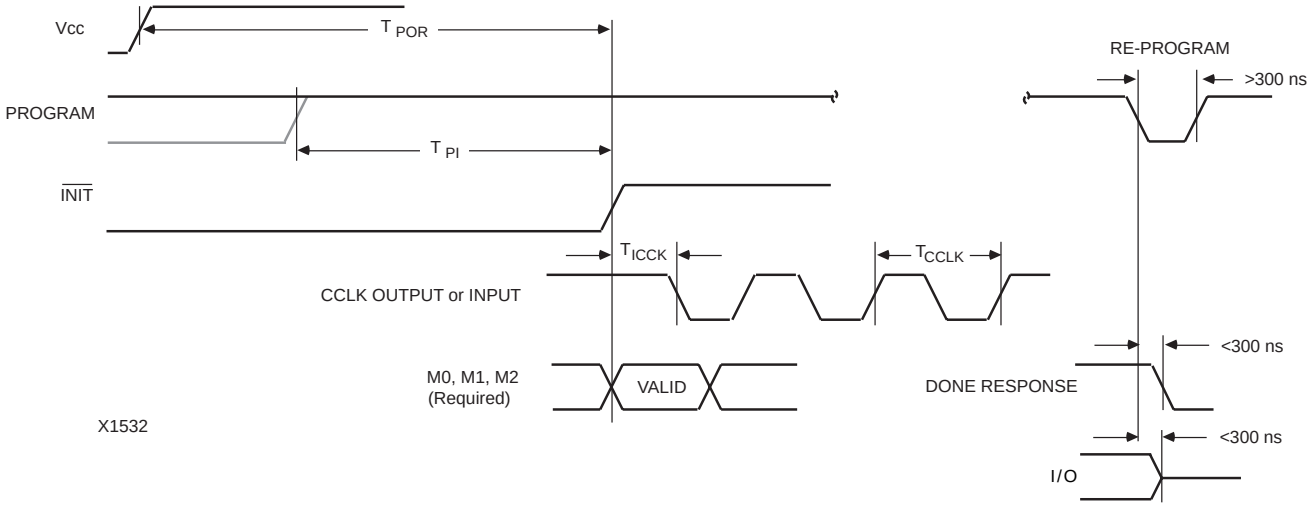



**Figure 33: Synchronous Peripheral Mode Circuit Diagram**

## Configuration Switching Characteristics




## Master Modes

| Description | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Power-On-Reset | $T_{POR}$ | 2 | 15 | ms |
| Program Latency | $T_{PI}$ | 6 | 70 | µs per CLB column |
| CCLK (output) Delay | $T_{ICCK}$ | 40 | 375 | µs |
| period (slow) | $T_{CCLK}$ | 640 | 3000 | ns |
| period (fast) | $T_{CCLK}$ | 100 | 375 | ns |

## Slave and Peripheral Modes

| Description | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Power-On-Reset | $T_{POR}$ | 2 | 15 | ms |
| Program Latency | $T_{PI}$ | 6 | 70 | µs per CLB column |
| CCLK (input) Delay (required) | $T_{ICCK}$ | 5 | | µs |
| period (required) | $T_{CCLK}$ | 100 | | ns |

**Note:** At power-up, $V_{CC}$ must rise from 2.0 to $V_{CC}$ min in less than 15 ms, otherwise delay configuration using $\overline{\text{PROGRAM}}$ until $V_{CC}$ is valid.

## XC5200 IOB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

| Speed Grade | | -6 | -5 | -4 | -3 |
|---|---|---|---|---|---|
| **Description** | **Symbol** | **Max (ns)** | **Max (ns)** | **Max (ns)** | **Max (ns)** |
| **Input** | | | | | |
| Propagation Delays from CMOS or TTL Levels | | | | | |
| Pad to I (no delay) | $T_{PI}$ | 5.7 | 5.0 | 4.8 | 3.3 |
| Pad to I (with delay) | $T_{PID}$ | 11.4 | 10.2 | 10.2 | 9.5 |
| **Output** | | | | | |
| Propagation Delays to CMOS or TTL Levels | | | | | |
| Output (O) to Pad (fast) | $T_{OPF}$ | 4.6 | 4.5 | 4.5 | 3.5 |
| Output (O) to Pad (slew-limited) | $T_{OPS}$ | 9.5 | 8.4 | 8.0 | 5.0 |
| From clock (CK) to output pad (fast), using direct connect between Q and output (O) | $T_{OKPOF}$ | 10.1 | 9.3 | 8.3 | 7.5 |
| From clock (CK) to output pad (slew-limited), using direct connect between Q and output (O) | $T_{OKPOS}$ | 14.9 | 13.1 | 11.8 | 10.0 |
| 3-state to Pad active (fast) | $T_{TSONF}$ | 5.6 | 5.2 | 4.9 | 4.6 |
| 3-state to Pad active (slew-limited) | $T_{TSONS}$ | 10.4 | 9.0 | 8.3 | 6.0 |
| Internal GTS to Pad active | $T_{GTS}$ | 17.7 | 15.9 | 14.7 | 13.5 |

**Note:**
1. Timing is measured at pin threshold, with 50-pF external capacitance loads. **Slew-limited** output rise/fall times are approximately two times longer than **fast** output rise/fall times.
2. Unused and unbonded IOBs are configured by default as inputs with internal pull-up resistors.
3. Timing is based upon the XC5215 device. For other devices, see Timing Calculator.

| Pin | Description | VQ64* | PC84 | PQ100 | VQ100 | TQ144 | PG156 | Boundary Scan Order |
|---|---|---|---|---|---|---|---|---|
| 35. | I/O (HDC) | 19 | 36 | 31 | 28 | 40 | D14 | 204 |
| 36. | I/O | - | - | 32 | 29 | 43 | E14 | 207 |
| 37. | I/O (LDC) | 20 | 37 | 33 | 30 | 44 | C16 | 210 |
| | GND | - | - | - | - | 45 | F14 | - |
| 38. | I/O | - | 38 | 34 | 31 | 48 | F16 | 216 |
| 39. | I/O | 21 | 39 | 35 | 32 | 49 | G14 | 219 |
| 40. | I/O | - | - | 36 | 33 | 50 | G15 | 222 |
| 41. | I/O | - | - | 37 | 34 | 51 | G16 | 228 |
| 42. | I/O | 22 | 40 | 38 | 35 | 52 | H16 | 231 |
| 43. | I/O ($\overline{ERR}$, $\overline{INIT}$) | 23 | 41 | 39 | 36 | 53 | H15 | 234 |
| | VCC | 24 | 42 | 40 | 37 | 54 | H14 | - |
| | GND | 25 | 43 | 41 | 38 | 55 | J14 | - |
| 44. | I/O | 26 | 44 | 42 | 39 | 56 | J15 | 240 |
| 45. | I/O | 27 | 45 | 43 | 40 | 57 | J16 | 243 |
| 46. | I/O | - | - | 44 | 41 | 58 | K16 | 246 |
| 47. | I/O | - | - | 45 | 42 | 59 | K15 | 252 |
| 48. | I/O | 28 | 46 | 46 | 43 | 60 | K14 | 255 |
| 49. | I/O | 29 | 47 | 47 | 44 | 61 | L16 | 258 |
| | GND | - | - | - | - | 64 | L14 | - |
| 50. | I/O | - | 48 | 48 | 45 | 65 | P16 | 264 |
| 51. | I/O | 30 | 49 | 49 | 46 | 66 | M14 | 267 |
| 52. | I/O | - | 50 | 50 | 47 | 69 | N14 | 276 |
| 53. | I/O | 31 | 51 | 51 | 48 | 70 | R16 | 279 |
| | GND | - | 52 | 52 | 49 | 71 | P14 | - |
| | DONE | 32 | 53 | 53 | 50 | 72 | R15 | - |
| | VCC | 33 | 54 | 54 | 51 | 73 | P13 | - |
| | PROG | 34 | 55 | 55 | 52 | 74 | R14 | - |
| 54. | I/O (D7) | 35 | 56 | 56 | 53 | 75 | T16 | 288 |
| 55. | GCK3 (I/O) | 36 | 57 | 57 | 54 | 76 | T15 | 291 |
| 56. | I/O (D6) | 37 | 58 | 58 | 55 | 79 | T14 | 300 |
| 57. | I/O | - | - | 59 | 56 | 80 | T13 | 303 |
| | GND | - | - | - | - | 81 | P11 | - |
| 58. | I/O (D5) | 38 | 59 | 60 | 57 | 84 | T10 | 306 |
| 59. | I/O ($\overline{CS0}$) | - | 60 | 61 | 58 | 85 | P10 | 312 |
| 60. | I/O | - | - | 62 | 59 | 86 | R10 | 315 |
| 61. | I/O | - | - | 63 | 60 | 87 | T9 | 318 |
| 62. | I/O (D4) | 39 | 61 | 64 | 61 | 88 | R9 | 324 |
| 63. | I/O | - | 62 | 65 | 62 | 89 | P9 | 327 |
| | VCC | 40 | 63 | 66 | 63 | 90 | R8 | - |
| | GND | 41 | 64 | 67 | 64 | 91 | P8 | - |
| 64. | I/O (D3) | 42 | 65 | 68 | 65 | 92 | T8 | 336 |
| 65. | I/O ($\overline{RS}$) | 43 | 66 | 69 | 66 | 93 | T7 | 339 |
| 66. | I/O | - | - | 70 | 67 | 94 | T6 | 342 |
| 67. | I/O | - | - | - | - | 95 | R7 | 348 |
| 68. | I/O (D2) | 44 | 67 | 71 | 68 | 96 | P7 | 351 |
| 69. | I/O | - | 68 | 72 | 69 | 97 | T5 | 360 |
| | GND | - | - | - | - | 100 | P6 | - |
| 70. | I/O (D1) | 45 | 69 | 73 | 70 | 101 | T3 | 363 |
| 71. | I/O ($\overline{RCLK\text{-}BUSY}$/RDY) | - | 70 | 74 | 71 | 102 | P5 | 366 |
| 72. | I/O (D0, DIN) | 46 | 71 | 75 | 72 | 105 | P4 | 372 |
| 73. | I/O (DOUT) | 47 | 72 | 76 | 73 | 106 | T2 | 375 |

## Pin Locations for XC5206 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

| Pin | Description | PC84 | PQ100 | VQ100 | TQ144 | PQ160 | TQ176 | PG191 | PQ208 | Boundary Scan Order |
|---|---|---|---|---|---|---|---|---|---|---|
| | VCC | 2 | 92 | 89 | 128 | 142 | 155 | J4 | 183 | - |
| 1. | I/O (A8) | 3 | 93 | 90 | 129 | 143 | 156 | J3 | 184 | 87 |
| 2. | I/O (A9) | 4 | 94 | 91 | 130 | 144 | 157 | J2 | 185 | 90 |
| 3. | I/O | - | 95 | 92 | 131 | 145 | 158 | J1 | 186 | 93 |
| 4. | I/O | - | 96 | 93 | 132 | 146 | 159 | H1 | 187 | 99 |
| 5. | I/O | - | - | - | - | - | 160 | H2 | 188 | 102 |
| 6. | I/O | - | - | - | - | - | 161 | H3 | 189 | 105 |
| 7. | I/O (A10) | 5 | 97 | 94 | 133 | 147 | 162 | G1 | 190 | 111 |
| 8. | I/O (A11) | 6 | 98 | 95 | 134 | 148 | 163 | G2 | 191 | 114 |
| 9. | I/O | - | - | - | 135 | 149 | 164 | F1 | 192 | 117 |
| 10. | I/O | - | - | - | 136 | 150 | 165 | E1 | 193 | 123 |
| | GND | - | - | - | 137 | 151 | 166 | G3 | 194 | - |
| 11. | I/O | - | - | - | - | 152 | 168 | C1 | 197 | 126 |
| 12. | I/O | - | - | - | - | 153 | 169 | E2 | 198 | 129 |
| 13. | I/O (A12) | 7 | 99 | 96 | 138 | 154 | 170 | F3 | 199 | 138 |
| 14. | I/O (A13) | 8 | 100 | 97 | 139 | 155 | 171 | D2 | 200 | 141 |
| 15. | I/O | - | - | - | 140 | 156 | 172 | B1 | 201 | 150 |
| 16. | I/O | - | - | - | 141 | 157 | 173 | E3 | 202 | 153 |
| 17. | I/O (A14) | 9 | 1 | 98 | 142 | 158 | 174 | C2 | 203 | 162 |
| 18. | I/O (A15) | 10 | 2 | 99 | 143 | 159 | 175 | B2 | 204 | 165 |
| | VCC | 11 | 3 | 100 | 144 | 160 | 176 | D3 | 205 | - |
| | GND | 12 | 4 | 1 | 1 | 1 | 1 | D4 | 2 | - |
| 19. | GCK1 (A16, I/O) | 13 | 5 | 2 | 2 | 2 | 2 | C3 | 4 | 174 |
| 20. | I/O (A17) | 14 | 6 | 3 | 3 | 3 | 3 | C4 | 5 | 177 |
| 21. | I/O | - | - | - | 4 | 4 | 4 | B3 | 6 | 183 |
| 22. | I/O | - | - | - | 5 | 5 | 5 | C5 | 7 | 186 |
| 23. | I/O (TDI) | 15 | 7 | 4 | 6 | 6 | 6 | A2 | 8 | 189 |
| 24. | I/O (TCK) | 16 | 8 | 5 | 7 | 7 | 7 | B4 | 9 | 195 |
| 25. | I/O | - | - | - | - | 8 | 8 | C6 | 10 | 198 |
| 26. | I/O | - | - | - | - | 9 | 9 | A3 | 11 | 201 |
| | GND | - | - | - | 8 | 10 | 10 | C7 | 14 | - |
| 27. | I/O | - | - | - | 9 | 11 | 11 | A4 | 15 | 207 |
| 28. | I/O | - | - | - | 10 | 12 | 12 | A5 | 16 | 210 |
| 29. | I/O (TMS) | 17 | 9 | 6 | 11 | 13 | 13 | B7 | 17 | 213 |
| 30. | I/O | 18 | 10 | 7 | 12 | 14 | 14 | A6 | 18 | 219 |
| 31. | I/O | - | - | - | - | - | 15 | C8 | 19 | 222 |
| 32. | I/O | - | - | - | - | - | 16 | A7 | 20 | 225 |
| 33. | I/O | - | - | - | 13 | 15 | 17 | B8 | 21 | 234 |
| 34. | I/O | - | 11 | 8 | 14 | 16 | 18 | A8 | 22 | 237 |
| 35. | I/O | 19 | 12 | 9 | 15 | 17 | 19 | B9 | 23 | 246 |
| 36. | I/O | 20 | 13 | 10 | 16 | 18 | 20 | C9 | 24 | 249 |
| | GND | 21 | 14 | 11 | 17 | 19 | 21 | D9 | 25 | - |
| | VCC | 22 | 15 | 12 | 18 | 20 | 22 | D10 | 26 | - |
| 37. | I/O | 23 | 16 | 13 | 19 | 21 | 23 | C10 | 27 | 255 |
| 38. | I/O | 24 | 17 | 14 | 20 | 22 | 24 | B10 | 28 | 258 |
| 39. | I/O | - | 18 | 15 | 21 | 23 | 25 | A9 | 29 | 261 |
| 40. | I/O | - | - | - | 22 | 24 | 26 | A10 | 30 | 267 |
| 41. | I/O | - | - | - | - | - | 27 | A11 | 31 | 270 |

| Pin | Description | PQ160 | HQ208 | HQ240 | PG299 | BG225 | BG352 | Boundary Scan Order |
|---|---|---|---|---|---|---|---|---|
| 100. | I/O | - | - | - | F17 | - | AE22 | 558 |
| 101. | I/O | - | - | - | G16 | - | AF23 | 564 |
| 102. | I/O | 49 | 63 | 69 | D19 | K7 | AD20 | 567 |
| 103. | I/O | 50 | 64 | 70 | E18 | M5 | AE21 | 570 |
| 104. | I/O | - | 65 | 71 | D20 | R4 | AF21 | 576 |
| 105. | I/O | - | 66 | 72 | G17 | N5 | AC19 | 579 |
| 106. | I/O | - | - | 73 | F18 | P5 | AD19 | 582 |
| 107. | I/O | - | - | 74 | H16 | L6 | AE20 | 588 |
| 108. | I/O | - | - | - | E19 | - | AF20 | 591 |
| 109. | I/O | - | - | - | F19 | - | AC18 | 594 |
| | GND | 51 | 67 | 75 | E20 | GND* | GND* | - |
| 110. | I/O | 52 | 68 | 76 | H17 | R5 | AD18 | 600 |
| 111. | I/O | 53 | 69 | 77 | G18 | M6 | AE19 | 603 |
| 112. | I/O | 54 | 70 | 78 | G19 | N6 | AC17 | 606 |
| 113. | I/O | 55 | 71 | 79 | H18 | P6 | AD17 | 612 |
| | VCC | - | - | 80 | F20 | VCC* | VCC* | - |
| 114. | I/O | - | 72 | 81 | J16 | R6 | AE17 | 615 |
| 115. | I/O | - | 73 | 82 | G20 | M7 | AE16 | 618 |
| 116. | I/O | - | - | - | H20 | - | AF16 | 624 |
| 117. | I/O | - | - | - | J18 | - | AC15 | 627 |
| 118. | I/O | - | - | 84 | J19 | N7 | AD15 | 630 |
| 119. | I/O | - | - | 85 | K16 | P7 | AE15 | 636 |
| 120. | I/O | 56 | 74 | 86 | J20 | R7 | AF15 | 639 |
| 121. | I/O | 57 | 75 | 87 | K17 | L7 | AD14 | 642 |
| 122. | I/O | 58 | 76 | 88 | K18 | N8 | AE14 | 648 |
| 123. | I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$) | 59 | 77 | 89 | K19 | P8 | AF14 | 651 |
| | VCC | 60 | 78 | 90 | L20 | VCC* | VCC* | - |
| | GND | 61 | 79 | 91 | K20 | GND* | GND* | - |
| 124. | I/O | 62 | 80 | 92 | L19 | L8 | AE13 | 660 |
| 125. | I/O | 63 | 81 | 93 | L18 | P9 | AC13 | 663 |
| 126. | I/O | 64 | 82 | 94 | L16 | R9 | AD13 | 672 |
| 127. | I/O | 65 | 83 | 95 | L17 | N9 | AF12 | 675 |
| 128. | I/O | - | 84 | 96 | M20 | M9 | AE12 | 678 |
| 129. | I/O | - | 85 | 97 | M19 | L9 | AD12 | 684 |
| 130. | I/O | - | - | - | N20 | - | AC12 | 687 |
| 131. | I/O | - | - | - | M18 | - | AF11 | 690 |
| 132. | I/O | - | - | 99 | N19 | R10 | AE11 | 696 |
| 133. | I/O | - | - | 100 | P20 | P10 | AD11 | 699 |
| | VCC | - | - | 101 | T20 | VCC* | VCC* | - |
| 134. | I/O | 66 | 86 | 102 | N18 | N10 | AE9 | 702 |
| 135. | I/O | 67 | 87 | 103 | P19 | K9 | AD9 | 708 |
| 136. | I/O | 68 | 88 | 104 | N17 | R11 | AC10 | 711 |
| 137. | I/O | 69 | 89 | 105 | R19 | P11 | AF7 | 714 |
| | GND | 70 | 90 | 106 | R20 | GND* | GND* | - |
| 138. | I/O | - | - | - | N16 | - | AE8 | 720 |
| 139. | I/O | - | - | - | P18 | - | AD8 | 723 |
| 140. | I/O | - | - | 107 | U20 | M10 | AC9 | 726 |
| 141. | I/O | - | - | 108 | P17 | N11 | AF6 | 732 |
| 142. | I/O | - | 91 | 109 | T19 | R12 | AE7 | 735 |
| 143. | I/O | - | 92 | 110 | R18 | L10 | AD7 | 738 |
| 144. | I/O | 71 | 93 | 111 | P16 | P12 | AE6 | 744 |
| 145. | I/O | 72 | 94 | 112 | V20 | M11 | AE5 | 747 |

## Product Availability

| | PINS | 64 | 84 | 100 | 100 | 144 | 156 | 160 | 176 | 191 | 208 | 208 | 223 | 225 | 240 | 240 | 299 | 352 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | TYPE | Plast. VQFP | Plast. PLCC | Plast. PQFP | Plast. VQFP | Plast. TQFP | Ceram. PGA | Plast. PQFP | Plast. TQFP | Ceram. PGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | Plast. BGA | High-Perf. QFP | Plast. PQFP | Ceram. PGA | Plast. BGA |
| | CODE | VQ64* | PC84 | PQ100 | VQ100 | TQ144 | PG156 | PQ160 | TQ176 | PG191 | HQ208 | PQ208 | PG223 | BG225 | HQ240 | PQ240 | PG299 | BG352 |
| XC5202 | -6 | CI | CI | CI | CI | CI | CI | | | | | | | | | | | |
| | -5 | CI | CI | CI | CI | CI | CI | | | | | | | | | | | |
| | -4 | C | C | C | C | C | C | | | | | | | | | | | |
| | -3 | C | C | C | C | C | C | | | | | | | | | | | |
| XC5204 | -6 | | CI | CI | CI | CI | CI | CI | | | | | | | | | | |
| | -5 | | CI | CI | CI | CI | CI | CI | | | | | | | | | | |
| | -4 | | C | C | C | C | C | C | | | | | | | | | | |
| | -3 | | C | C | C | C | C | C | | | | | | | | | | |
| XC5206 | -6 | | CI | CI | CI | CI | | CI | CI | CI | | CI | | | | | | |
| | -5 | | CI | CI | CI | CI | | CI | CI | CI | | CI | | | | | | |
| | -4 | | C | C | C | C | | C | C | C | | C | | | | | | |
| | -3 | | C | C | C | C | | C | C | C | | C | | | | | | |
| XC5210 | -6 | | CI | | | CI | | CI | CI | | | CI | CI | CI | | CI | | |
| | -5 | | CI | | | CI | | CI | CI | | | CI | CI | CI | | CI | | |
| | -4 | | C | | | C | | C | C | | | C | C | C | | C | | |
| | -3 | | C | | | C | | C | C | | | C | C | C | | C | | |
| XC5215 | -6 | | | | | | | CI | | | CI | | | CI | CI | | CI | CI |
| | -5 | | | | | | | C | | | C | | | C | C | | C | C |
| | -4 | | | | | | | C | | | C | | | C | C | | C | C |
| | -3 | | | | | | | C | | | C | | | C | C | | C | C |

7/8/98

C = Commercial $T_J$ = 0° to +85°C

I= Industrial $T_J$ = -40°C to +100°C

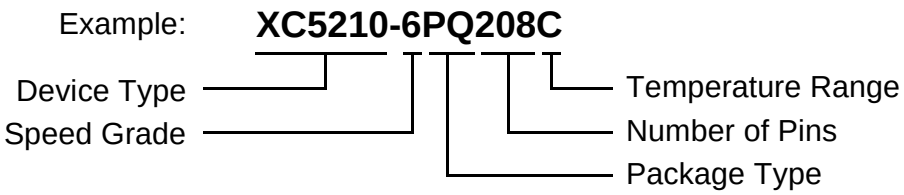
* VQ64 package supports Master Serial, Slave Serial, and Express configuration modes only.

## User I/O Per Package

| Device | Max I/O | Package Type | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VQ64 | PC84 | PQ100 | VQ100 | TQ144 | PG156 | PQ160 | TQ176 | PG191 | HQ208 | PQ208 | PG223 | BG225 | HQ240 | PQ240 | PG299 | BG352 |
| XC5202 | 84 | 52 | 65 | 81 | 81 | 84 | 84 | | | | | | | | | | | |
| XC5204 | 124 | | 65 | 81 | 81 | 117 | 124 | 124 | | | | | | | | | | |
| XC5206 | 148 | | 65 | 81 | 81 | 117 | | 133 | 148 | 148 | | 148 | | | | | | |
| XC5210 | 196 | | 65 | | | 117 | | 133 | 149 | | | 164 | 196 | 196 | | 196 | | |
| XC5215 | 244 | | | | | | | 133 | | | 164 | | | 196 | 197 | | 244 | 244 |

7/8/98

## Ordering Information



## Revisions

| Version | Description |
|---|---|
| 12/97 | Rev 5.0 added -3, -4 specification |
| 7/98 | Rev 5.1 added Spartan family to comparison, removed HQ304 |
| 11/98 | Rev 5.2 All specifications made final. |