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AMD Xilinx - XC5204-6TQ144C Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	120
Number of Logic Elements/Cells	480
Total RAM Bits	-
Number of I/O	117
Number of Gates	6000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc5204-6tq144c

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XC5200 Family Compared to XC4000/Spartan[™] and XC3000 Series

For readers already familiar with the XC4000/Spartan and XC3000 FPGA Families, this section describes significant differences between them and the XC5200 family. Unless otherwise indicated, comparisons refer to both XC4000/Spartan and XC3000 devices.

Configurable Logic Block (CLB) Resources

Each XC5200 CLB contains four independent 4-input function generators and four registers, which are configured as four independent Logic Cells[™] (LCs). The registers in each XC5200 LC are optionally configurable as edge-triggered D-type flip-flops or as transparent level-sensitive latches.

The XC5200 CLB includes dedicated carry logic that provides fast arithmetic carry capability. The dedicated carry logic may also be used to cascade function generators for implementing wide arithmetic functions.

XC4000 family: XC5200 devices have no wide edge decoders. Wide decoders are implemented using cascade logic. Although sacrificing speed for some designs, lack of wide edge decoders reduces the die area and hence cost of the XC5200.

XC4000/Spartan family: XC5200 dedicated carry logic differs from that of the XC4000/Spartan family in that the sum is generated in an additional function generator in the adjacent column. This design reduces XC5200 die size and hence cost for many applications. Note, however, that a loadable up/down counter requires the same number of function generators in both families. XC3000 has no dedicated carry.

XC4000/Spartan family: XC5200 lookup tables are optimized for cost and hence cannot implement RAM.

Input/Output Block (IOB) Resources

The XC5200 family maintains footprint compatibility with the XC4000 family, but not with the XC3000 family.

To minimize cost and maximize the number of I/O per Logic Cell, the XC5200 I/O does not include flip-flops or latches.

For high performance paths, the XC5200 family provides direct connections from each IOB to the registers in the adjacent CLB in order to emulate IOB registers.

Each XC5200 I/O Pin provides a programmable delay element to control input set-up time. This element can be used to avoid potential hold-time problems. Each XC5200 I/O Pin is capable of 8-mA source and sink currents.

IEEE 1149.1-type boundary scan is supported in each XC5200 I/O.

Table 2: Xilinx Field-Programmable Gate ArrayFamilies

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Parameter	XC5200	Spartan	XC4000	XC3000
CLB function generators	4	3	3	2
CLB inputs	20	9	9	5
CLB outputs	12	4	4	2
Global buffers	4	8	8	2
User RAM	no	yes	yes	no
Edge decoders	no	no	yes	no
Cascade chain	yes	no	no	no
Fast carry logic	yes	yes	yes	no
Internal 3-state	yes	yes	yes	yes
Boundary scan	yes	yes	yes	no
Slew-rate control	yes	yes	yes	yes

Routing Resources

The XC5200 family provides a flexible coupling of logic and local routing resources called the VersaBlock. The XC5200 VersaBlock element includes the CLB, a Local Interconnect Matrix (LIM), and direct connects to neighboring Versa-Blocks.

The XC5200 provides four global buffers for clocking or high-fanout control signals. Each buffer may be sourced by means of its dedicated pad or from any internal source.

Each XC5200 TBUF can drive up to two horizontal and two vertical Longlines. There are no internal pull-ups for XC5200 Longlines.

Configuration and Readback

The XC5200 supports a new configuration mode called Express mode.

XC4000/Spartan family: The XC5200 family provides a global reset but not a global set.

XC5200 devices use a different configuration process than that of the XC3000 family, but use the same process as the XC4000 and Spartan families.

XC3000 family: Although their configuration processes differ, XC5200 devices may be used in daisy chains with XC3000 devices.

XC3000 family: The XC5200 PROGRAM pin is a single-function input pin that overrides all other inputs. The PROGRAM pin does not exist in XC3000.

XC5200 Series Field Programmable Gate Arrays



Figure 10: 3-State Buffers Implement a Multiplexer

Input/Output Blocks

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

The I/O block, shown in Figure 11, consists of an input buffer and an output buffer. The output driver is an 8-mA full-rail CMOS buffer with 3-state control. Two slew-rate control modes are supported to minimize bus transients. Both the output buffer and the 3-state control are invertible. The input buffer has globally selected CMOS or TTL input thresholds. The input buffer is invertible and also provides a programmable delay line to assure reliable chip-to-chip set-up and hold times. Minimum ESD protection is 3 KV using the Human Body Model.



Figure 11: XC5200 I/O Block

IOB Input Signals

The XC5200 inputs can be globally configured for either TTL (1.2V) or CMOS thresholds, using an option in the bitstream generation software. There is a slight hysteresis of about 300mV.

The inputs of XC5200-Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC5200-Series device inputs are shown in Table 5.

Table 5: Supported Sources	for XC5200-Series	Device
Inputs		

	XC5200 Input Mode				
Source	5 V, TTL	5 V, CMOS			
Any device, Vcc = 3.3 V, CMOS outputs	\checkmark	Unreliable			
Any device, Vcc = 5 V, TTL outputs	\checkmark	Data			
Any device, Vcc = 5 V, CMOS outputs	\checkmark	\checkmark			

Optional Delay Guarantees Zero Hold Time

XC5200 devices do not have storage elements in the IOBs. However, XC5200 IOBs can be efficiently routed to CLB flip-flops or latches to store the I/O signals.

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the CLB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the CLB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the software default.

The XC5200 IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC5200 global clock buffers. (See "Global Lines" on page 96 for a description of the global clock buffers in the XC5200.) For a shorter input register setup time, with

non-zero hold, attach a NODELAY attribute or property to the flip-flop or input buffer.

IOB Output Signals

Output signals can be optionally inverted within the IOB, and pass directly to the pad. As with the inputs, a CLB flip-flop or latch can be used to store the output signal.

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The XC5200 devices provide a guaranteed output sink current of 8 mA.

Supported destinations for XC5200-Series device outputs are shown in Table 6.(For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 12.)

Table 6: Supported Destinations for XC5200-SeriesOutputs

	XC5200 Output Mode
Destination	5 V, CMOS
XC5200 device, V _{CC} =3.3 V, CMOS-threshold inputs	\checkmark
Any typical device, $V_{CC} = 3.3 V$, CMOS-threshold inputs	some ¹
Any device, V _{CC} = 5 V, TTL-threshold inputs	\checkmark
Any device, V _{CC} = 5 V, CMOS-threshold inputs	\checkmark

1. Only if destination device has 5-V tolerant inputs



Figure 12: Open-Drain Output

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop. For XC5200 devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For some XC5200 devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC5200 devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC5200 Series.

XC5200-Series devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Global Three-State

A separate Global 3-State line (not shown in Figure 11) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to Global Reset. See Figure 8 on page 90 for details. Alternatively, GTS can be driven from any internal node.

Other IOB Options

There are a number of other programmable options in the XC5200-Series IOB.

Pull-up and Pull-down Resistors

Programmable IOB pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls

segments span the width and height of the chip, respectively.

Two low-skew horizontal and vertical unidirectional global-line segments span each row and column of the chip, respectively.

Single- and Double-Length Lines

The single- and double-length bidirectional line segments make up the bulk of the routing channels. The double-length lines hop across every other CLB to reduce the propagation delays in speed-critical nets. Regenerating the signal strength is recommended after traversing three or four such segments. Xilinx place-and-route software automatically connects buffers in the path of the signal as necessary. Single- and double-length lines cannot drive onto Longlines and global lines; Longlines and global lines can, however, drive onto single- and double-length lines. As a general rule, Longline and global-line connections to the general routing matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

Longlines

Longlines are used for high-fan-out signals, 3-state busses, low-skew nets, and faraway destinations. Row and column splitter PIPs in the middle of the array effectively double the total number of Longlines by electrically dividing them into two separated half-lines. Longlines are driven by the 3-state buffers in each CLB, and are driven by similar buffers at the periphery of the array from the VersaRing I/O Interface.

Bus-oriented designs are easily implemented by using Longlines in conjunction with the 3-state buffers in the CLB and in the VersaRing. Additionally, weak keeper cells at the periphery retain the last valid logic level on the Longlines when all buffers are in 3-state mode.

Longlines connect to the single-length or double-length lines, or to the logic inside the CLB, through the General Routing Matrix. The only manner in which a Longline can be driven is through the four 3-state buffers; therefore, a Longline-to-Longline or single-line-to-Longline connection through PIPs in the General Routing Matrix is not possible. Again, as a general rule, long- and global-line connections to the General Routing Matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

The XC5200 family has no pull-ups on the ends of the Longlines sourced by TBUFs, unlike the XC4000 Series. Consequently, wired functions (i.e., WAND and WORAND) and wide multiplexing functions requiring pull-ups for undefined states (i.e., bus applications) must be implemented in a different way. In the case of the wired functions, the same functionality can be achieved by taking advantage of the carry/cascade logic described above, implementing a wide logic function in place of the wired function. In the case of 3-state bus applications, the user must insure that all states of the multiplexing function are defined. This process is as simple as adding an additional TBUF to drive the bus High when the previously undefined states are activated.

Global Lines

Global buffers in Xilinx FPGAs are special buffers that drive a dedicated routing network called Global Lines, as shown in Figure 16. This network is intended for high-fanout clocks or other control signals, to maximize speed and minimize skewing while distributing the signal to many loads.

The XC5200 family has a total of four global buffers (BUFG symbol in the library), each with its own dedicated routing channel. Two are distributed vertically and two horizontally throughout the FPGA.

The global lines provide direct input only to the CLB clock pins. The global lines also connect to the General Routing Matrix to provide access from these lines to the function generators and other control signals.

Four clock input pads at the corners of the chip, as shown in Figure 16, provide a high-speed, low-skew clock network to each of the four global-line buffers. In addition to the dedicated pad, the global lines can be sourced by internal logic. PIPs from several routing channels within the VersaRing can also be configured to drive the global-line buffers.

Details of all the programmable interconnect for a CLB is shown in Figure 17.



Figure 16: Global Lines

VersaRing Input/Output Interface

The VersaRing, shown in Figure 18, is positioned between the core logic and the pad ring; it has all the routing resources of a VersaBlock without the CLB logic. The VersaRing decouples the core logic from the I/O pads. Each VersaRing Cell provides up to four pad-cell connections on one side, and connects directly to the CLB ports on the other side.



Figure 18: VersaRing I/O Interface

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE boundary scan standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two. XC5200 devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP can also support two USERCODE instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output.

Boundary-scan operation is independent of individual IOB configuration and package type. All IOBs are treated as independently controlled bidirectional pins, including any unbonded IOBs. Retaining the bidirectional test capability after configuration provides flexibility for interconnect testing.

Also, internal signals can be captured during EXTEST by connecting them to unbonded IOBs, or to the unused outputs in IOBs used as unidirectional input pins. This technique partially compensates for the lack of INTEST support.

The user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: *"Boundary Scan in XC4000 and XC5200 Series devices"*

Figure 19 on page 99 is a diagram of the XC5200-Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

The public boundary-scan instructions are always available prior to configuration. After configuration, the public instructions and any USERCODE instructions are only available if specified in the design. While SAMPLE and BYPASS are available during configuration, it is recommended that boundary-scan operations not be performed during this transitory period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA device, and to read back the configuration data.

All of the XC4000 boundary-scan modes are supported in the XC5200 family. Three additional outputs for the User-Register are provided (Reset, Update, and Shift), repre-

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senting the decoding of the corresponding state of the boundary-scan internal state machine.



Figure 19: XC5200-Series Boundary Scan Logic



Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as 1 MHz (default), 6 MHz, or 12 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +50%.

Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/BUSY status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 28 on page 114. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. Figure 25 on page 109 shows the start-up timing for an XC5200-Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, XC4000, and XC5200 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. If the chain contains XC5200-Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in Figure 25 on page 109. Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of Figure 25. The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC5200-Series device, not reaching F means that readback cannot be initiated and most boundary scan instructions cannot be used.

The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using options in the bitstream generation software.

XC5200 devices always have the same number of CCLKs in the power up delay, independent of the configuration mode, unlike the XC3000/XC4000 Series devices. To guarantee all devices in a daisy chain have finished the power-up delay, tie the INIT pins together, as shown in Figure 27.

XC3000 Master with an XC5200-Series Slave

Some designers want to use an XC3000 lead device in peripheral mode and have the I/O pins of the XC5200-Series devices all available for user I/O. Figure 22 provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC5200-Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.



Table 11: XC5200 Bitstream Format

Data Type	Value	Occurrences				
Start Byte	11111110	Once per data				
Data Frame *	DATA(N-1:0)	frame				
Cyclic Redundancy Check or Constant Field Check	CRC(3:0) or 0110					
Fill Nibble	1111					
Extend Write Cycle	FFFFF					
Postamble	11111110	Once per de-				
Fill Bytes (30)	FFFFFF	vice				
Start-Up Byte	FF	Once per bit- stream				
*Bits per Frame (N) depends on device size, as described for table 11.						

Data Stream Format

The data stream ("bitstream") format is identical for all configuration modes, with the exception of Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode.

The data stream formats are shown in Table 11. Express mode data is shown with D0 at the left and D7 at the right. For all other modes, bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 12). Each frame begins with a start field and ends with an error check. In all modes except Express mode, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

In Express mode, only non-CRC error checking is supported. In all other modes, a selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the INIT pin. In Master modes,

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CCLK and address signals continue to operate externally. The user must detect INIT and initialize a new configuration by pulsing the PROGRAM pin Low or cycling Vcc.

Table 12: Internal Configuration Data Structure

Device	VersaBlock Array	PROM Size (bits)	Xilinx Serial PROM Needed
XC5202	8 x 8	42,416	XC1765E
XC5204	10 x 12	70,704	XC17128E
XC5206	14 x 14	106,288	XC17128E
XC5210	18 x 18	165,488	XC17256E
XC5215	22 x 22	237,744	XC17256E

Bits per Frame = $(34 \times \text{number of Rows}) + 28$ for the top + 28 for the bottom + 4 splitter bits + 8 start bits + 4 error check bits + 4 fill bits * + 24 extended write bits

= (34 x number of Rows) + 100

* In the XC5202 (8 x 8), there are 8 fill bits per frame, not 4 Number of Frames = (12 x number of Columns) + 7 for the left edge + 8 for the right edge + 1 splitter bit

= (12 x number of Columns) + 16

Program Data = (Bits per Frame x Number of Frames) + 48 header bits + 8 postamble bits + 240 fill bits + 8 start-up bits = (Bits per Frame x Number of Frames) + 304 PROM Size = Program Data

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 11. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the INIT pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 23. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture option not used). Statistically, one error out of 2048 might go undetected.

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F = Finished, no more configuration clocks needed Daisy-chain lead device must have latest F

Heavy lines describe default timing

X6700

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TO DIN OF OPTIONAL HIGH DAISY-CHAINED FPGAS or LOW 3.3 K N/C \sim N/C M1 M2 M0 TO CCLK OF OPTIONAL DAISY-CHAINED FPGAS CCLK DOUT NOTE:M0 can be shorted to Ground if not used as I/O. MO M1 M2 A17 XC5200 A16 DOUT DIN VCC Master EPROM Parallel A15 (8K x 8) (OR LARGER) CCLK ≶ X 4.7K A14 XC5200/ USER CONTROL OF HIGHER INIT A13 ORDER PROM ADDRESS BITS XC4000E/EX/ Spartan SLAVE CAN BE USED TO SELECT BETWEEN A12 A12 ALTERNATIVE CONFIGURATIONS A11 A11 PROGRAM A10 A10 PROGRAM A9 A9 DONE INIT \leftrightarrow D7 A8 A8 D6 A7 A7 D7 D5 A6 A6 D6 D4 A5 D5 A5 D3 A4 > A4 D4 D2 A3 D3 A3 D1 A2 D2 A2 D0 A1 A1 D1 A0 D0 A0 ŌE DONE > CE DATA BUS / 8 PROGRAM

Figure 31: Master Parallel Mode Circuit Diagram

X9004_01

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	Description	ę	Symbol	Min	Max	Units
	Delay to Address valid	1	T _{RAC}	0	200	ns
CCLK	Data setup time	2	T _{DRC}	60		ns
	Data hold time	3	T _{RCD}	0		ns

1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less then 25 ms, otherwise delay configuration by pulling PROGRAM Note: Low until V_{CC} is Valid.
The first Data byte is loaded and CCLK starts at the end of the first RCLK active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Figure 32: Master Parallel Mode Programming Switching Characteristics

Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/BUSY output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal

for test purposes. Note that RDY/BUSY is pulled High with a high-impedance pullup prior to INIT going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).



Figure 33: Synchronous Peripheral Mode Circuit Diagram



Pin Functions During Configuration Table 13.

CONFIGURATION MODE: <m2:m1:m0></m2:m1:m0>							
SLAVE <1:1:1>	MASTER-SER <0:0:0>	SYN.PERIPH <0:1:1>	ASYN.PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	EXPRESS <0:1:0>	OPERATION
	1		•	A16	A16		GCK1-I/O
				A17	A17		I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
			·				I/O
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	I/O
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	M0 (LOW) (I)	I/O
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (LOW) (I)	I/O
							GCK2-I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	I/O
							I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
				1	T	T	GCK3-I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
			CSO (I)				1/0
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
			RS (I)		//		1/0
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	1/0
				DATA 1 (I)	DATA 1 (I)	DATA1(I)	1/0
		RDY/BUSY	RDY/BUSY	RCLK	RCLK		1/0
DIN (I)	DIN (I)						1/0
							1/0
	CCLK (U)		CCLK (U)	CCLK (U)	CCLK (O)		
TDO	TDO	IDO		100	1DO	100	100-1/0
			VVS (I)	AU	AU		
			CS1 (I)	A1	A1	CS1 (I)	GCK4-I/O
			031(1)	A2 A2	A2		1/0
				A3	AJ		1/0
				Δ5	Δ5		1/0
				A6	A6		1/0
				Δ7	Δ7		1/0
				Δ <u>Α</u>	<u>A8</u>		1/0
				Δ9	A9		1/O
				A10	A10		1/O
				A11	A11		/O
				A12	A12		
				A13	A13		I/O
				A14	A14		/O
				A15	A15		I/O
							ALL OTHERS

Notes: 1. A shaded table cell represents a 20-kΩ to 100-kΩ pull-up resistor before and during configuration.
2. (I) represents an input (O) represents an output.
3. INIT is an open-drain output during configuration.



XC5200 CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Speed	d Grade	Grade -6		-5		-4		Ŷ	3
Description	Symbol	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)
Combinatorial Delays									
F inputs to X output	T _{IIO}		5.6		4.6		3.8		3.0
F inputs via transparent latch to Q	T _{ITO}		8.0		6.6		5.4		4.3
DI inputs to DO output (Logic-Cell	T _{IDO}		4.3		3.5		2.8		2.4
Feedthrough)									
F inputs via F5_MUX to DO output	T _{IMO}		7.2		5.8		5.0		4.3
Carry Delays									
Incremental delay per bit	T _{CY}		0.7		0.6		0.5		0.5
Carry-in overhead from DI	T _{CYDI}		1.8		1.6		1.5		1.4
Carry-in overhead from F	T _{CYL}		3.7		3.2		2.9		2.4
Carry-out overhead to DO	T _{CYO}		4.0		3.2		2.5		2.1
Sequential Delays									
Clock (CK) to out (Q) (Flip-Flop)	Тско		5.8		4.9		4.0		4.0
Gate (Latch enable) going active to out (Q)	T _{GO}		9.2		7.4		5.9		5.5
Set-up Time Before Clock (CK)									
F inputs	Т _{ICK}	2.3		1.8		1.4		1.3	
F inputs via F5_MUX	T _{MICK}	3.8		3.0		2.5		2.4	
DI input	T _{DICK}	0.8		0.5		0.4		0.4	
CE input	T _{EICK}	1.6		1.2		0.9		0.9	
Hold Times After Clock (CK)									
F inputs	Тскі	0		0		0		0	
F inputs via F5_MUX	Тскмі	0		0		0		0	
DI input	T _{CKDI}	0		0		0		0	
CE input	T _{CKEI}	0		0		0		0	
Clock Widths									
Clock High Time	T _{CH}	6.0		6.0		6.0		6.0	
Clock Low Time	T _{CL}	6.0		6.0		6.0		6.0	
Toggle Frequency (MHz) (Note 3)	F _{TOG}		83		83		83		83
Reset Delays									
Width (High)	T _{CLRW}	6.0		6.0		6.0		6.0	
Delay from CLR to Q (Flip-Flop)	T _{CLR}		7.7		6.3		5.1		4.0
Delay from CLR to Q (Latch)	T _{CLRL}		6.5		5.2		4.2		3.0
Global Reset Delays									
Width (High)	T _{GCLRW}	6.0		6.0		6.0		6.0	
Delay from internal GR to Q	T _{GCLR}		14.7		12.1		9.1		8.0

Note: 1. The CLB K to Q output delay (T_{CKO}) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold-time requirement (T_{CKDI}) of any CLB on the same die.
2. Timing is based upon the XC5215 device. For other devices, see Timing Calculator.

3. Maximum flip-flop toggle rate for export control purposes.

XC5200 Boundary Scan (JTAG) Switching Characteristic Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC5200 devices unless otherwise noted.

Speed Grade		-	-6		-5		-4		-3	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Setup and Hold										
Input (TDI) to clock (TCK) setup time	T _{TDITCK}	30.0		30.0		30.0		30.0		
Input (TDI) to clock (TCK) hold time	Т _{ТСКТОІ}	0		0		0		0		
Input (TMS) to clock (TCK) setup time	T _{TMSTCK}	15.0		15.0		15.0		15.0		
Input (TMS) to clock (TCK) hold time	Т _{ТСКТМЅ}	0		0		0		0		
Propagation Delay										
Clock (TCK) to Pad (TDO)	T _{TCKPO}		30.0		30.0		30.0		30.0	
Clock										
Clock (TCK) High	Т _{ТСКН}	30.0		30.0		30.0		30.0		
Clock (TCK) Low	T _{TCKL}	30.0		30.0		30.0		30.0		
F _{MAX} (MHz)	F _{MAX}		10.0		10.0		10.0		10.0	

Note 1: Input pad setup and hold times are specified with respect to the internal clock.

XC5200 Series Field Programmable Gate Arrays

<7	VII	I IN	۱V®
<⊾			IV.

Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
35.	I/O (HDC)	19	36	31	28	40	D14	204
36.	I/O	-	-	32	29	43	E14	207
37.	I/O (LDC)	20	37	33	30	44	C16	210
	GND	-	-	-	-	45	F14	-
38.	I/O	-	38	34	31	48	F16	216
39.	I/O	21	39	35	32	49	G14	219
40.	I/O	-	-	36	33	50	G15	222
41.	I/O	-	-	37	34	51	G16	228
42.	I/O	22	40	38	35	52	H16	231
43.	I/O (ERR, INIT)	23	41	39	36	53	H15	234
	VCC	24	42	40	37	54	H14	-
	GND	25	43	41	38	55	J14	-
44.	I/O	26	44	42	39	56	J15	240
45.	I/O	27	45	43	40	57	J16	243
46.	I/O	-	-	44	41	58	K16	246
47.	I/O	-	-	45	42	59	K15	252
48.	I/O	28	46	46	43	60	K14	255
49.	I/O	29	47	47	44	61	L16	258
	GND	-	-	-	-	64	L14	-
50.	I/O	-	48	48	45	65	P16	264
51.	I/O	30	49	49	46	66	M14	267
52.	I/O	-	50	50	47	69	N14	276
53.	I/O	31	51	51	48	70	R16	279
	GND	-	52	52	49	71	P14	
	DONE	32	53	53	50	72	R15	
	VCC	33	54	54	51	73	P13	_
	PROG	34	55	55	52	74	R14	-
54.	I/O (D7)	35	56	56	53	75	T16	288
55.	GCK3 (I/O)	36	57	57	54	76	T15	291
56.	I/O (D6)	37	58	58	55	79	T14	300
57.	I/O	-	-	59	56	80	T13	303
	GND	-	-	-	-	81	P11	-
58.	I/O (D5)	38	59	60	57	84	T10	306
59.	$I/O(\overline{CS0})$	-	60	61	58	85	P10	312
60.	I/O	-	-	62	59	86	R10	315
61.	1/0	-	-	63	60	87	Т9	318
62.	I/O (D4)	39	61	64	61	88	R9	324
63.	1/0	-	62	65	62	89	P9	327
	VCC	40	63	66	63	90	R8	-
	GND	41	64	67	64	91	P8	-
64.	I/O (D3)	42	65	68	65	92	T8	336
65.	$I/O(\overline{RS})$	43	66	69	66	93	T7	339
66.	I/O	-	-	70	67	94	T6	342
67.	I/O	-	-	-	-	95	R7	348
68	I/O (D2)	44	67	71	68	96	P7	351
69	1/0	-	68	72	69	97	T5	360
	GND	-	-	-	-	100	P6	-
70	I/O (D1)	45	69	73	70	101	T3	363
71	1/0	-	70	74	71	102	P5	366
	(RCLK-BUSY/RDY)						. 0	
72.	I/O (D0, DIN)	46	71	75	72	105	P4	372
73.	I/O (DOUT)	47	72	76	73	106	T2	375

XC5200 Series Field Programmable Gate Arrays

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Pin	Description	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
99.	I/O	68	72	69	97	T5	107	486
100.	I/O	-	-	-	98	R6	108	492
101.	I/O	-	-	-	99	T4	109	495
	GND	-	-	-	100	P6	110	-
102.	I/O (D1)	69	73	70	101	T3	113	498
103.	I <u>/O</u> (RCLK-BUSY/RDY)	70	74	71	102	P5	114	504
104.	I/O	-	-	-	103	R4	115	507
105.	I/O	-	-	-	104	R3	116	510
106.	I/O (D0, DIN)	71	75	72	105	P4	117	516
107.	I/O (DOUT)	72	76	73	106	T2	118	519
	CCLK	73	77	74	107	R2	119	-
	VCC	74	78	75	108	P3	120	-
108.	I/O (TDO)	75	79	76	109	T1	121	0
	GND	76	80	77	110	N3	122	-
109.	I/O (A0, WS)	77	81	78	111	R1	123	9
110.	GCK4 (A1, I/O)	78	82	79	112	P2	124	15
111.	I/O	-	-	-	113	N2	125	18
112.	I/O	-	-	-	114	M3	126	21
113.	I/O (A2, CS1)	79	83	80	115	P1	127	27
114.	I/O (A3)	80	84	81	116	N1	128	30
115.	I/O	-	-	-	117	M2	129	33
116.	I/O	-	-	-	-	M1	130	39
	GND	-	-	-	118	L3	131	-
117.	I/O	-	-	-	119	L2	132	42
118.	I/O	-	-	-	120	L1	133	45
119.	I/O (A4)	81	85	82	121	K3	134	51
120.	I/O (A5)	82	86	83	122	K2	135	54
121.	I/O	-	87	84	123	K1	137	57
122.	I/O	-	88	85	124	J1	138	63
123.	I/O (A6)	83	89	86	125	J2	139	66
124.	I/O (A7)	84	90	87	126	J3	140	69
	GND	1	91	88	127	H2	141	-

Additional No Connect (N.C.) Connections for PQ160 Package

		PQ160		
8	30	89	111	136
9	31	90	112	

Notes: Boundary Scan Bit 0 = TDO.T Boundary Scan Bit 1 = TDO.O Boundary Scan Bit 1056 = BSCAN.UPD



Pin Locations for XC5206 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	VCC	2	92	89	128	142	155	J4	183	-
1.	I/O (A8)	3	93	90	129	143	156	J3	184	87
2.	I/O (A9)	4	94	91	130	144	157	J2	185	90
3.	I/O	-	95	92	131	145	158	J1	186	93
4.	I/O	-	96	93	132	146	159	H1	187	99
5.	I/O	-	-	-	-	-	160	H2	188	102
6.	I/O	-	-	-	-	-	161	H3	189	105
7.	I/O (A10)	5	97	94	133	147	162	G1	190	111
8.	I/O (A11)	6	98	95	134	148	163	G2	191	114
9.	I/O	-	-	-	135	149	164	F1	192	117
10.	I/O	-	-	-	136	150	165	E1	193	123
	GND	-	-	-	137	151	166	G3	194	-
11.	I/O	-	-	-	-	152	168	C1	197	126
12.	I/O	-	-	-	-	153	169	E2	198	129
13.	I/O (A12)	7	99	96	138	154	170	F3	199	138
14.	I/O (A13)	8	100	97	139	155	171	D2	200	141
15.	I/O	-	-	-	140	156	172	B1	201	150
16.	I/O	-	-	-	141	157	173	E3	202	153
17.	I/O (A14)	9	1	98	142	158	174	C2	203	162
18.	I/O (A15)	10	2	99	143	159	175	B2	204	165
	VCC	11	3	100	144	160	176	D3	205	-
	GND	12	4	1	1	1	1	D4	2	-
19.	GCK1 (A16, I/O)	13	5	2	2	2	2	C3	4	174
20.	I/O (A17)	14	6	3	3	3	3	C4	5	177
21.	I/O	-	-	-	4	4	4	B3	6	183
22.	I/O	-	-	-	5	5	5	C5	7	186
23.	I/O (TDI)	15	7	4	6	6	6	A2	8	189
24.	I/O (TCK)	16	8	5	7	7	7	B4	9	195
25.	I/O	-	-	-	-	8	8	C6	10	198
26.	I/O	-	-	-	-	9	9	A3	11	201
	GND	-	-	-	8	10	10	C7	14	-
27.	I/O	-	-	-	9	11	11	A4	15	207
28.	I/O	-	-	-	10	12	12	A5	16	210
29.	I/O (TMS)	17	9	6	11	13	13	B7	17	213
30.	I/O	18	10	7	12	14	14	A6	18	219
31.	I/O	-	-	-	-	-	15	C8	19	222
32.	I/O	-	-	-	-	-	16	A7	20	225
33.	I/O	-	-	-	13	15	17	B8	21	234
34.	I/O	-	11	8	14	16	18	A8	22	237
35.	I/O	19	12	9	15	17	19	B9	23	246
36.	I/O	20	13	10	16	18	20	C9	24	249
	GND	21	14	11	17	19	21	D9	25	-
	VCC	22	15	12	18	20	22	D10	26	-
37.	I/O	23	16	13	19	21	23	C10	27	255
38.	I/O	24	17	14	20	22	24	B10	28	258
39.	I/O	-	18	15	21	23	25	A9	29	261
40.	I/O	-	-	-	22	24	26	A10	30	267
41.	I/O	-	-	-	-	-	27	A11	31	270

XC5200 Series Field Programmable Gate Arrays



Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
100.	I/O	-	-	-	F17	-	AE22	558
101.	I/O	-	-	-	G16	-	AF23	564
102.	I/O	49	63	69	D19	K7	AD20	567
103.	I/O	50	64	70	E18	M5	AE21	570
104.	I/O	-	65	71	D20	R4	AF21	576
105.	I/O	-	66	72	G17	N5	AC19	579
106.	I/O	-	-	73	F18	P5	AD19	582
107.	I/O	-	-	74	H16	L6	AE20	588
108.	I/O	-	-	-	E19	-	AF20	591
109.	I/O	-	-	-	F19	-	AC18	594
	GND	51	67	75	E20	GND*	GND*	-
110.	I/O	52	68	76	H17	R5	AD18	600
111.	I/O	53	69	77	G18	M6	AE19	603
112.	I/O	54	70	78	G19	N6	AC17	606
113.	I/O	55	71	79	H18	P6	AD17	612
	VCC	-	-	80	F20	VCC*	VCC*	-
114.	I/O	-	72	81	J16	R6	AE17	615
115.	I/O	-	73	82	G20	M7	AE16	618
116.	I/O	-	-	-	H20	-	AF16	624
117.	I/O	-	-	-	J18	-	AC15	627
118.	I/O	-	-	84	J19	N7	AD15	630
119.	1/Q	-	_	85	K16	P7	AF15	636
120.	1/Q	56	74	86	.120	R7	AF15	639
121.	1/Q	57	75	87	K17	17	AD14	642
122	1/0	58	76	88	K18	 N8	AF14	648
122.		59	77	89	K19	P8	AF14	651
120.	VCC	60	78	90	1.20	VCC*		-
	GND	61	79	91	K20	GND*	GND*	_
124	1/0	62	80	92	119	18	AF13	660
125	1/0	63	81	02	118	PQ	AC13	663
120.	1/0	64	82	94 94	116	RQ	AD13	672
120.		65	83	95	117	NG	ΔE12	675
127.		-	84	96	M20	MQ		678
120.		_	85	97	M1Q	10		684
120.		_		57	N20		AC12	687
130.		_		_	M18		ΔE11	690
132				00	N10	P10		696
133				100	P20	P10		699
100.				101	T20			-
13/	1/0			107	N18	N10		702
134.	1/0	67	87	102	D10	KO		702
135.	1/0	68	07	103	F 19 N17	P11	AC10	708
130.	1/0	60	80	104	P10	D11	AC10	711
137.		70	09	105	R 19 R 20			/ 14
120		70	90	001	N16	GND		-
130.	1/0	-	-	-		-		722
139.	1/0	-	-	-	F 10	- M10		123
140.	1/0	-	-	107	D20	NI 1	ACS	720
141.	1/0	-	-	100	T10			1.52
142.	1/0	-	91	109	D10	rt I Z		739
143.	1/0	- 74	92	110				744
144.	1/0	71	93	110	10	riz Maa		744
145.		72	94	112	v20	IV111	AE5	/4/



Revisions

Version	Description
12/97	Rev 5.0 added -3, -4 specification
7/98	Rev 5.1 added Spartan family to comparison, removed HQ304
11/98	Rev 5.2 All specifications made final.