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### AMD Xilinx - XC5206-5TQ144C Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	784
Total RAM Bits	-
Number of I/O	117
Number of Gates	10000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc5206-5tq144c

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## XC5200 Family Compared to XC4000/Spartan<sup>™</sup> and XC3000 Series

For readers already familiar with the XC4000/Spartan and XC3000 FPGA Families, this section describes significant differences between them and the XC5200 family. Unless otherwise indicated, comparisons refer to both XC4000/Spartan and XC3000 devices.

### Configurable Logic Block (CLB) Resources

Each XC5200 CLB contains four independent 4-input function generators and four registers, which are configured as four independent Logic Cells<sup>™</sup> (LCs). The registers in each XC5200 LC are optionally configurable as edge-triggered D-type flip-flops or as transparent level-sensitive latches.

The XC5200 CLB includes dedicated carry logic that provides fast arithmetic carry capability. The dedicated carry logic may also be used to cascade function generators for implementing wide arithmetic functions.

*XC4000 family:* XC5200 devices have no wide edge decoders. Wide decoders are implemented using cascade logic. Although sacrificing speed for some designs, lack of wide edge decoders reduces the die area and hence cost of the XC5200.

*XC4000/Spartan family:* XC5200 dedicated carry logic differs from that of the XC4000/Spartan family in that the sum is generated in an additional function generator in the adjacent column. This design reduces XC5200 die size and hence cost for many applications. Note, however, that a loadable up/down counter requires the same number of function generators in both families. XC3000 has no dedicated carry.

*XC4000/Spartan family:* XC5200 lookup tables are optimized for cost and hence cannot implement RAM.

### Input/Output Block (IOB) Resources

The XC5200 family maintains footprint compatibility with the XC4000 family, but not with the XC3000 family.

To minimize cost and maximize the number of I/O per Logic Cell, the XC5200 I/O does not include flip-flops or latches.

For high performance paths, the XC5200 family provides direct connections from each IOB to the registers in the adjacent CLB in order to emulate IOB registers.

Each XC5200 I/O Pin provides a programmable delay element to control input set-up time. This element can be used to avoid potential hold-time problems. Each XC5200 I/O Pin is capable of 8-mA source and sink currents.

IEEE 1149.1-type boundary scan is supported in each XC5200 I/O.

## Table 2: Xilinx Field-Programmable Gate ArrayFamilies

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Parameter	XC5200	Spartan	XC4000	XC3000
CLB function generators	4	3	3	2
CLB inputs	20	9	9	5
CLB outputs	12	4	4	2
Global buffers	4	8	8	2
User RAM	no	yes	yes	no
Edge decoders	no	no	yes	no
Cascade chain	yes	no	no	no
Fast carry logic	yes	yes	yes	no
Internal 3-state	yes	yes	yes	yes
Boundary scan	yes	yes	yes	no
Slew-rate control	yes	yes	yes	yes

### Routing Resources

The XC5200 family provides a flexible coupling of logic and local routing resources called the VersaBlock. The XC5200 VersaBlock element includes the CLB, a Local Interconnect Matrix (LIM), and direct connects to neighboring Versa-Blocks.

The XC5200 provides four global buffers for clocking or high-fanout control signals. Each buffer may be sourced by means of its dedicated pad or from any internal source.

Each XC5200 TBUF can drive up to two horizontal and two vertical Longlines. There are no internal pull-ups for XC5200 Longlines.

### **Configuration and Readback**

The XC5200 supports a new configuration mode called Express mode.

*XC4000/Spartan family:* The XC5200 family provides a global reset but not a global set.

XC5200 devices use a different configuration process than that of the XC3000 family, but use the same process as the XC4000 and Spartan families.

*XC3000 family:* Although their configuration processes differ, XC5200 devices may be used in daisy chains with XC3000 devices.

*XC3000 family:* The XC5200 PROGRAM pin is a single-function input pin that overrides all other inputs. The PROGRAM pin does not exist in XC3000.

non-zero hold, attach a NODELAY attribute or property to the flip-flop or input buffer.

### **IOB Output Signals**

Output signals can be optionally inverted within the IOB, and pass directly to the pad. As with the inputs, a CLB flip-flop or latch can be used to store the output signal.

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The XC5200 devices provide a guaranteed output sink current of 8 mA.

Supported destinations for XC5200-Series device outputs are shown in Table 6.(For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 12.)

## Table 6: Supported Destinations for XC5200-SeriesOutputs

	XC5200 Output Mode
Destination	5 V, CMOS
XC5200 device, V <sub>CC</sub> =3.3 V, CMOS-threshold inputs	$\checkmark$
Any typical device, $V_{CC} = 3.3 V$ , CMOS-threshold inputs	some <sup>1</sup>
Any device, V <sub>CC</sub> = 5 V, TTL-threshold inputs	$\checkmark$
Any device, V <sub>CC</sub> = 5 V, CMOS-threshold inputs	$\checkmark$

1. Only if destination device has 5-V tolerant inputs



Figure 12: Open-Drain Output

### **Output Slew Rate**

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop. For XC5200 devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For some XC5200 devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC5200 devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC5200 Series.

XC5200-Series devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

### **Global Three-State**

A separate Global 3-State line (not shown in Figure 11) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to Global Reset. See Figure 8 on page 90 for details. Alternatively, GTS can be driven from any internal node.

### Other IOB Options

There are a number of other programmable options in the XC5200-Series IOB.

### Pull-up and Pull-down Resistors

Programmable IOB pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls

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Figure 17: Detail of Programmable Interconnect Associated with XC5200 Series CLB

### VersaRing Input/Output Interface

The VersaRing, shown in Figure 18, is positioned between the core logic and the pad ring; it has all the routing resources of a VersaBlock without the CLB logic. The VersaRing decouples the core logic from the I/O pads. Each VersaRing Cell provides up to four pad-cell connections on one side, and connects directly to the CLB ports on the other side.



Figure 18: VersaRing I/O Interface

## **Boundary Scan**

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE boundary scan standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two. XC5200 devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP can also support two USERCODE instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output.

Boundary-scan operation is independent of individual IOB configuration and package type. All IOBs are treated as independently controlled bidirectional pins, including any unbonded IOBs. Retaining the bidirectional test capability after configuration provides flexibility for interconnect testing.

Also, internal signals can be captured during EXTEST by connecting them to unbonded IOBs, or to the unused outputs in IOBs used as unidirectional input pins. This technique partially compensates for the lack of INTEST support.

The user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: *"Boundary Scan in XC4000 and XC5200 Series devices"* 

Figure 19 on page 99 is a diagram of the XC5200-Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

The public boundary-scan instructions are always available prior to configuration. After configuration, the public instructions and any USERCODE instructions are only available if specified in the design. While SAMPLE and BYPASS are available during configuration, it is recommended that boundary-scan operations not be performed during this transitory period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA device, and to read back the configuration data.

All of the XC4000 boundary-scan modes are supported in the XC5200 family. Three additional outputs for the User-Register are provided (Reset, Update, and Shift), repre-

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### **XC5200 Series Field Programmable Gate Arrays**

senting the decoding of the corresponding state of the boundary-scan internal state machine.



Figure 19: XC5200-Series Boundary Scan Logic

#### Table 9: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Unrestricted L	Jser-Prog	rammabl	e I/O Pins
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor ( $20 \text{ k}\Omega - 100 \text{ k}\Omega$ ) that defines the logic level as High.

## Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC5200-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

### **Special Purpose Pins**

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary I/O connections. The development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC5200-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 k $\Omega$ .) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of  $3.3k\Omega$  is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

### **Configuration Modes**

XC5200 devices have seven configuration modes. These modes are selected by a 3-bit input code applied to the M2,

M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode,

#### **Table 10: Configuration Modes**

Mode	M2	M1	MO	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note :\*Peripheral Synchronous can be considered byte-wide Slave Parallel

which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration. The coding for mode selection is shown in Table 10.

Note that the smallest package, VQ64, only supports the Master Serial, Slave Serial, and Express modes. A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 13 on page 124.

### Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The



### **Master Serial Mode**

In Master Serial mode, the CCLK output of the lead FPGA drives a Xilinx Serial PROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The lead FPGA accepts this data on the subsequent rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In the bitstream generation software, the user can specify Fast ConfigRate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of twelve. The value increases from a nominal 1 MHz, to a nominal 12 MHz. Be sure that the serial PROM and slaves are fast enough to support this data rate. The Medium ConfigRate option changes the frequency to a nominal 6 MHz. XC2000, XC3000/A, and XC3100A devices do not support the Fast or Medium ConfigRate options.

The SPROM CE input can be driven from either LDC or DONE. Using LDC avoids potential contention on the DIN pin, if this pin is configured as user-I/O, but LDC is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the DONE before I/O enable option is invoked.

Figure 28 on page 114 shows a full master/slave system. The leftmost device is in Master Serial mode.

Master Serial mode is selected by a <000> on the mode pins (M2, M1, M0).



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	Т <sub>DSCK</sub>	20		ns
COLK	DIN hold	2	T <sub>CKDS</sub>	0		ns

Notes: 1. At power-up, Vcc must rise from 2.0 V to Vcc min in less than 25 ms, otherwise delay configuration by pulling PROGRAM Low until Vcc is valid.

2. Master Serial mode timing is based on testing in slave mode.

#### Figure 30: Master Serial Mode Programming Switching Characteristics

In the two Master Parallel modes, the lead FPGA directly addresses an industry-standard byte-wide EPROM, and accepts eight data bits just before incrementing or decrementing the address outputs.

The eight data bits are serialized in the lead FPGA, which then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 1.5 CCLK periods, after the rising CCLK edge that accepts a byte of data (and also changes the EPROM address) until the falling CCLK edge that makes the LSB (D0) of this byte appear at DOUT. This means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. The PROM address pins can be incremented or decremented, depending on the mode pin settings. This option allows the FPGA to share the PROM with a wide variety of microprocessors and microcontrollers. Some processors must boot from the bottom of memory (all zeros) while others must boot from the top. The FPGA is flexible and can load its configuration bitstream from either end of the memory.

Master Parallel Up mode is selected by a <100> on the mode pins (M2, M1, M0). The EPROM addresses start at 00000 and increment.

Master Parallel Down mode is selected by a <110> on the mode pins. The EPROM addresses start at 3FFFF and decrement.

### **XC5200 Series Field Programmable Gate Arrays**

TO DIN OF OPTIONAL HIGH DAISY-CHAINED FPGAS or LOW 3.3 K N/C  $\sim$ N/C M1 M2 M0 TO CCLK OF OPTIONAL DAISY-CHAINED FPGAS CCLK DOUT NOTE:M0 can be shorted to Ground if not used as I/O. MO M1 M2 A17 XC5200 A16 DOUT DIN VCC Master EPROM Parallel A15 (8K x 8) (OR LARGER) CCLK ≶ X 4.7K A14 XC5200/ USER CONTROL OF HIGHER INIT A13 ORDER PROM ADDRESS BITS XC4000E/EX/ Spartan SLAVE CAN BE USED TO SELECT BETWEEN A12 A12 ALTERNATIVE CONFIGURATIONS A11 A11 PROGRAM A10 A10 PROGRAM A9 A9 DONE INIT  $\leftrightarrow$ D7 A8 A8 D6 A7 A7 D7 D5 A6 A6 D6 D4 A5 D5 A5 D3 A4 > A4 D4 D2 A3 D3 A3 D1 A2 D2 A2 D0 A1 A1 D1 A0 D0 A0 ŌE DONE > CE DATA BUS / 8 PROGRAM

Figure 31: Master Parallel Mode Circuit Diagram

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### **XC5200 Series Field Programmable Gate Arrays**



	Description	ę	Symbol	Min	Max	Units
	Delay to Address valid	1	T <sub>RAC</sub>	0	200	ns
CCLK	Data setup time	2	T <sub>DRC</sub>	60		ns
	Data hold time	3	T <sub>RCD</sub>	0		ns

1. At power-up, V<sub>CC</sub> must rise from 2.0 V to V<sub>CC</sub> min in less then 25 ms, otherwise delay configuration by pulling PROGRAM Note: Low until V<sub>CC</sub> is Valid.
 The first Data byte is loaded and CCLK starts at the end of the first RCLK active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

### Figure 32: Master Parallel Mode Programming Switching Characteristics

### **Asynchronous Peripheral Mode**

### Write to FPGA

Asynchronous Peripheral mode uses the trailing edge of the logic AND condition of WS and CS0 being Low and RS and CS1 being High to accept byte-wide data from a microprocessor bus. In the lead FPGA, this data is loaded into a double-buffered UART-like parallel-to-serial converter and is serially shifted into the internal logic.

The lead FPGA presents the preamble data (and all data that overflows the lead device) on its DOUT pin. The RDY/BUSY output from the lead FPGA acts as a hand-shake signal to the microprocessor. RDY/BUSY goes Low when a byte has been received, and goes High again when the byte-wide input buffer has transferred its information into the shift register, and the buffer is ready to receive new data. A new write may be started immediately, as soon as the RDY/BUSY output has gone Low, acknowledging receipt of the previous data. Write may not be terminated until RDY/BUSY is High again for one CCLK period. Note that RDY/BUSY is pulled High with a high-impedance pull-up prior to INIT going High.

The length of the BUSY signal depends on the activity in the UART. If the shift register was empty when the new byte was received, the BUSY signal lasts for only two CCLK periods. If the shift register was still full when the new byte was received, the BUSY signal can be as long as nine CCLK periods.

Note that after the last byte has been entered, only seven of its bits are shifted out. CCLK remains High with DOUT equal to bit 6 (the next-to-last bit) of the last byte entered. The READY/BUSY handshake can be ignored if the delay from any one Write to the end of the next Write is guaranteed to be longer than 10 CCLK periods.

### Status Read

The logic AND condition of the  $\overline{CS0}$ , CS1 and  $\overline{RS}$  inputs puts the device status on the Data bus.

- D7 High indicates Ready
- D7 Low indicates Busy
- D0 through D6 go unconditionally High

It is mandatory that the whole start-up sequence be started and completed by one byte-wide input. Otherwise, the pins used as Write Strobe or Chip Enable might become active outputs and interfere with the final byte transfer. If this transfer does not occur, the start-up sequence is not completed all the way to the finish (point F in Figure 25 on page 109).

In this case, at worst, the internal reset is not released. At best, Readback and Boundary Scan are inhibited. The length-count value, as generated by the software, ensures that these problems never occur.

Although RDY/BUSY is brought out as a separate signal, microprocessors can more easily read this information on one of the data lines. For this purpose, D7 represents the RDY/BUSY status when RS is Low, WS is High, and the two chip select lines are both active.

Asynchronous Peripheral mode is selected by a <101> on the mode pins (M2, M1, M0).



Figure 35: Asynchronous Peripheral Mode Circuit Diagram



#### **Pin Functions During Configuration** Table 13.

CONFIGURATION MODE: <m2:m1:m0></m2:m1:m0>									
SLAVE <1:1:1>	MASTER-SER <0:0:0>	SYN.PERIPH <0:1:1>	ASYN.PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	EXPRESS <0:1:0>	OPERATION		
	1		•	A16	A16		GCK1-I/O		
				A17	A17		I/O		
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O		
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O		
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O		
			·				I/O		
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	I/O		
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	M0 (LOW) (I)	I/O		
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (LOW) (I)	I/O		
							GCK2-I/O		
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O		
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O		
INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	INIT-ERROR	I/O		
							I/O		
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE		
PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM (I)	PROGRAM		
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O		
				1	T	T	GCK3-I/O		
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O		
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O		
			CSO (I)				1/0		
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O		
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O		
			RS (I)		//		1/0		
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	1/0		
				DATA 1 (I)	DATA 1 (I)	DATA1(I)	1/0		
		RDY/BUSY	RDY/BUSY	RCLK	RCLK		1/0		
DIN (I)	DIN (I)						1/0		
							1/0		
	CCLK (U)		CCLK (U)	CCLK (U)	CCLK (O)				
TDO	TDO	IDO		100	1DO	100	100-1/0		
			VVS (I)	AU	AU				
			CS1 (I)	A1	A1	CS1 (I)	GCK4-I/O		
			031(1)	A2 A2	A2		1/0		
				A3	AJ		1/0		
				Δ5	Δ5		1/0		
				A6	A6		1/0		
				Δ7	Δ7		1/0		
				Δ <u>Α</u>	<u>A8</u>		1/0		
				Α9	A9		1/O		
				A10	A10		1/O		
				A11	A11		/O		
				A12	A12				
				A13	A13		I/O		
				A14	A14		/O		
				A15	A15		I/O		
							ALL OTHERS		

Notes: 1. A shaded table cell represents a 20-kΩ to 100-kΩ pull-up resistor before and during configuration.
 2. (I) represents an input (O) represents an output.
 3. INIT is an open-drain output during configuration.

### XC5200 Boundary Scan (JTAG) Switching Characteristic Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC5200 devices unless otherwise noted.

Speed Grade		-	6	-5		-4		-3	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
Setup and Hold									
Input (TDI) to clock (TCK) setup time	T <sub>TDITCK</sub>	30.0		30.0		30.0		30.0	
Input (TDI) to clock (TCK) hold time	Т <sub>ТСКТОІ</sub>	0		0		0		0	
Input (TMS) to clock (TCK) setup time	T <sub>TMSTCK</sub>	15.0		15.0		15.0		15.0	
Input (TMS) to clock (TCK) hold time	Т <sub>ТСКТМЅ</sub>	0		0		0		0	
Propagation Delay									
Clock (TCK) to Pad (TDO)	T <sub>TCKPO</sub>		30.0		30.0		30.0		30.0
Clock									
Clock (TCK) High	Т <sub>ТСКН</sub>	30.0		30.0		30.0		30.0	
Clock (TCK) Low	T <sub>TCKL</sub>	30.0		30.0		30.0		30.0	
F <sub>MAX</sub> (MHz)	F <sub>MAX</sub>		10.0		10.0		10.0		10.0

Note 1: Input pad setup and hold times are specified with respect to the internal clock.



### **XC5200 Series Field Programmable Gate Arrays**

Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	CCLK	48	73	77	74	107	R2	-
	VCC	-	74	78	75	108	P3	-
74.	I/O (TDO)	49	75	79	76	109	T1	0
	GND	-	76	80	77	110	N3	-
75.	I/O (A0, WS)	50	77	81	78	111	R1	9
76.	GCK4 (A1, I/O)	51	78	82	79	112	P2	15
77.	I/O (A2, CS1)	52	79	83	80	115	P1	18
78.	I/O (A3)	-	80	84	81	116	N1	21
	GND	-	-	-	-	118	L3	-
79.	I/O (A4)	-	81	85	82	121	K3	27
80.	I/O (A5)	53	82	86	83	122	K2	30
81.	I/O	-	-	87	84	123	K1	33
82.	I/O	-	-	88	85	124	J1	39
83.	I/O (A6)	54	83	89	86	125	J2	42
84.	I/O (A7)	55	84	90	87	126	J3	45
	GND	56	1	91	88	127	H2	-

\* VQ64 package supports Master Serial, Slave Serial, and Express configuration modes only.

### Additional No Connect (N.C.) Connections on TQ144 Package

	TQ144											
135	9	41	67	98	117							
136	10	42	68	99	119							
140	25	46	77	103	120							
141	26	47	78	104								
4	30	62	82	113								
5	31	63	83	114								

**Notes:** Boundary Scan Bit 0 = TDO.T Boundary Scan Bit 1 = TDO.O

Boundary Scan Bit 1056 = BSCAN.UPD

### Pin Locations for XC5204 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
	VCC	2	92	89	128	H3	142	-
1.	I/O (A8)	3	93	90	129	H1	143	78
2.	I/O (A9)	4	94	91	130	G1	144	81
3.	I/O	-	95	92	131	G2	145	87
4.	I/O	-	96	93	132	G3	146	90
5.	I/O (A10)	5	97	94	133	F1	147	93
6.	I/O (A11)	6	98	95	134	F2	148	99
7.	I/O	-	-	-	135	E1	149	102
8.	I/O	-	-	-	136	E2	150	105
	GND	-	-	-	137	F3	151	-
9.	I/O	-	-	-	-	D1	152	111
10.	I/O	-	-	-	-	D2	153	114
11.	I/O (A12)	7	99	96	138	E3	154	117
12.	I/O (A13)	8	100	97	139	C1	155	123
13.	I/O	-	-	-	140	C2	156	126

### XC5200 Series Field Programmable Gate Arrays

## **∑**XILINX<sup>®</sup>

Pin	Description	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
14.	I/O	-	-	-	141	D3	157	129
15.	I/O (A14)	9	1	98	142	B1	158	138
16.	I/O (A15)	10	2	99	143	B2	159	141
	VCC	11	3	100	144	C3	160	-
	GND	12	4	1	1	C4	1	-
17.	GCK1 (A16, I/O)	13	5	2	2	B3	2	150
18.	I/O (A17)	14	6	3	3	A1	3	153
19.	I/O	-	-	-	4	A2	4	159
20.	I/O	-	-	-	5	C5	5	162
21.	I/O (TDI)	15	7	4	6	B4	6	165
22.	I/O (TCK)	16	8	5	7	A3	7	171
	GND	-	-	-	8	C6	10	-
23.	I/O	-	-	-	9	B5	11	174
24.	I/O	-	-	-	10	B6	12	177
25.	I/O (TMS)	17	9	6	11	A5	13	180
26.	I/O	18	10	7	12	C7	14	183
27.	I/O	-	-	-	13	B7	15	186
28.	I/O	-	11	8	14	A6	16	189
29.	I/O	19	12	9	15	A7	17	195
30.	I/O	20	13	10	16	A8	18	198
	GND	21	14	11	17	C8	19	-
	VCC	22	15	12	18	B8	20	-
31.	I/O	23	16	13	19	C9	21	201
32.	I/O	24	17	14	20	B9	22	207
33.	I/O	-	18	15	21	A9	23	210
34.	1/0	-	-	-	22	B10	24	213
35.	1/0	25	19	16	23	C10	25	219
36.	I/O	26	20	17	24	A10	26	222
37.	I/O	-	-	-	25	A11	27	225
38.	I/O	-	-	-	26	B11	28	231
	GND	-	-	-	27	C11	29	-
39.	I/O	27	21	18	28	B12	32	234
40.	I/O	-	22	19	29	A13	33	237
41.	I/O	-	-	-	30	A14	34	240
42	1/0	-	-	-	31	C12	35	243
43.	1/O	28	23	20	32	B13	36	246
44.	1/O	29	24	21	33	B14	37	249
45.	M1 (I/O)	30	25	22	34	A15	38	258
	GND	31	26	23	35	C13	39	-
46	M0 (I/O)	32	27	24	36	A16	40	261
10.	VCC	33	28	25	37	C14	41	-
47	M2 (I/Q)	34	29	26	38	B15	42	264
48.	GCK2 (I/O)	35	30	27	39	B16	43	267
49		36	31	28	40	D14	44	276
50	1/O	-	-	-	41	C15	45	279
51		-	-	-	42	D15	46	282
52		-	32	29	43	F14	40	288
53		37	33	30	44	C16	48	200
54	1/0	-	-	-		F15	40	201
55	1/0	_	_	_	_	D16	50	300
	GND	_	_	_	45	F14	51	-
56		_	_	_	46	F15	52	303
00.			1		-0	110	52	000



Pin	Description	PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
57.	I/O	-	-	-	47	E16	53	306
58.	I/O	38	34	31	48	F16	54	312
59.	I/O	39	35	32	49	G14	55	315
60.	I/O	-	36	33	50	G15	56	318
61.	I/O	-	37	34	51	G16	57	324
62.	I/O	40	38	35	52	H16	58	327
63.	I/O (ERR, INIT)	41	39	36	53	H15	59	330
	VCC	42	40	37	54	H14	60	-
	GND	43	41	38	55	J14	61	-
64.	I/O	44	42	39	56	J15	62	336
65.	I/O	45	43	40	57	J16	63	339
66.	I/O	-	44	41	58	K16	64	348
67.	I/O	-	45	42	59	K15	65	351
68.	I/O	46	46	43	60	K14	66	354
69.	I/O	47	47	44	61	L16	67	360
70.	I/O	-	-	-	62	M16	68	363
71.	I/O	-	-	-	63	L15	69	366
	GND	-	-	-	64	L14	70	-
72.	I/O	-	-	-	-	N16	71	372
73.	I/O	-	-	-	-	M15	72	375
74.	I/O	48	48	45	65	P16	73	378
75.	I/O	49	49	46	66	M14	74	384
76.	I/O	-	-	-	67	N15	75	387
77.	I/O	-	-	-	68	P15	76	390
78.	I/O	50	50	47	69	N14	77	396
79.	I/O	51	51	48	70	R16	78	399
	GND	52	52	49	71	P14	79	-
	DONE	53	53	50	72	R15	80	-
	VCC	54	54	51	73	P13	81	-
	PROG	55	55	52	74	R14	82	-
80.	I/O (D7)	56	56	53	75	T16	83	408
81.	GCK3 (I/O)	57	57	54	76	T15	84	411
82.	I/O	-	-	-	77	R13	85	420
83.	I/O	-	-	-	78	P12	86	423
84.	I/O (D6)	58	58	55	79	T14	87	426
85.	I/O	-	59	56	80	T13	88	432
	GND	-	-	-	81	P11	91	-
86.	I/O	-	-	-	82	R11	92	435
87.	I/O	-	-	-	83	T11	93	438
88.	I/O (D5)	59	60	57	84	T10	94	444
89.	I/O (CS0)	60	61	58	85	P10	95	447
90.	I/O	-	62	59	86	R10	96	450
91.	I/O	-	63	60	87	Т9	97	456
92.	I/O (D4)	61	64	61	88	R9	98	459
93.	I/O	62	65	62	89	P9	99	462
	VCC	63	66	63	90	R8	100	-
L	GND	64	67	64	91	P8	101	-
94.	I/O (D3)	65	68	65	92	T8	102	468
95.	I/O (RS)	66	69	66	93	17	103	471
96.	1/0	-	70	67	94	T6	104	474
97.	I/O	-	-	-	95	R7	105	480
98.	I/O (D2)	67	71	68	96	P7	106	483



Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
50.	I/O	24	20	22	24	28	B10	H5	32	330
51.	I/O	-	21	23	25	29	A9	J2	33	333
52.	I/O	-	22	24	26	30	A10	J1	34	339
53.	I/O	-	-	-	27	31	A11	J3	35	342
54.	I/O	-	-	-	28	32	C11	J4	36	345
55.	I/O	-	-	-	-	-	D11	J5	38	351
56.	I/O	-	-	-	-	-	D12	K1	39	354
	VCC	-	-	-	-	-	-	VCC*	40	-
57.	I/O	25	23	25	29	33	B11	K2	41	357
58.	I/O	26	24	26	30	34	A12	K3	42	363
59.	I/O	-	25	27	31	35	B12	J6	43	366
60.	I/O	-	26	28	32	36	A13	L1	44	369
	GND	-	27	29	33	37	C12	GND*	45	-
61.	I/O	-	-	-	-	-	D13	L2	46	375
62.	I/O	-	-	-	-	-	D14	K4	47	378
63.	I/O	-	-	-	-	38	B13	L3	48	381
64.	I/O	-	-	-	-	39	A14	M1	49	387
65.	I/O	-	-	30	34	40	A15	K5	50	390
66.	I/O	-	-	31	35	41	C13	M2	51	393
67.	I/O	27	28	32	36	42	B14	L4	52	399
68.	I/O	-	29	33	37	43	A16	N1	53	402
69.	I/O	-	30	34	38	44	B15	M3	54	405
70.	I/O	-	31	35	39	45	C14	N2	55	411
71.	I/O	28	32	36	40	46	A17	K6	56	414
72.	I/O	29	33	37	41	47	B16	P1	57	417
73.	M1 (I/O)	30	34	38	42	48	C15	N3	58	426
	GND	31	35	39	43	49	D15	GND*	59	-
74.	M0 (I/O)	32	36	40	44	50	A18	P2	60	429
	VCC	33	37	41	45	55	D16	VCC*	61	-
75.	M2 (I/O)	34	38	42	46	56	C16	M4	62	432
76.	GCK2 (I/O)	35	39	43	47	57	B17	R2	63	435
77.	I/O (HDC)	36	40	44	48	58	E16	P3	64	444
78.	I/O	-	41	45	49	59	C17	L5	65	447
79.	I/O	-	42	46	50	60	D17	N4	66	450
80.	I/O	-	43	47	51	61	B18	R3	67	456
81.	I/O (LDC)	37	44	48	52	62	E17	P4	68	459
82.	I/O	-	-	49	53	63	F16	K7	69	462
83.	I/O	-	-	50	54	64	C18	M5	70	468
84.	I/O	-	-	-	-	65	D18	R4	71	471
85.	I/O	-	-	-	-	66	F17	N5	72	474
86.	I/O	-	-	-	-	-	E15	P5	73	480
87.	I/O	-	-	-	-	-	F15	L6	74	483
	GND	-	45	51	55	67	G16	GND*	75	-
88.	I/O	-	46	52	56	68	E18	R5	76	486
89.	I/O	-	47	53	57	69	F18	M6	77	492
90.	I/O	38	48	54	58	70	G17	N6	78	495
91.	I/O	39	49	55	59	71	G18	P6	79	504
	VCC	-	-	-	-	-	-	VCC*	80	-
92.	I/O	-	-	-	60	72	H16	R6	81	507
93.	I/O	-	-	-	61	73	H17	M7	82	510
94.	I/O	-	-	-	-	-	G15	N7	84	516

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
137.	I/O	-	-	-	-	-	R11	K12	137	708
138.	I/O	-	82	92	100	120	U13	K13	138	711
139.	I/O	-	83	93	101	121	V13	K14	139	714
	VCC	-	-	-	-	-	-	VCC*	140	-
140.	I/O (D5)	59	84	94	102	122	U12	K15	141	720
141.	I/O ( <u>CS0</u> )	60	85	95	103	123	V12	J12	142	723
142.	I/O	-	-	-	104	124	T11	J13	144	726
143.	I/O	-	-	-	105	125	U11	J14	145	732
144.	I/O	-	86	96	106	126	V11	J15	146	735
145.	I/O	-	87	97	107	127	V10	J11	147	738
146.	I/O (D4)	61	88	98	108	128	U10	H13	148	744
147.	I/O	62	89	99	109	129	T10	H14	149	747
	VCC	63	90	100	110	130	R10	VCC*	150	-
	GND	64	91	101	111	131	R9	GND*	151	-
148.	I/O (D3)	65	92	102	112	132	Т9	H12	152	756
149.	I/O (RS)	66	93	103	113	133	U9	H11	153	759
150.	1/O	-	94	104	114	134	V9	G14	154	768
151	1/0	-	95	105	115	135	V8	G15	155	771
152	1/0	_	-	-	116	136	U8	G13	156	780
153	1/0	-	-	-	117	137	T8	G12	157	783
154	1/Q (D2)	67	96	106	118	138	. 10 V7	G11	159	786
155	1/0	68	07	100	110	130	117	E15	160	700
155.		00	51	107	115	155	07	113 VCC*	161	192
156		-	-	109	- 120	140	-	F14	162	-
150.	1/0	-	90	100	120	140	116	E12	102	795
157.	1/0	-	99	109	121	141	D0	C10	164	790 804
150.	1/0	-	-	-	-	-		G10 E15	104	807
159.		-	-	-	-	-			100	007
100	GND	-	100	110	122	142			100	-
100.	1/0	-	-	-	-	-		E14	107	810
101.	1/0	-	-	-	-	-	KO VE	F12	100	810
162.	1/0	-	-	-	-	143	V5	E13	169	819
163.	1/0	-	-	-	-	144	V4	D15	170	822
164.	1/0	-	-	111	123	145	U5 To	F11	1/1	828
165.	1/0	-	-	112	124	146	16	D14	172	831
166.	1/O (D1)	69	101	113	125	147	V3	E12	1/3	834
167.	I/O (RCLK-BUSY/RDY)	70	102	114	126	148	V2	C15	1/4	840
168.	1/0	-	103	115	127	149	04	D13	175	843
169.	1/0	-	104	116	128	150	T5	C14	176	846
170.	I/O (D0, DIN)	71	105	117	129	151	U3	F10	177	855
171.	I/O (DOUT)	72	106	118	130	152	T4	B15	178	858
	CCLK	73	107	119	131	153	V1	C13	179	-
	VCC	74	108	120	132	154	R4	VCC*	180	-
172.	I/O (TDO)	75	109	121	133	159	U2	A15	181	-
	GND	76	110	122	134	160	R3	GND*	182	-
173.	I/O (A0, WS)	77	111	123	135	161	Т3	A14	183	9
174.	GCK4 (A1, I/O)	78	112	124	136	162	U1	B13	184	15
175.	I/O	-	113	125	137	163	P3	E11	185	18
176.	I/O	-	114	126	138	164	R2	C12	186	21
177.	I/O (CS1, A2)	79	115	127	139	165	T2	A13	187	27
178.	I/O (A3)	80	116	128	140	166	N3	B12	188	30
179.	I/O		-	-	-	-	P4	F9	189	33

5	XII	<b>INX</b> ®
<b>~</b>		

Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
190.	I/O	-	-	-	X8	-	M4	951
191.	I/O	-	-	-	V9	-	L1	954
192.	I/O (D2)	106	138	159	W8	G11	J1	960
193.	I/O	107	139	160	X7	F15	K3	963
	VCC	-	-	161	X5	VCC*	VCC*	
194.	I/O	108	140	162	V8	F14	J2	966
195.	I/O	109	141	163	W7	F13	J3	972
196.	I/O	-	-	164	U8	G10	K4	975
197.	I/O	-	-	165	W6	E15	G1	978
	GND	110	142	166	X6	GND*	GND*	
198.	I/O	-	-	-	T8	-	H2	984
199.	I/O	-	-	-	V7	-	H3	987
200.	I/O	-	-	167	X4	E14	J4	990
201.	I/O	-	-	168	U7	F12	F1	996
202.	I/O	-	143	169	W5	E13	G2	999
203.	I/O	-	144	170	V6	D15	G3	1002
204.	I/O	111	145	171	T7	F11	F2	1008
205.	I/O	112	146	172	Х3	D14	E2	1011
206.	I/O (D1)	113	147	173	U6	E12	F3	1014
207.	I/O (RCLK-BUSY/RDY)	114	148	174	V5	C15	G4	1020
208.	I/O	-	-	-	W4	-	D2	1023
209.	I/O	-	-	-	W3	-	F4	1032
210.	I/O	115	149	175	T6	D13	E3	1035
211.	I/O	116	150	176	U5	C14	C2	1038
212.	I/O (D0, DIN)	117	151	177	V4	F10	D3	1044
213.	I/O (DOUT)	118	152	178	X1	B15	E4	1047
	CCLK	119	153	179	V3	C13	C3	-
	VCC	120	154	180	W1	VCC*	VCC*	-
214.	I/O (TDO)	121	159	181	U4	A15	D4	0
	GND	122	160	182	X2	GND*	GND*	-
215.	I/O (A0, WS)	123	161	183	W2	A14	B3	9
216.	GCK4 (A1, I/O)	124	162	184	V2	B13	C4	15
217.	I/O	125	163	185	R5	E11	D5	18
218.	I/O	126	164	186	T4	C12	A3	21
219.	I/O (A2, CS1)	127	165	187	U3	A13	D6	27
220.	I/O (A3)	128	166	188	V1	B12	C6	30
221.	I/O	-	-	-	R4	-	B5	33
222.	I/O	-	-	-	P5	-	A4	39
223.	I/O	-	-	189	U2	F9	C7	42
224.	I/O	-	-	190	T3	D11	B6	45
225.	I/O	129	167	191	U1	A12	A6	51
226.	I/O	130	168	192	P4	C11	D8	54
227.	I/O	-	169	193	R3	B11	B7	57
228.	I/O	-	170	194	N5	E10	A7	63
229.	I/O	-	-	195	T2	-	D9	66
230.	I/O	-	-	-	R2	-	C9	69
	GND	131	171	196	T1	GND*	GND*	-
231.	I/O	132	172	197	N4	A11	B8	75
232.	I/O	133	173	198	P3	D10	D10	78
233.	I/O	-	-	199	P2	C10	C10	81
234.	I/O	-	-	200	N3	B10	B9	87
	VCC	-	-	201	R1	VCC*	VCC*	-

### **XC5200 Series Field Programmable Gate Arrays**

## **∑**XILINX<sup>®</sup>

### **Product Availability**

	PINS	64	84	100	100	144	156	160	176	191	208	208	223	225	240	240	299	352
	TYPE	Plast. VQFP	Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	Ceram. PGA	Plast. PQFP	Plast. TQFP	Ceram. PGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	Plast. BGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	Plast. BGA
	CODE	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	PQ160	т0176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	BG352
	-6	CI	CI	CI	CI	CI	CI											
XC5202	-5	CI	CI	CI	CI	CI	CI											
700202	-4	С	С	С	С	С	С											
	-3	С	С	С	С	С	С											
XC5204	-6		CI	CI	CI	CI	CI	CI										
	-5		CI	CI	CI	CI	CI	CI										
700204	-4		С	С	С	С	С	С										
	-3		С	С	С	С	С	С										
	-6		CI	CI	CI	CI		CI	CI	CI		CI						
XC5206	-5		CI	CI	CI	CI		CI	CI	CI		CI						
700200	-4		С	С	С	С		С	С	С		С						
	-3		С	С	С	С		С	С	С		С						
	-6		CI			CI		CI	CI			CI	CI	CI		CI		
XC5210	-5		CI			CI		CI	CI			CI	CI	CI		CI		
	-4		С			С		С	С			С	С	С		С		
	-3		С			С		С	С			С	С	С		С		
	-6							CI			CI			CI	CI		CI	CI
XC5215	-5							С			С			С	С		С	С
7.00210	-4							С			С			С	С		С	С
	-3							С			С			С	С		С	С

C = Commercial  $T_J = 0^{\circ}$  to +85°C

I= Industrial  $T_J = -40^{\circ}C$  to  $+100^{\circ}C$ 

\* VQ64 package supports Master Serial, Slave Serial, and Express configuration modes only.

## **User I/O Per Package**

_	Мах	Package Type																
Device	I/O	VQ64	PC84	PQ100	VQ100	TQ144	PG156	PQ160	TQ176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	BG352
XC5202	84	52	65	81	81	84	84											
XC5204	124		65	81	81	117	124	124										
XC5206	148		65	81	81	117		133	148	148		148						
XC5210	196		65			117		133	149			164	196	196		196		
XC5215	244							133			164			196	197		244	244

7/8/98

## **Ordering Information**





## Revisions

Version	Description
12/97	Rev 5.0 added -3, -4 specification
7/98	Rev 5.1 added Spartan family to comparison, removed HQ304
11/98	Rev 5.2 All specifications made final.