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### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### **Details**

Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	784
Total RAM Bits	-
Number of I/O	81
Number of Gates	10000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-BQFP
Supplier Device Package	100-PQFP (20x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc5206-6pq100c">https://www.e-xfl.com/product-detail/xilinx/xc5206-6pq100c</a>

*XC3000 family:* XC5200 devices support an additional programming mode: Peripheral Synchronous.

*XC3000 family:* The XC5200 family does not support Power-down, but offers a Global 3-state input that does not reset any flip-flops.

*XC3000 family:* The XC5200 family does not provide an on-chip crystal oscillator amplifier, but it does provide an internal oscillator from which a variety of frequencies up to 12 MHz are available.

### Architectural Overview

Figure 1 presents a simplified, conceptual overview of the XC5200 architecture. Similar to conventional FPGAs, the XC5200 family consists of programmable IOBs, programmable logic blocks, and programmable interconnect. Unlike other FPGAs, however, the logic and local routing resources of the XC5200 family are combined in flexible VersaBlocks (Figure 2). General-purpose routing connects to the VersaBlock through the General Routing Matrix (GRM).

### VersaBlock: Abundant Local Routing Plus Versatile Logic

The basic logic element in each VersaBlock structure is the Logic Cell, shown in Figure 3. Each LC contains a 4-input function generator (F), a storage device (FD), and control logic. There are five independent inputs and three outputs to each LC. The independence of the inputs and outputs allows the software to maximize the resource utilization within each LC. Each Logic Cell also contains a direct feedthrough path that does not sacrifice the use of either the function generator or the register; this feature is a first for FPGAs. The storage device is configurable as either a D flip-flop or a latch. The control logic consists of carry logic for fast implementation of arithmetic functions, which can also be configured as a cascade chain allowing decode of very wide input functions.

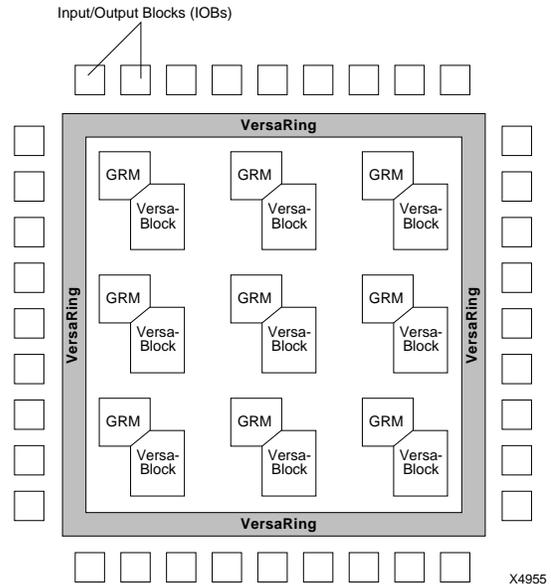


Figure 1: XC5200 Architectural Overview

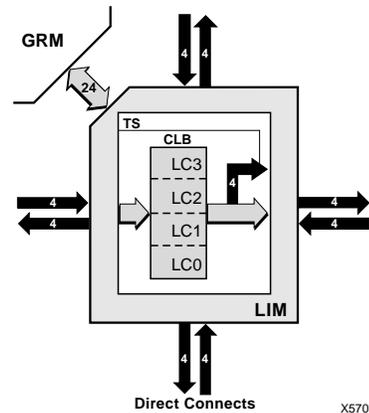


Figure 2: VersaBlock

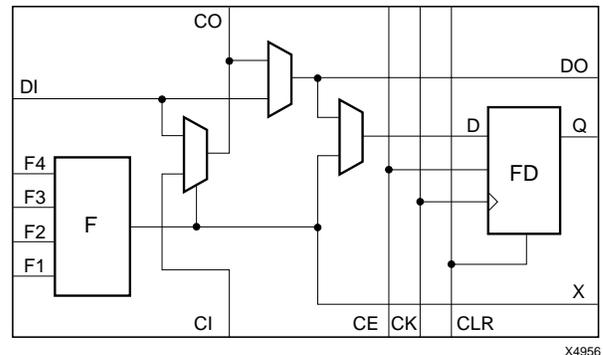
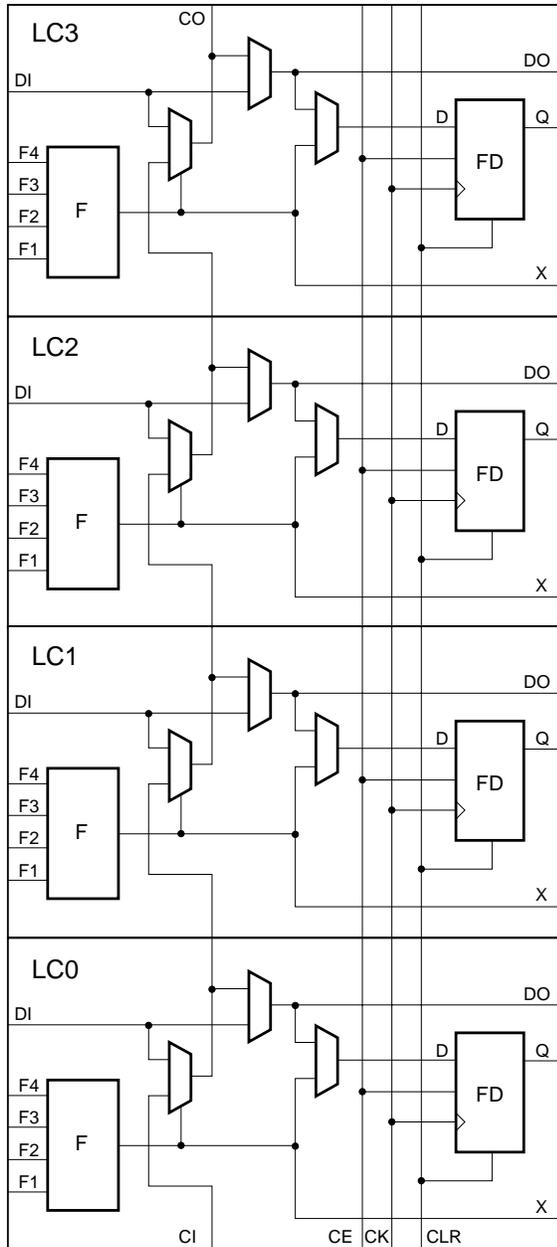


Figure 3: XC5200 Logic Cell (Four LCs per CLB)

The XC5200 CLB consists of four LCs, as shown in Figure 4. Each CLB has 20 independent inputs and 12 independent outputs. The top and bottom pairs of LCs can be configured to implement 5-input functions. The challenge of FPGA implementation software has always been to maximize the usage of logic resources. The XC5200 family addresses this issue by surrounding each CLB with two types of local interconnect — the Local Interconnect Matrix (LIM) and direct connects. These two interconnect resources, combined with the CLB, form the VersaBlock, represented in Figure 2.



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Figure 4: Configurable Logic Block

The LIM provides 100% connectivity of the inputs and outputs of each LC in a given CLB. The benefit of the LIM is that no general routing resources are required to connect feedback paths within a CLB. The LIM connects to the GRM via 24 bidirectional nodes.

The direct connects allow immediate connections to neighboring CLBs, once again without using any of the general interconnect. These two layers of local routing resource improve the granularity of the architecture, effectively making the XC5200 family a “sea of logic cells.” Each Versa-Block has four 3-state buffers that share a common enable line and directly drive horizontal and vertical Longlines, creating robust on-chip bussing capability. The VersaBlock allows fast, local implementation of logic functions, effectively implementing user designs in a hierarchical fashion. These resources also minimize local routing congestion and improve the efficiency of the general interconnect, which is used for connecting larger groups of logic. It is this combination of both fine-grain and coarse-grain architecture attributes that maximize logic utilization in the XC5200 family. This symmetrical structure takes full advantage of the third metal layer, freeing the placement software to pack user logic optimally with minimal routing restrictions.

### VersaRing I/O Interface

The interface between the IOBs and core logic has been redesigned in the XC5200 family. The IOBs are completely decoupled from the core logic. The XC5200 IOBs contain dedicated boundary-scan logic for added board-level testability, but do not include input or output registers. This approach allows a maximum number of IOBs to be placed around the device, improving the I/O-to-gate ratio and decreasing the cost per I/O. A “freeway” of interconnect cells surrounding the device forms the VersaRing, which provides connections from the IOBs to the internal logic. These incremental routing resources provide abundant connections from each IOB to the nearest VersaBlock, in addition to Longline connections surrounding the device. The VersaRing eliminates the historic trade-off between high logic utilization and pin placement flexibility. These incremental edge resources give users increased flexibility in preassigning (i.e., locking) I/O pins before completing their logic designs. This ability accelerates time-to-market, since PCBs and other system components can be manufactured concurrent with the logic design.

### General Routing Matrix

The GRM is functionally similar to the switch matrices found in other architectures, but it is novel in its tight coupling to the logic resources contained in the VersaBlocks. Advanced simulation tools were used during the development of the XC5200 architecture to determine the optimal level of routing resources required. The XC5200 family contains six levels of interconnect hierarchy — a series of

single-length lines, double-length lines, and Longlines all routed through the GRM. The direct connects, LIM, and logic-cell feedthrough are contained within each Versa-Block. Throughout the XC5200 interconnect, an efficient multiplexing scheme, in combination with three layer metal (TLM), was used to improve the overall efficiency of silicon usage.

### Performance Overview

The XC5200 family has been benchmarked with many designs running synchronous clock rates beyond 66 MHz. The performance of any design depends on the circuit to be implemented, and the delay through the combinatorial and sequential logic elements, plus the delay in the interconnect routing. A rough estimate of timing can be made by assuming 3-6 ns per logic level, which includes direct-connect routing delays, depending on speed grade. More accurate estimations can be made using the information in the Switching Characteristic Guideline section.

### Taking Advantage of Reconfiguration

FPGA devices can be reconfigured to change logic function while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be reconfigured dynamically to perform different functions at different times.

Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement multi-purpose hardware for a given application. As an added benefit, using reconfigurable FPGA devices simplifies hardware design and debugging and shortens product time-to-market.

## Detailed Functional Description

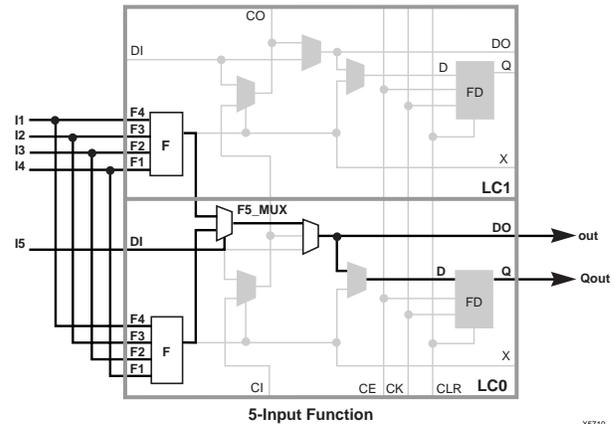
### Configurable Logic Blocks (CLBs)

Figure 4 shows the logic in the XC5200 CLB, which consists of four Logic Cells (LC[3:0]). Each Logic Cell consists of an independent 4-input Lookup Table (LUT), and a D-Type flip-flop or latch with common clock, clock enable, and clear, but individually selectable clock polarity. Additional logic features provided in the CLB are:

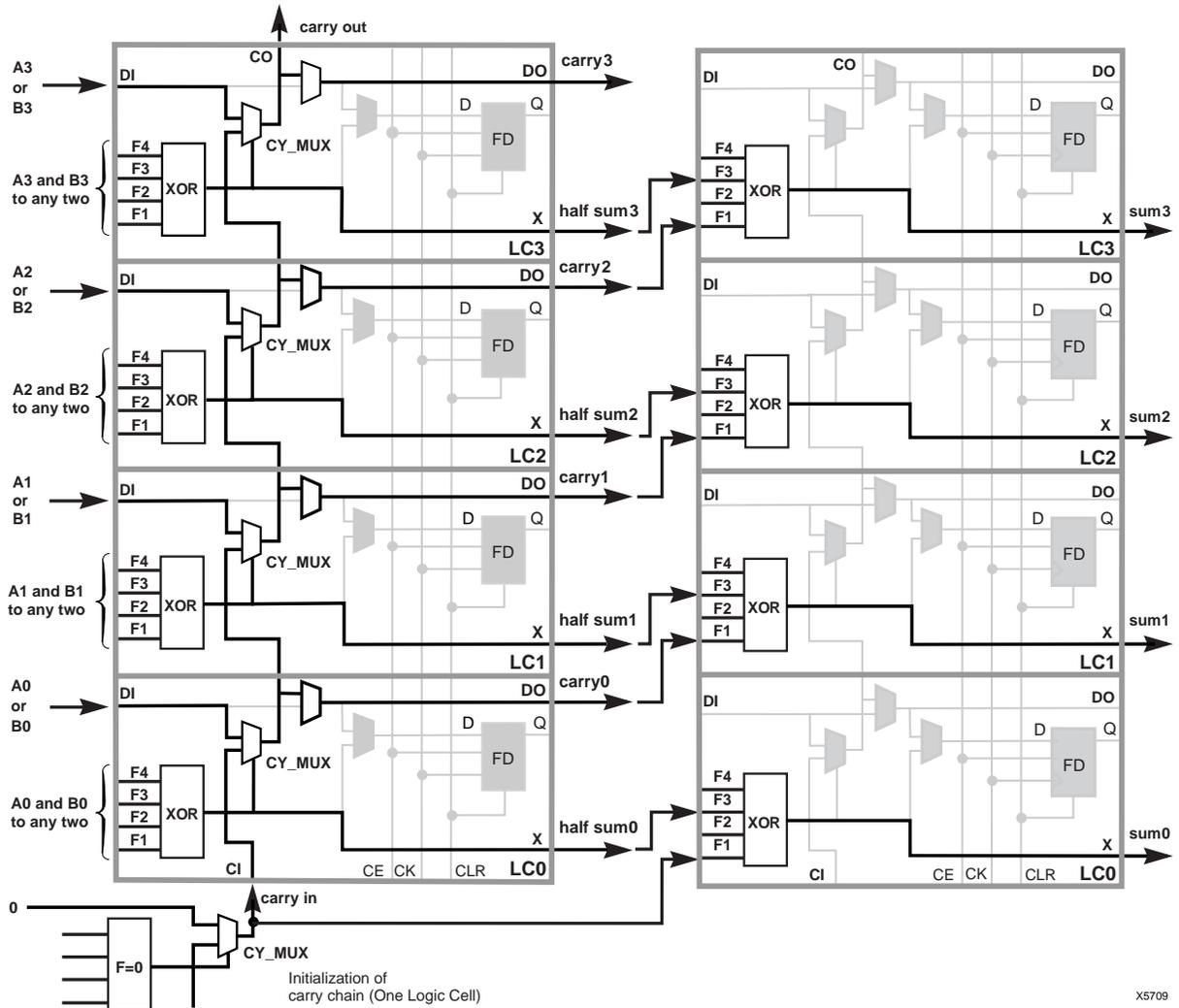
- An independent 5-input LUT by combining two 4-input LUTs.
- High-speed carry propagate logic.
- High-speed pattern decoding.
- High-speed direct connection to flip-flop D-inputs.
- Individual selection of either a transparent, level-sensitive latch or a D flip-flop.
- Four 3-state buffers with a shared Output Enable.

### 5-Input Functions

Figure 5 illustrates how the outputs from the LUTs from LC0 and LC1 can be combined with a 2:1 multiplexer (F5\_MUX) to provide a 5-input function. The outputs from the LUTs of LC2 and LC3 can be similarly combined.



**Figure 5: Two LUTs in Parallel Combined to Create a 5-input Function**



**Figure 6: XC5200 CY\_MUX Used for Adder Carry Propagate**

### Carry Function

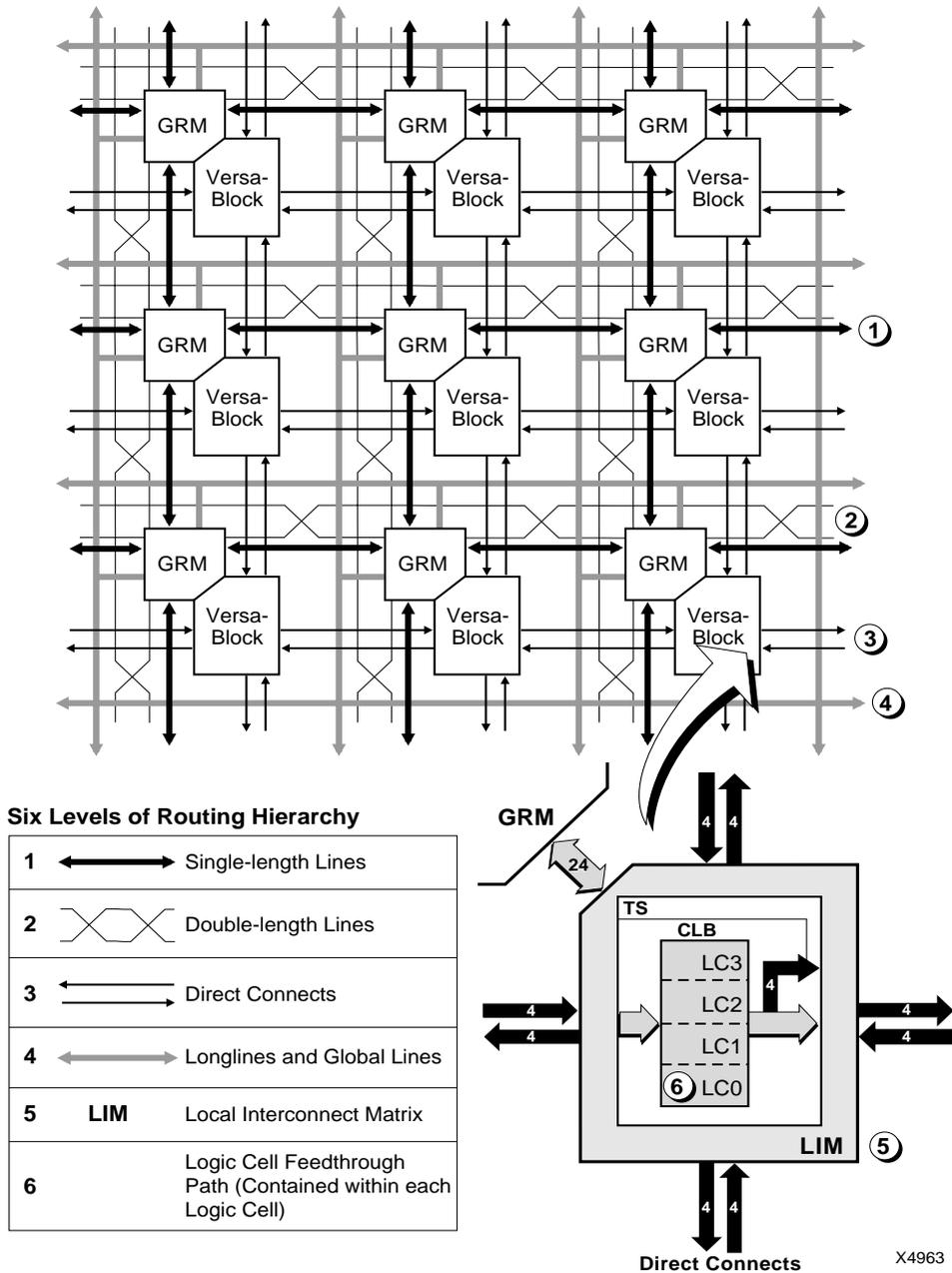
The XC5200 family supports a carry-logic feature that enhances the performance of arithmetic functions such as counters, adders, etc. A carry multiplexer (CY\_MUX) symbol is used to indicate the XC5200 carry logic. This symbol represents the dedicated 2:1 multiplexer in each LC that performs the one-bit high-speed carry propagate per logic cell (four bits per CLB).

While the carry propagate is performed inside the LC, an adjacent LC must be used to complete the arithmetic function. Figure 6 represents an example of an adder function. The carry propagate is performed on the CLB shown,

which also generates the half-sum for the four-bit adder. An adjacent CLB is responsible for XORing the half-sum with the corresponding carry-out. Thus an adder or counter requires two LCs per bit. Notice that the carry chain requires an initialization stage, which the XC5200 family accomplishes using the carry initialize (CY\_INIT) macro and one additional LC. The carry chain can propagate vertically up a column of CLBs.

The XC5200 library contains a set of Relationally-Placed Macros (RPMs) and arithmetic functions designed to take advantage of the dedicated carry logic. Using and modifying these macros makes it much easier to implement cus-

Matrix through a hierarchy of different-length metal segments in both the horizontal and vertical directions. A pro-



**Figure 15: XC5200 Interconnect Structure**

programmable interconnect point (PIP) establishes an electrical connection between two wire segments. The PIP, consisting of a pass transistor switch controlled by a memory element, provides bidirectional (in some cases, unidirectional) connection between two adjoining wires. A collection of PIPs inside the General Routing Matrix and in the Local Interconnect Matrix provides connectivity between various types of metal segments. A hierarchy of PIPs and

associated routing segments combine to provide a powerful interconnect hierarchy:

- Forty bidirectional single-length segments per CLB provide ten routing channels to each of the four neighboring CLBs in four directions.
- Sixteen bidirectional double-length segments per CLB provide four routing channels to each of four other (non-neighboring) CLBs in four directions.
- Eight horizontal and eight vertical bidirectional Longline

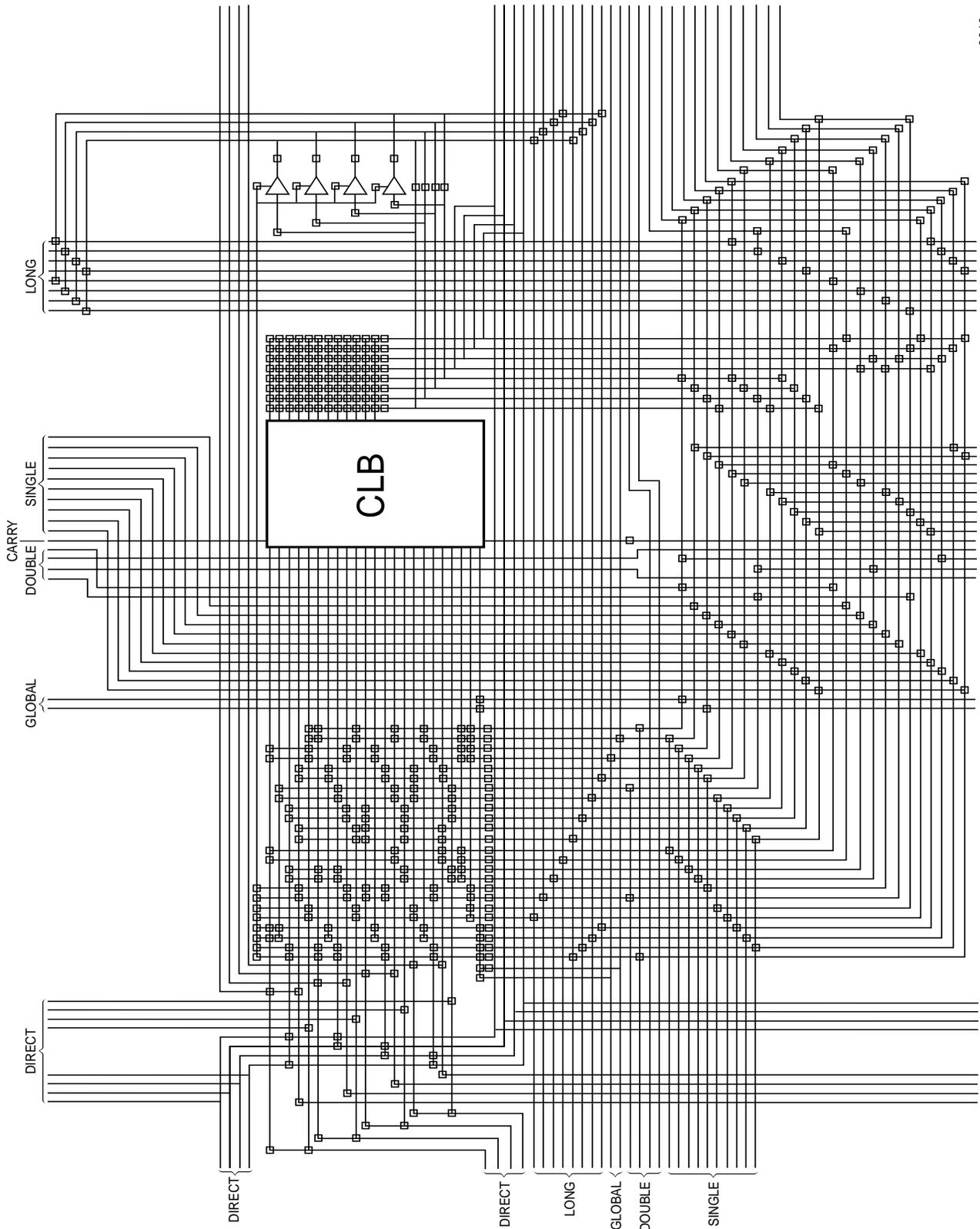


Figure 17: Detail of Programmable Interconnect Associated with XC5200 Series CLB

Master Serial mode generates CCLK and receives the configuration data in serial form from a Xilinx serial-configuration PROM.

CCLK speed is selectable as 1 MHz (default), 6 MHz, or 12 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +50%.

### Peripheral Modes

The two Peripheral modes accept byte-wide data from a bus. A RDY/BUSY status is available as a handshake signal. In Asynchronous Peripheral mode, the internal oscillator generates a CCLK burst signal that serializes the byte-wide data. CCLK can also drive slave devices. In the synchronous mode, an externally supplied clock input to CCLK serializes the data.

### Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

### Serial Daisy Chain

Multiple devices with different configurations can be connected together in a “daisy chain,” and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in [Figure 28 on page 114](#). Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received. [Figure 25 on page 109](#) shows the start-up timing for an XC5200-Series device.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM file formatter must be used to combine the bitstreams for a daisy-chained configuration.

### Multi-Family Daisy Chain

All Xilinx FPGAs of the XC2000, XC3000, XC4000, and XC5200 Series use a compatible bitstream format and can, therefore, be connected in a daisy chain in an arbitrary sequence. There is, however, one limitation. If the chain contains XC5200-Series devices, the master normally cannot be an XC2000 or XC3000 device.

The reason for this rule is shown in [Figure 25 on page 109](#). Since all devices in the chain store the same length count value and generate or receive one common sequence of CCLK pulses, they all recognize length-count match on the same CCLK edge, as indicated on the left edge of [Figure 25](#). The master device then generates additional CCLK pulses until it reaches its finish point F. The different families generate or require different numbers of additional CCLK pulses until they reach F. Not reaching F means that the device does not really finish its configuration, although DONE may have gone High, the outputs became active, and the internal reset was released. For the XC5200-Series device, not reaching F means that read-back cannot be initiated and most boundary scan instructions cannot be used.

The user has some control over the relative timing of these events and can, therefore, make sure that they occur at the proper time and the finish point F is reached. Timing is controlled using options in the bitstream generation software.

XC5200 devices always have the same number of CCLKs in the power up delay, independent of the configuration mode, unlike the XC3000/XC4000 Series devices. To guarantee all devices in a daisy chain have finished the power-up delay, tie the INIT pins together, as shown in [Figure 27](#).

### XC3000 Master with an XC5200-Series Slave

Some designers want to use an XC3000 lead device in peripheral mode and have the I/O pins of the XC5200-Series devices all available for user I/O. [Figure 22](#) provides a solution for that case.

This solution requires one CLB, one IOB and pin, and an internal oscillator with a frequency of up to 5 MHz as a clock source. The XC3000 master device must be configured with late Internal Reset, which is the default option.

One CLB and one IOB in the lead XC3000-family device are used to generate the additional CCLK pulse required by the XC5200-Series devices. When the lead device removes the internal RESET signal, the 2-bit shift register responds to its clock input and generates an active Low output signal for the duration of the subsequent clock period. An external connection between this output and CCLK thus creates the extra CCLK pulse.



### Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/ $\overline{\text{BUSY}}$  output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal

for test purposes. Note that  $\overline{\text{RDY/BUSY}}$  is pulled High with a high-impedance pullup prior to INIT going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

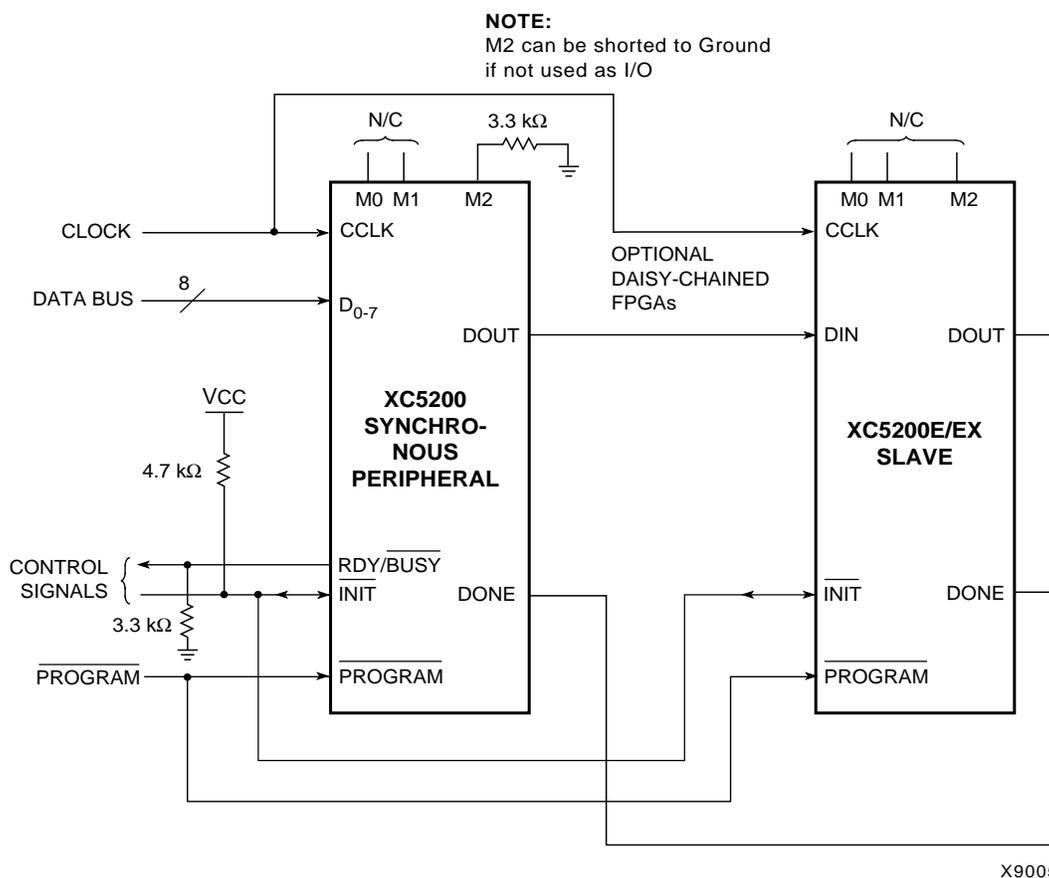
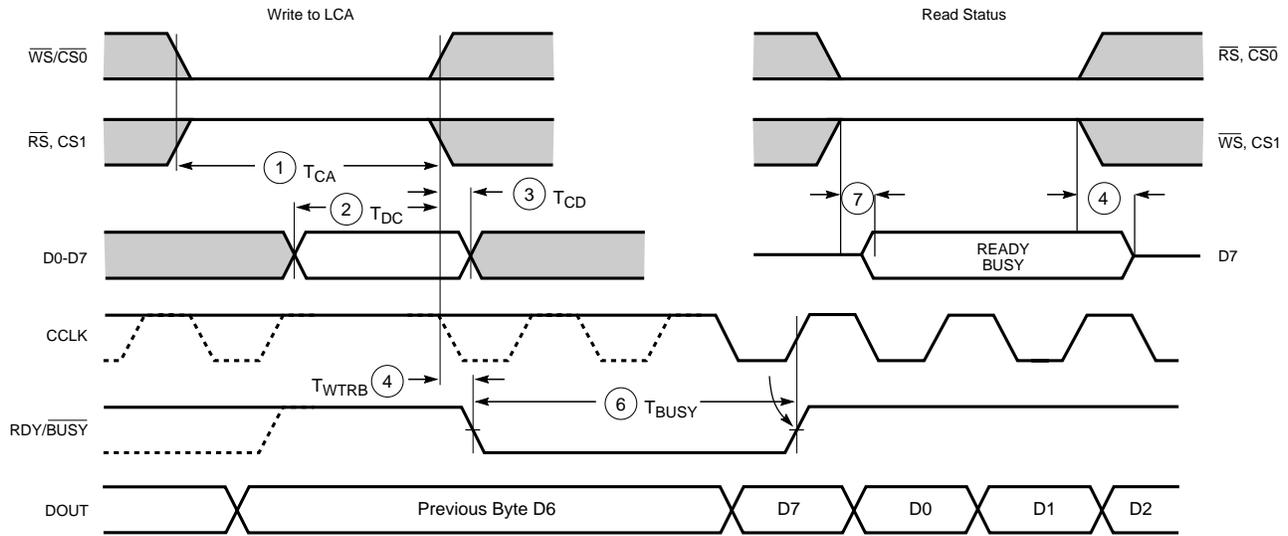


Figure 33: Synchronous Peripheral Mode Circuit Diagram



X6097

	Description	Symbol	Min	Max	Units
Write	Effective Write time (CS0, WS=Low; RS, CS1=High)	1 $T_{CA}$	100		ns
	DIN setup time	2 $T_{DC}$	60		ns
	DIN hold time	3 $T_{CD}$	0		ns
RDY	RDY/BUSY delay after end of Write or Read	4 $T_{WTRB}$		60	ns
	RDY/BUSY active after beginning of Read	7		60	ns
	RDY/BUSY Low output (Note 4)	6 $T_{BUSY}$	2	9	CCLK periods

- Notes:
1. Configuration must be delayed until  $\overline{INIT}$  pins of all daisy-chained FPGAs are high.
  2. The time from the end of  $\overline{WS}$  to CCLK cycle for the new byte of data depends on the completion of previous byte processing and the phase of internal timing generator for CCLK.
  3. CCLK and DOUT timing is tested in slave mode.
  4.  $T_{BUSY}$  indicates that the double-buffered parallel-to-serial converter is not yet ready to receive new data. The shortest  $T_{BUSY}$  occurs when a byte is loaded into an empty parallel-to-serial converter. The longest  $T_{BUSY}$  occurs when a new word is loaded into the input register before the second-level buffer has started shifting out data.

This timing diagram shows very relaxed requirements. Data need not be held beyond the rising edge of  $\overline{WS}$ . RDY/BUSY will go active within 60 ns after the end of  $\overline{WS}$ . A new write may be asserted immediately after RDY/BUSY goes Low, but write may not be terminated until RDY/BUSY has been High for one CCLK period.

Figure 36: Asynchronous Peripheral Mode Programming Switching Characteristics

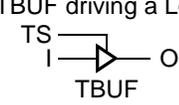
### XC5200 Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

			Speed Grade			
Description	Symbol	Device	-6 Max (ns)	-5 Max (ns)	-4 Max (ns)	-3 Max (ns)
<b>Global Signal Distribution</b> From pad through global buffer, to any clock (CK)	$T_{\text{BUFG}}$	XC5202	9.1	8.5	8.0	6.9
		XC5204	9.3	8.7	8.2	7.6
		XC5206	9.4	8.8	8.3	7.7
		XC5210	9.4	8.8	8.5	7.7
		XC5215	10.5	9.9	9.8	9.6

### XC5200 Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

			Speed Grade			
Description	Symbol	Device	-6 Max (ns)	-5 Max (ns)	-4 Max (ns)	-3 Max (ns)
TBUF driving a Longline  I to Longline, while TS is Low; i.e., buffer is constantly active	$T_{\text{IO}}$	XC5202	6.0	3.8	3.0	2.0
		XC5204	6.4	4.1	3.2	2.3
		XC5206	6.6	4.2	3.3	2.7
		XC5210	6.6	4.2	3.3	2.9
		XC5215	7.3	4.6	3.8	3.2
TS going Low to Longline going from floating High or Low to active Low or High	$T_{\text{ON}}$	XC5202	7.8	5.6	4.7	4.0
		XC5204	8.3	5.9	4.9	4.3
		XC5206	8.4	6.0	5.0	4.4
		XC5210	8.4	6.0	5.0	4.4
		XC5215	8.9	6.3	5.3	4.5
TS going High to TBUF going inactive, not driving Longline	$T_{\text{OFF}}$	XC52xx	3.0	2.8	2.6	2.4

**Note:** 1. Die-size-dependent parameters are based upon XC5215 characterization. Production specifications will vary with array size.

# Product Obsolete or Under Obsolescence



### XC5200 CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Speed Grade		-6		-5		-4		-3	
Description	Symbol	Min (ns)	Max (ns)						
<b>Combinatorial Delays</b>									
F inputs to X output	$T_{ILO}$		5.6		4.6		3.8		3.0
F inputs via transparent latch to Q	$T_{ITO}$		8.0		6.6		5.4		4.3
DI inputs to DO output (Logic-Cell Feedthrough)	$T_{IDO}$		4.3		3.5		2.8		2.4
F inputs via F5_MUX to DO output	$T_{IMO}$		7.2		5.8		5.0		4.3
<b>Carry Delays</b>									
Incremental delay per bit	$T_{CY}$		0.7		0.6		0.5		0.5
Carry-in overhead from DI	$T_{CYDI}$		1.8		1.6		1.5		1.4
Carry-in overhead from F	$T_{CYL}$		3.7		3.2		2.9		2.4
Carry-out overhead to DO	$T_{CYO}$		4.0		3.2		2.5		2.1
<b>Sequential Delays</b>									
Clock (CK) to out (Q) (Flip-Flop)	$T_{CKO}$		5.8		4.9		4.0		4.0
Gate (Latch enable) going active to out (Q)	$T_{GO}$		9.2		7.4		5.9		5.5
<b>Set-up Time Before Clock (CK)</b>									
F inputs	$T_{ICK}$	2.3		1.8		1.4		1.3	
F inputs via F5_MUX	$T_{MICK}$	3.8		3.0		2.5		2.4	
DI input	$T_{DICK}$	0.8		0.5		0.4		0.4	
CE input	$T_{EICK}$	1.6		1.2		0.9		0.9	
<b>Hold Times After Clock (CK)</b>									
F inputs	$T_{CKI}$	0		0		0		0	
F inputs via F5_MUX	$T_{CKMI}$	0		0		0		0	
DI input	$T_{CKDI}$	0		0		0		0	
CE input	$T_{CKEI}$	0		0		0		0	
<b>Clock Widths</b>									
Clock High Time	$T_{CH}$	6.0		6.0		6.0		6.0	
Clock Low Time	$T_{CL}$	6.0		6.0		6.0		6.0	
Toggle Frequency (MHz) (Note 3)	$F_{TOG}$		83		83		83		83
<b>Reset Delays</b>									
Width (High)	$T_{CLR\ W}$	6.0		6.0		6.0		6.0	
Delay from CLR to Q (Flip-Flop)	$T_{CLR}$		7.7		6.3		5.1		4.0
Delay from CLR to Q (Latch)	$T_{CLR\ L}$		6.5		5.2		4.2		3.0
<b>Global Reset Delays</b>									
Width (High)	$T_{GCLR\ W}$	6.0		6.0		6.0		6.0	
Delay from internal GR to Q	$T_{GCLR}$		14.7		12.1		9.1		8.0

- Note:**
1. The CLB K to Q output delay ( $T_{CKO}$ ) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold-time requirement ( $T_{CKDI}$ ) of any CLB on the same die.
  2. Timing is based upon the XC5215 device. For other devices, see Timing Calculator.
  3. Maximum flip-flop toggle rate for export control purposes.

# Product Obsolete or Under Obsolescence

## XC5200 Series Field Programmable Gate Arrays



### XC5200 Boundary Scan (JTAG) Switching Characteristic Guidelines

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC5200 devices unless otherwise noted.

Speed Grade		-6		-5		-4		-3	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max
<b>Setup and Hold</b>									
Input (TDI) to clock (TCK) setup time	$T_{TDITCK}$	30.0		30.0		30.0		30.0	
Input (TDI) to clock (TCK) hold time	$T_{TCKTDI}$	0		0		0		0	
Input (TMS) to clock (TCK) setup time	$T_{TMSTCK}$	15.0		15.0		15.0		15.0	
Input (TMS) to clock (TCK) hold time	$T_{TCKTMS}$	0		0		0		0	
<b>Propagation Delay</b>									
Clock (TCK) to Pad (TDO)	$T_{TCKPO}$		30.0		30.0		30.0		30.0
<b>Clock</b>									
Clock (TCK) High	$T_{TCKH}$	30.0		30.0		30.0		30.0	
Clock (TCK) Low	$T_{TCKL}$	30.0		30.0		30.0		30.0	
$F_{MAX}$ (MHz)	$F_{MAX}$		10.0		10.0		10.0		10.0

Note 1: Input pad setup and hold times are specified with respect to the internal clock.

# Product Obsolete or Under Obsolescence

## XC5200 Series Field Programmable Gate Arrays



Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
35.	I/O (HDC)	19	36	31	28	40	D14	204
36.	I/O	-	-	32	29	43	E14	207
37.	I/O (LDC)	20	37	33	30	44	C16	210
	GND	-	-	-	-	45	F14	-
38.	I/O	-	38	34	31	48	F16	216
39.	I/O	21	39	35	32	49	G14	219
40.	I/O	-	-	36	33	50	G15	222
41.	I/O	-	-	37	34	51	G16	228
42.	I/O	22	40	38	35	52	H16	231
43.	I/O (ERR, INIT)	23	41	39	36	53	H15	234
	VCC	24	42	40	37	54	H14	-
	GND	25	43	41	38	55	J14	-
44.	I/O	26	44	42	39	56	J15	240
45.	I/O	27	45	43	40	57	J16	243
46.	I/O	-	-	44	41	58	K16	246
47.	I/O	-	-	45	42	59	K15	252
48.	I/O	28	46	46	43	60	K14	255
49.	I/O	29	47	47	44	61	L16	258
	GND	-	-	-	-	64	L14	-
50.	I/O	-	48	48	45	65	P16	264
51.	I/O	30	49	49	46	66	M14	267
52.	I/O	-	50	50	47	69	N14	276
53.	I/O	31	51	51	48	70	R16	279
	GND	-	52	52	49	71	P14	-
	DONE	32	53	53	50	72	R15	-
	VCC	33	54	54	51	73	P13	-
	PROG	34	55	55	52	74	R14	-
54.	I/O (D7)	35	56	56	53	75	T16	288
55.	GCK3 (I/O)	36	57	57	54	76	T15	291
56.	I/O (D6)	37	58	58	55	79	T14	300
57.	I/O	-	-	59	56	80	T13	303
	GND	-	-	-	-	81	P11	-
58.	I/O (D5)	38	59	60	57	84	T10	306
59.	I/O (CS0)	-	60	61	58	85	P10	312
60.	I/O	-	-	62	59	86	R10	315
61.	I/O	-	-	63	60	87	T9	318
62.	I/O (D4)	39	61	64	61	88	R9	324
63.	I/O	-	62	65	62	89	P9	327
	VCC	40	63	66	63	90	R8	-
	GND	41	64	67	64	91	P8	-
64.	I/O (D3)	42	65	68	65	92	T8	336
65.	I/O (RS)	43	66	69	66	93	T7	339
66.	I/O	-	-	70	67	94	T6	342
67.	I/O	-	-	-	-	95	R7	348
68.	I/O (D2)	44	67	71	68	96	P7	351
69.	I/O	-	68	72	69	97	T5	360
	GND	-	-	-	-	100	P6	-
70.	I/O (D1)	45	69	73	70	101	T3	363
71.	I/O (RCLK-BUSY/RDY)	-	70	74	71	102	P5	366
72.	I/O (D0, DIN)	46	71	75	72	105	P4	372
73.	I/O (DOUT)	47	72	76	73	106	T2	375

# Product Obsolete or Under Obsolescence

## XC5200 Series Field Programmable Gate Arrays



Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
42.	I/O	-	-	-	-	-	28	C11	32	273
43.	I/O	25	19	16	23	25	29	B11	33	279
44.	I/O	26	20	17	24	26	30	A12	34	282
45.	I/O	-	-	-	25	27	31	B12	35	285
46.	I/O	-	-	-	26	28	32	A13	36	291
	GND	-	-	-	27	29	33	C12	37	-
47.	I/O	-	-	-	-	30	34	A15	40	294
48.	I/O	-	-	-	-	31	35	C13	41	297
49.	I/O	27	21	18	28	32	36	B14	42	303
50.	I/O	-	22	19	29	33	37	A16	43	306
51.	I/O	-	-	-	30	34	38	B15	44	309
52.	I/O	-	-	-	31	35	39	C14	45	315
53.	I/O	28	23	20	32	36	40	A17	46	318
54.	I/O	29	24	21	33	37	41	B16	47	321
55.	M1 (I/O)	30	25	22	34	38	42	C15	48	330
	GND	31	26	23	35	39	43	D15	49	-
56.	M0 (I/O)	32	27	24	36	40	44	A18	50	333
	VCC	33	28	25	37	41	45	D16	55	-
57.	M2 (I/O)	34	29	26	38	42	46	C16	56	336
58.	GCK2 (I/O)	35	30	27	39	43	47	B17	57	339
59.	I/O (HDC)	36	31	28	40	44	48	E16	58	348
60.	I/O	-	-	-	41	45	49	C17	59	351
61.	I/O	-	-	-	42	46	50	D17	60	354
62.	I/O	-	32	29	43	47	51	B18	61	360
63.	I/O (LDC)	37	33	30	44	48	52	E17	62	363
64.	I/O	-	-	-	-	49	53	F16	63	372
65.	I/O	-	-	-	-	50	54	C18	64	375
	GND	-	-	-	45	51	55	G16	67	-
66.	I/O	-	-	-	46	52	56	E18	68	378
67.	I/O	-	-	-	47	53	57	F18	69	384
68.	I/O	38	34	31	48	54	58	G17	70	387
69.	I/O	39	35	32	49	55	59	G18	71	390
70.	I/O	-	-	-	-	-	60	H16	72	396
71.	I/O	-	-	-	-	-	61	H17	73	399
72.	I/O	-	36	33	50	56	62	H18	74	402
73.	I/O	-	37	34	51	57	63	J18	75	408
74.	I/O	40	38	35	52	58	64	J17	76	411
75.	I/O (ERR, INIT)	41	39	36	53	59	65	J16	77	414
	VCC	42	40	37	54	60	66	J15	78	-
	GND	43	41	38	55	61	67	K15	79	-
76.	I/O	44	42	39	56	62	68	K16	80	420
77.	I/O	45	43	40	57	63	69	K17	81	423
78.	I/O	-	44	41	58	64	70	K18	82	426
79.	I/O	-	45	42	59	65	71	L18	83	432
80.	I/O	-	-	-	-	-	72	L17	84	435
81.	I/O	-	-	-	-	-	73	L16	85	438
82.	I/O	46	46	43	60	66	74	M18	86	444
83.	I/O	47	47	44	61	67	75	M17	87	447
84.	I/O	-	-	-	62	68	76	N18	88	450
85.	I/O	-	-	-	63	69	77	P18	89	456
	GND	-	-	-	64	70	78	M16	90	-
86.	I/O	-	-	-	-	71	79	T18	93	459

# Product Obsolete or Under Obsolescence

## XC5200 Series Field Programmable Gate Arrays



Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
	CCLK	73	77	74	107	119	131	V1	153	-
	VCC	74	78	75	108	120	132	R4	154	-
130.	I/O (TDO)	75	79	76	109	121	133	U2	159	-
	GND	76	80	77	110	122	134	R3	160	-
131.	I/O (A0, $\overline{WS}$ )	77	81	78	111	123	135	T3	161	9
132.	GCK4 (A1, I/O)	78	82	79	112	124	136	U1	162	15
133.	I/O	-	-	-	113	125	137	P3	163	18
134.	I/O	-	-	-	114	126	138	R2	164	21
135.	I/O (A2, CS1)	79	83	80	115	127	139	T2	165	27
136.	I/O (A3)	80	84	81	116	128	140	N3	166	30
137.	I/O	-	-	-	117	129	141	P2	167	33
138.	I/O	-	-	-	-	130	142	T1	168	42
	GND	-	-	-	118	131	143	M3	171	-
139.	I/O	-	-	-	119	132	144	P1	172	45
140.	I/O	-	-	-	120	133	145	N1	173	51
141.	I/O (A4)	81	85	82	121	134	146	M2	174	54
142.	I/O (A5)	82	86	83	122	135	147	M1	175	57
143.	I/O	-	-	-	-	-	148	L3	176	63
144.	I/O	-	-	-	-	136	149	L2	177	66
145.	I/O	-	87	84	123	137	150	L1	178	69
146.	I/O	-	88	85	124	138	151	K1	179	75
147.	I/O (A6)	83	89	86	125	139	152	K2	180	78
148.	I/O (A7)	84	90	87	126	140	153	K3	181	81
	GND	1	91	88	127	141	154	K4	182	-

### Additional No Connect (N.C.) Connections for PQ208 and TQ176 Packages

PQ208							TQ176
195	1	39	65	104	143	158	167
196	3	51	66	105	144	169	
206	12	52	91	107	155	170	
207	13	53	92	117	156		
208	38	54	102	118	157		

**Notes:** Boundary Scan Bit 0 = TDO.T  
 Boundary Scan Bit 1 = TDO.O  
 Boundary Scan Bit 1056 = BSCAN.UPD

### Pin Locations for XC5210 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
	VCC	2	128	142	155	183	J4	VCC*	212	-
1.	I/O (A8)	3	129	143	156	184	J3	E8	213	111
2.	I/O (A9)	4	130	144	157	185	J2	B7	214	114
3.	I/O	-	131	145	158	186	J1	A7	215	117
4.	I/O	-	132	146	159	187	H1	C7	216	123
5.	I/O	-	-	-	160	188	H2	D7	217	126
6.	I/O	-	-	-	161	189	H3	E7	218	129

# Product Obsolete or Under Obsolescence

## XC5200 Series Field Programmable Gate Arrays



Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
50.	I/O	24	20	22	24	28	B10	H5	32	330
51.	I/O	-	21	23	25	29	A9	J2	33	333
52.	I/O	-	22	24	26	30	A10	J1	34	339
53.	I/O	-	-	-	27	31	A11	J3	35	342
54.	I/O	-	-	-	28	32	C11	J4	36	345
55.	I/O	-	-	-	-	-	D11	J5	38	351
56.	I/O	-	-	-	-	-	D12	K1	39	354
	VCC	-	-	-	-	-	-	VCC*	40	-
57.	I/O	25	23	25	29	33	B11	K2	41	357
58.	I/O	26	24	26	30	34	A12	K3	42	363
59.	I/O	-	25	27	31	35	B12	J6	43	366
60.	I/O	-	26	28	32	36	A13	L1	44	369
	GND	-	27	29	33	37	C12	GND*	45	-
61.	I/O	-	-	-	-	-	D13	L2	46	375
62.	I/O	-	-	-	-	-	D14	K4	47	378
63.	I/O	-	-	-	-	38	B13	L3	48	381
64.	I/O	-	-	-	-	39	A14	M1	49	387
65.	I/O	-	-	30	34	40	A15	K5	50	390
66.	I/O	-	-	31	35	41	C13	M2	51	393
67.	I/O	27	28	32	36	42	B14	L4	52	399
68.	I/O	-	29	33	37	43	A16	N1	53	402
69.	I/O	-	30	34	38	44	B15	M3	54	405
70.	I/O	-	31	35	39	45	C14	N2	55	411
71.	I/O	28	32	36	40	46	A17	K6	56	414
72.	I/O	29	33	37	41	47	B16	P1	57	417
73.	M1 (I/O)	30	34	38	42	48	C15	N3	58	426
	GND	31	35	39	43	49	D15	GND*	59	-
74.	M0 (I/O)	32	36	40	44	50	A18	P2	60	429
	VCC	33	37	41	45	55	D16	VCC*	61	-
75.	M2 (I/O)	34	38	42	46	56	C16	M4	62	432
76.	GCK2 (I/O)	35	39	43	47	57	B17	R2	63	435
77.	I/O (HDC)	36	40	44	48	58	E16	P3	64	444
78.	I/O	-	41	45	49	59	C17	L5	65	447
79.	I/O	-	42	46	50	60	D17	N4	66	450
80.	I/O	-	43	47	51	61	B18	R3	67	456
81.	I/O (LDC)	37	44	48	52	62	E17	P4	68	459
82.	I/O	-	-	49	53	63	F16	K7	69	462
83.	I/O	-	-	50	54	64	C18	M5	70	468
84.	I/O	-	-	-	-	65	D18	R4	71	471
85.	I/O	-	-	-	-	66	F17	N5	72	474
86.	I/O	-	-	-	-	-	E15	P5	73	480
87.	I/O	-	-	-	-	-	F15	L6	74	483
	GND	-	45	51	55	67	G16	GND*	75	-
88.	I/O	-	46	52	56	68	E18	R5	76	486
89.	I/O	-	47	53	57	69	F18	M6	77	492
90.	I/O	38	48	54	58	70	G17	N6	78	495
91.	I/O	39	49	55	59	71	G18	P6	79	504
	VCC	-	-	-	-	-	-	VCC*	80	-
92.	I/O	-	-	-	60	72	H16	R6	81	507
93.	I/O	-	-	-	61	73	H17	M7	82	510
94.	I/O	-	-	-	-	-	G15	N7	84	516

# Product Obsolete or Under Obsolescence

## XC5200 Series Field Programmable Gate Arrays



Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
190.	I/O	-	-	-	X8	-	M4	951
191.	I/O	-	-	-	V9	-	L1	954
192.	I/O (D2)	106	138	159	W8	G11	J1	960
193.	I/O	107	139	160	X7	F15	K3	963
	VCC	-	-	161	X5	VCC*	VCC*	
194.	I/O	108	140	162	V8	F14	J2	966
195.	I/O	109	141	163	W7	F13	J3	972
196.	I/O	-	-	164	U8	G10	K4	975
197.	I/O	-	-	165	W6	E15	G1	978
	GND	110	142	166	X6	GND*	GND*	
198.	I/O	-	-	-	T8	-	H2	984
199.	I/O	-	-	-	V7	-	H3	987
200.	I/O	-	-	167	X4	E14	J4	990
201.	I/O	-	-	168	U7	F12	F1	996
202.	I/O	-	143	169	W5	E13	G2	999
203.	I/O	-	144	170	V6	D15	G3	1002
204.	I/O	111	145	171	T7	F11	F2	1008
205.	I/O	112	146	172	X3	D14	E2	1011
206.	I/O (D1)	113	147	173	U6	E12	F3	1014
207.	I/O (RCLK-BUSY/RDY)	114	148	174	V5	C15	G4	1020
208.	I/O	-	-	-	W4	-	D2	1023
209.	I/O	-	-	-	W3	-	F4	1032
210.	I/O	115	149	175	T6	D13	E3	1035
211.	I/O	116	150	176	U5	C14	C2	1038
212.	I/O (D0, DIN)	117	151	177	V4	F10	D3	1044
213.	I/O (DOUT)	118	152	178	X1	B15	E4	1047
	CCLK	119	153	179	V3	C13	C3	-
	VCC	120	154	180	W1	VCC*	VCC*	-
214.	I/O (TDO)	121	159	181	U4	A15	D4	0
	GND	122	160	182	X2	GND*	GND*	-
215.	I/O (A0, WS)	123	161	183	W2	A14	B3	9
216.	GCK4 (A1, I/O)	124	162	184	V2	B13	C4	15
217.	I/O	125	163	185	R5	E11	D5	18
218.	I/O	126	164	186	T4	C12	A3	21
219.	I/O (A2, CS1)	127	165	187	U3	A13	D6	27
220.	I/O (A3)	128	166	188	V1	B12	C6	30
221.	I/O	-	-	-	R4	-	B5	33
222.	I/O	-	-	-	P5	-	A4	39
223.	I/O	-	-	189	U2	F9	C7	42
224.	I/O	-	-	190	T3	D11	B6	45
225.	I/O	129	167	191	U1	A12	A6	51
226.	I/O	130	168	192	P4	C11	D8	54
227.	I/O	-	169	193	R3	B11	B7	57
228.	I/O	-	170	194	N5	E10	A7	63
229.	I/O	-	-	195	T2	-	D9	66
230.	I/O	-	-	-	R2	-	C9	69
	GND	131	171	196	T1	GND*	GND*	-
231.	I/O	132	172	197	N4	A11	B8	75
232.	I/O	133	173	198	P3	D10	D10	78
233.	I/O	-	-	199	P2	C10	C10	81
234.	I/O	-	-	200	N3	B10	B9	87
	VCC	-	-	201	R1	VCC*	VCC*	-

# Product Obsolete or Under Obsolescence



## XC5200 Series Field Programmable Gate Arrays

Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
235.	I/O	-	-	-	M5	-	B11	90
236.	I/O	-	-	-	P1	-	A11	93
237.	I/O (A4)	134	174	202	N1	A10	D12	99
238.	I/O (A5)	135	175	203	M3	D9	C12	102
239.	I/O	-	176	205	M2	C9	B12	105
240.	I/O	136	177	206	L5	B9	A12	111
241.	I/O	137	178	207	M1	A9	C13	114
242.	I/O	138	179	208	L4	E9	B13	117
243.	I/O (A6)	139	180	209	L3	C8	A13	126
244.	I/O (A7)	140	181	210	L2	B8	B14	129
	GND	141	182	211	L1	GND*	GND*	-

### Additional No Connect (N.C.) Connections for HQ208 and HQ240 Packages

HQ208		HQ240
206	102	219
207	104	22
208	105	37
1	107	83
3	155	98
51	156	143
52	157	158
53	158	204
54	-	-

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**Notes:** \* Pins labeled VCC\* are internally bonded to a VCC plane within the BG225 and BG352 packages. The external pins for the BG225 are: B2, D8, H15, R8, B14, R1, H1, and R15. The external pins for the BG352 are: A10, A17, B2, B25, D13, D19, D7, G23, H4, K1, K26, N23, P4, U1, U26, W23, Y4, AC14, AC20, AC8, AE2, AE25, AF10, and AF17.  
Pins labeled GND\* are internally bonded to a ground plane within the BG225 and BG352 packages. The external pins for the BG225 are: A1, D12, G7, G9, H6, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8. The external pins for the BG352 are: A1, A2, A5, A8, A14, A19, A22, A25, A26, B1, B26, E1, E26, H1, H26, N1, P26, W1, W26, AB1, AB26, AE1, AE26, AF1, AF13, AF19, AF2, AF22, AF25, AF26, AF5, AF8.

Boundary Scan Bit 0 = TDO.T  
Boundary Scan Bit 1 = TDO.O  
Boundary Scan Bit 1056 = BSCAN.UPD

# Product Obsolete or Under Obsolescence



## XC5200 Series Field Programmable Gate Arrays

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### Revisions

Version	Description
12/97	Rev 5.0 added -3, -4 specification
7/98	Rev 5.1 added Spartan family to comparison, removed HQ304
11/98	Rev 5.2 All specifications made final.