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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	196
Number of Logic Elements/Cells	784
Total RAM Bits	-
Number of I/O	133
Number of Gates	10000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc5206-6pq160c

XC5200 Family Compared to XC4000/Spartan™ and XC3000 Series

For readers already familiar with the XC4000/Spartan and XC3000 FPGA Families, this section describes significant differences between them and the XC5200 family. Unless otherwise indicated, comparisons refer to both XC4000/Spartan and XC3000 devices.

Configurable Logic Block (CLB) Resources

Each XC5200 CLB contains four independent 4-input function generators and four registers, which are configured as four independent Logic Cells™ (LCs). The registers in each XC5200 LC are optionally configurable as edge-triggered D-type flip-flops or as transparent level-sensitive latches.

The XC5200 CLB includes dedicated carry logic that provides fast arithmetic carry capability. The dedicated carry logic may also be used to cascade function generators for implementing wide arithmetic functions.

XC4000 family: XC5200 devices have no wide edge decoders. Wide decoders are implemented using cascade logic. Although sacrificing speed for some designs, lack of wide edge decoders reduces the die area and hence cost of the XC5200.

XC4000/Spartan family: XC5200 dedicated carry logic differs from that of the XC4000/Spartan family in that the sum is generated in an additional function generator in the adjacent column. This design reduces XC5200 die size and hence cost for many applications. Note, however, that a loadable up/down counter requires the same number of function generators in both families. XC3000 has no dedicated carry.

XC4000/Spartan family: XC5200 lookup tables are optimized for cost and hence cannot implement RAM.

Input/Output Block (IOB) Resources

The XC5200 family maintains footprint compatibility with the XC4000 family, but not with the XC3000 family.

To minimize cost and maximize the number of I/O per Logic Cell, the XC5200 I/O does not include flip-flops or latches.

For high performance paths, the XC5200 family provides direct connections from each IOB to the registers in the adjacent CLB in order to emulate IOB registers.

Each XC5200 I/O Pin provides a programmable delay element to control input set-up time. This element can be used to avoid potential hold-time problems. Each XC5200 I/O Pin is capable of 8-mA source and sink currents.

IEEE 1149.1-type boundary scan is supported in each XC5200 I/O.

Table 2: Xilinx Field-Programmable Gate Array Families

Parameter	XC5200	Spartan	XC4000	XC3000
CLB function generators	4	3	3	2
CLB inputs	20	9	9	5
CLB outputs	12	4	4	2
Global buffers	4	8	8	2
User RAM	no	yes	yes	no
Edge decoders	no	no	yes	no
Cascade chain	yes	no	no	no
Fast carry logic	yes	yes	yes	no
Internal 3-state	yes	yes	yes	yes
Boundary scan	yes	yes	yes	no
Slew-rate control	yes	yes	yes	yes

Routing Resources

The XC5200 family provides a flexible coupling of logic and local routing resources called the VersaBlock. The XC5200 VersaBlock element includes the CLB, a Local Interconnect Matrix (LIM), and direct connects to neighboring VersaBlocks.

The XC5200 provides four global buffers for clocking or high-fanout control signals. Each buffer may be sourced by means of its dedicated pad or from any internal source.

Each XC5200 TBUF can drive up to two horizontal and two vertical Longlines. There are no internal pull-ups for XC5200 Longlines.

Configuration and Readback

The XC5200 supports a new configuration mode called Express mode.

XC4000/Spartan family: The XC5200 family provides a global reset but not a global set.

XC5200 devices use a different configuration process than that of the XC3000 family, but use the same process as the XC4000 and Spartan families.

XC3000 family: Although their configuration processes differ, XC5200 devices may be used in daisy chains with XC3000 devices.

XC3000 family: The XC5200 PROGRAM pin is a single-function input pin that overrides all other inputs. The PROGRAM pin does not exist in XC3000.

XC3000 family: XC5200 devices support an additional programming mode: Peripheral Synchronous.

XC3000 family: The XC5200 family does not support Power-down, but offers a Global 3-state input that does not reset any flip-flops.

XC3000 family: The XC5200 family does not provide an on-chip crystal oscillator amplifier, but it does provide an internal oscillator from which a variety of frequencies up to 12 MHz are available.

Architectural Overview

Figure 1 presents a simplified, conceptual overview of the XC5200 architecture. Similar to conventional FPGAs, the XC5200 family consists of programmable IOBs, programmable logic blocks, and programmable interconnect. Unlike other FPGAs, however, the logic and local routing resources of the XC5200 family are combined in flexible VersaBlocks (Figure 2). General-purpose routing connects to the VersaBlock through the General Routing Matrix (GRM).

VersaBlock: Abundant Local Routing Plus Versatile Logic

The basic logic element in each VersaBlock structure is the Logic Cell, shown in Figure 3. Each LC contains a 4-input function generator (F), a storage device (FD), and control logic. There are five independent inputs and three outputs to each LC. The independence of the inputs and outputs allows the software to maximize the resource utilization within each LC. Each Logic Cell also contains a direct feedthrough path that does not sacrifice the use of either the function generator or the register; this feature is a first for FPGAs. The storage device is configurable as either a D flip-flop or a latch. The control logic consists of carry logic for fast implementation of arithmetic functions, which can also be configured as a cascade chain allowing decode of very wide input functions.

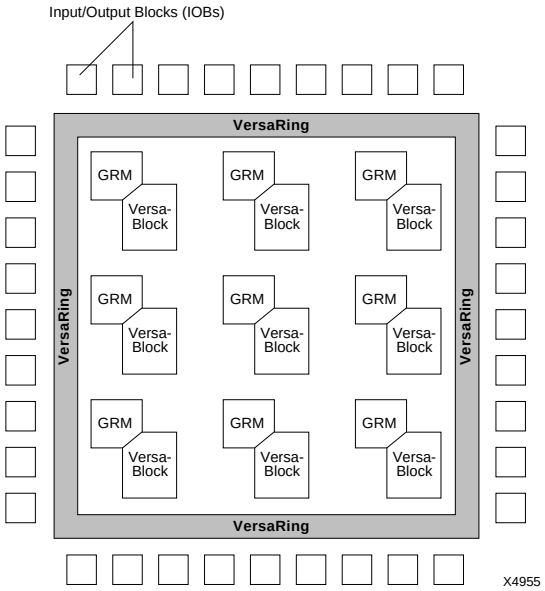


Figure 1: XC5200 Architectural Overview

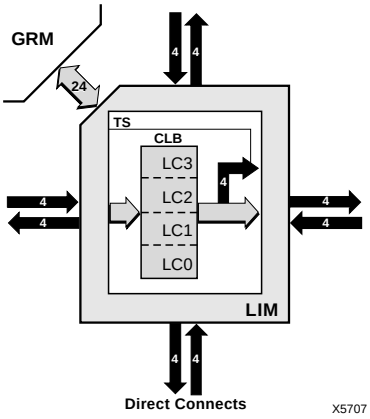


Figure 2: VersaBlock

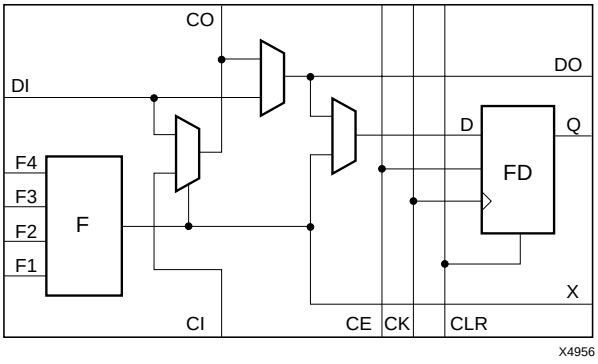


Figure 3: XC5200 Logic Cell (Four LCs per CLB)

tomized RPMs, freeing the designer from the need to become an expert on architectures.

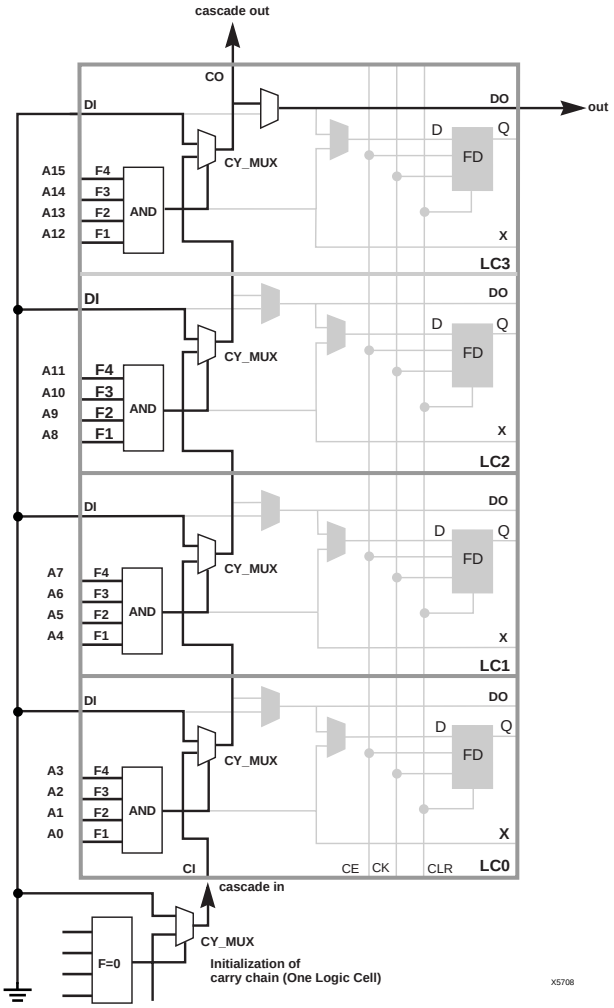


Figure 7: XC5200 CY_MUX Used for Decoder Cascade Logic

Cascade Function

Each CY_MUX can be connected to the CY_MUX in the adjacent LC to provide cascadable decode logic. Figure 7 illustrates how the 4-input function generators can be configured to take advantage of these four cascaded CY_MUXes. Note that AND and OR cascading are specific cases of a general decode. In AND cascading all bits are decoded equal to logic one, while in OR cascading all bits are decoded equal to logic zero. The flexibility of the LUT achieves this result. The XC5200 library contains gate macros designed to take advantage of this function.

CLB Flip-Flops and Latches

The CLB can pass the combinatorial output(s) to the interconnect network, but can also store the combinatorial results or other incoming data in flip-flops, and connect their outputs to the interconnect network as well. The CLB storage elements can also be configured as latches.

Table 3: CLB Storage Element Functionality (active rising edge is shown)

Mode	CK	CE	CLR	D	Q
Power-Up or GR	X	X	X	X	0
Flip-Flop	X	X	1	X	0
	__/	1*	0*	D	D
	0	X	0*	X	Q
Latch	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X _	Don't care
__/	Rising edge
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

Data Inputs and Outputs

The source of a storage element data input is programmable. It is driven by the function F, or by the Direct In (DI) block input. The flip-flops or latches drive the Q CLB outputs.

Four fast feed-through paths from DI to DO are available, as shown in Figure 4. This bypass is sometimes used by the automated router to repower internal signals. In addition to the storage element (Q) and direct (DO) outputs, there is a combinatorial output (X) that is always sourced by the Lookup Table.

The four edge-triggered D-type flip-flops or level-sensitive latches have common clock (CK) and clock enable (CE) inputs. Any of the clock inputs can also be permanently enabled. Storage element functionality is described in Table 3.

Clock Input

The flip-flops can be triggered on either the rising or falling clock edge. The clock pin is shared by all four storage elements with individual polarity control. Any inverter placed on the clock input is automatically absorbed into the CLB.

Clock Enable

The clock enable signal (CE) is active High. The CE pin is shared by the four storage elements. If left unconnected for any, the clock enable for that storage element defaults to the active state. CE is not invertible within the CLB.

Clear

An asynchronous storage element input (CLR) can be used to reset all four flip-flops or latches in the CLB. This input

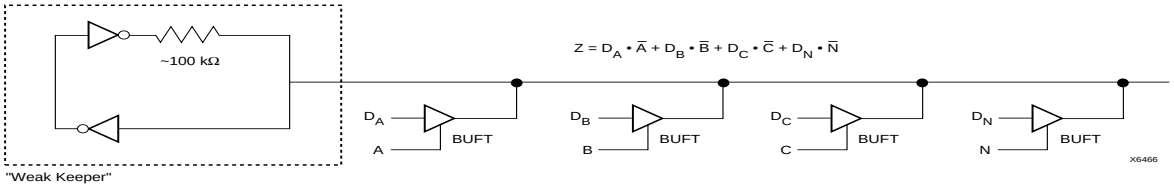


Figure 10: 3-State Buffers Implement a Multiplexer

Input/Output Blocks

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

The I/O block, shown in Figure 11, consists of an input buffer and an output buffer. The output driver is an 8-mA full-rail CMOS buffer with 3-state control. Two slew-rate control modes are supported to minimize bus transients. Both the output buffer and the 3-state control are invertible. The input buffer has globally selected CMOS or TTL input thresholds. The input buffer is invertible and also provides a programmable delay line to assure reliable chip-to-chip set-up and hold times. Minimum ESD protection is 3 KV using the Human Body Model.

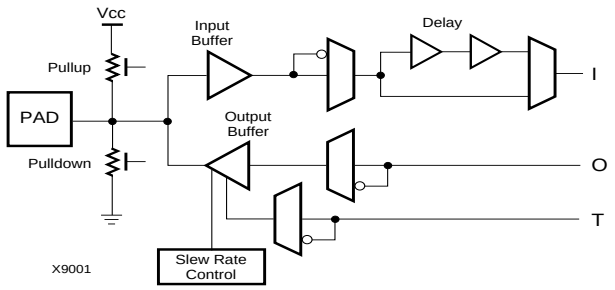


Figure 11: XC5200 I/O Block

IOB Input Signals

The XC5200 inputs can be globally configured for either TTL (1.2V) or CMOS thresholds, using an option in the bitstream generation software. There is a slight hysteresis of about 300mV.

The inputs of XC5200-Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC5200-Series device inputs are shown in Table 5.

Table 5: Supported Sources for XC5200-Series Device Inputs

Source	XC5200 Input Mode	
	5 V, TTL	5 V, CMOS
Any device, Vcc = 3.3 V, CMOS outputs	√	**Unreliable Data**
Any device, Vcc = 5 V, TTL outputs	√	
Any device, Vcc = 5 V, CMOS outputs	√	√

Optional Delay Guarantees Zero Hold Time

XC5200 devices do not have storage elements in the IOBs. However, XC5200 IOBs can be efficiently routed to CLB flip-flops or latches to store the I/O signals.

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the CLB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the CLB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the software default.

The XC5200 IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC5200 global clock buffers. (See "Global Lines" on page 96 for a description of the global clock buffers in the XC5200.) For a shorter input register setup time, with

non-zero hold, attach a NODELAY attribute or property to the flip-flop or input buffer.

IOB Output Signals

Output signals can be optionally inverted within the IOB, and pass directly to the pad. As with the inputs, a CLB flip-flop or latch can be used to store the output signal.

An active-High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (OUT) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB.

The XC5200 devices provide a guaranteed output sink current of 8 mA.

Supported destinations for XC5200-Series device outputs are shown in Table 6.(For a detailed discussion of how to interface between 5 V and 3.3 V devices, see the 3V Products section of *The Programmable Logic Data Book*.)

An output can be configured as open-drain (open-collector) by placing an OBUFT symbol in a schematic or HDL code, then tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground. (See Figure 12.)

Table 6: Supported Destinations for XC5200-Series Outputs

Destination	XC5200 Output Mode
	5 V, CMOS
XC5200 device, V_{CC}=3.3 V, CMOS-threshold inputs	√
Any typical device, V_{CC} = 3.3 V, CMOS-threshold inputs	some[1]
Any device, V_{CC} = 5 V, TTL-threshold inputs	√
Any device, V_{CC} = 5 V, CMOS-threshold inputs	√

1. Only if destination device has 5-V tolerant inputs

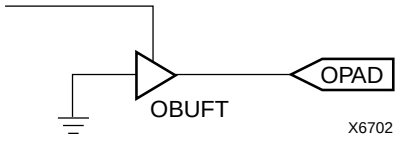


Figure 12: Open-Drain Output

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

For XC5200 devices, maximum total capacitive load for simultaneous fast mode switching in the same direction is 200 pF for all package pins between each Power/Ground pin pair. For some XC5200 devices, additional internal Power/Ground pin pairs are connected to special Power and Ground planes within the packages, to reduce ground bounce.

For slew-rate limited outputs this total is two times larger for each device type: 400 pF for XC5200 devices. This maximum capacitive load should not be exceeded, as it can result in ground bounce of greater than 1.5 V amplitude and more than 5 ns duration. This level of ground bounce may cause undesired transient behavior on an output, or in the internal logic. This restriction is common to all high-speed digital ICs, and is not particular to Xilinx or the XC5200 Series.

XC5200-Series devices have a feature called “Soft Start-up,” designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Global Three-State

A separate Global 3-State line (not shown in Figure 11) forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. This global net (GTS) does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-State signal. Using GTS is similar to Global Reset. See Figure 8 on page 90 for details. Alternatively, GTS can be driven from any internal node.

Other IOB Options

There are a number of other programmable options in the XC5200-Series IOB.

Pull-up and Pull-down Resistors

Programmable IOB pull-up and pull-down resistors are useful for tying unused pins to Vcc or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls

segments span the width and height of the chip, respectively.

Two low-skew horizontal and vertical unidirectional global-line segments span each row and column of the chip, respectively.

Single- and Double-Length Lines

The single- and double-length bidirectional line segments make up the bulk of the routing channels. The double-length lines hop across every other CLB to reduce the propagation delays in speed-critical nets. Regenerating the signal strength is recommended after traversing three or four such segments. Xilinx place-and-route software automatically connects buffers in the path of the signal as necessary. Single- and double-length lines cannot drive onto Longlines and global lines; Longlines and global lines can, however, drive onto single- and double-length lines. As a general rule, Longline and global-line connections to the general routing matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

Longlines

Longlines are used for high-fan-out signals, 3-state busses, low-skew nets, and faraway destinations. Row and column splitter PIPs in the middle of the array effectively double the total number of Longlines by electrically dividing them into two separated half-lines. Longlines are driven by the 3-state buffers in each CLB, and are driven by similar buffers at the periphery of the array from the VersaRing I/O Interface.

Bus-oriented designs are easily implemented by using Longlines in conjunction with the 3-state buffers in the CLB and in the VersaRing. Additionally, weak keeper cells at the periphery retain the last valid logic level on the Longlines when all buffers are in 3-state mode.

Longlines connect to the single-length or double-length lines, or to the logic inside the CLB, through the General Routing Matrix. The only manner in which a Longline can be driven is through the four 3-state buffers; therefore, a Longline-to-Longline or single-line-to-Longline connection through PIPs in the General Routing Matrix is not possible. Again, as a general rule, long- and global-line connections to the General Routing Matrix are unidirectional, with the signal direction from these lines toward the routing matrix.

The XC5200 family has no pull-ups on the ends of the Longlines sourced by TBUFs, unlike the XC4000 Series. Consequently, wired functions (i.e., WAND and WORAND) and wide multiplexing functions requiring pull-ups for undefined states (i.e., bus applications) must be implemented in a different way. In the case of the wired functions, the same functionality can be achieved by taking advantage of the carry/cascade logic described above, implementing a wide logic function in place of the wired function. In the case of 3-state bus applications, the user must insure that all states of the multiplexing function are defined. This process is as simple as adding an additional TBUF to drive the bus High when the previously undefined states are activated.

Global Lines

Global buffers in Xilinx FPGAs are special buffers that drive a dedicated routing network called Global Lines, as shown in Figure 16. This network is intended for high-fanout clocks or other control signals, to maximize speed and minimize skewing while distributing the signal to many loads.

The XC5200 family has a total of four global buffers (BUFG symbol in the library), each with its own dedicated routing channel. Two are distributed vertically and two horizontally throughout the FPGA.

The global lines provide direct input only to the CLB clock pins. The global lines also connect to the General Routing Matrix to provide access from these lines to the function generators and other control signals.

Four clock input pads at the corners of the chip, as shown in Figure 16, provide a high-speed, low-skew clock network to each of the four global-line buffers. In addition to the dedicated pad, the global lines can be sourced by internal logic. PIPs from several routing channels within the VersaRing can also be configured to drive the global-line buffers.

Details of all the programmable interconnect for a CLB is shown in Figure 17.

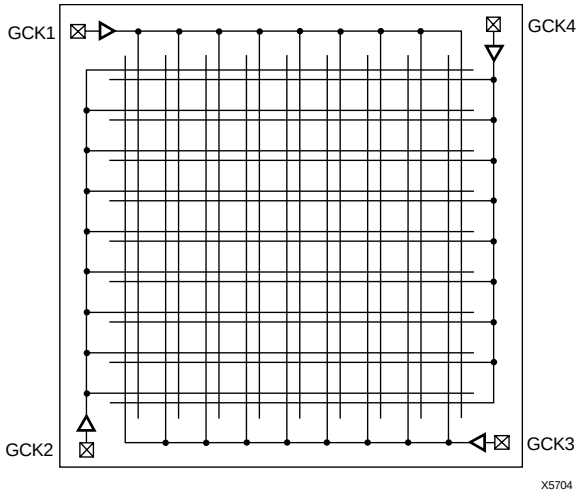


Figure 16: Global Lines

Table 9: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor (20 kΩ - 100 kΩ) that defines the logic level as High.

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC5200-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary I/O connections. The development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC5200-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 3.3kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

XC5200 devices have seven configuration modes. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode,

Table 10: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note :*Peripheral Synchronous can be considered byte-wide Slave Parallel

which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration. The coding for mode selection is shown in Table 10.

Note that the smallest package, VQ64, only supports the Master Serial, Slave Serial, and Express modes.A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 13 on page 124.

Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The

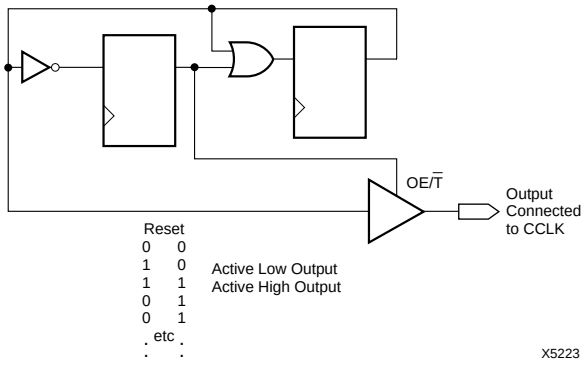


Figure 22: CCLK Generation for XC3000 Master Driving an XC5200-Series Slave

Express Mode

Express mode is similar to Slave Serial mode, except the data is presented in parallel format, and is clocked into the target device a byte at a time rather than a bit at a time. The data is loaded in parallel into eight different columns: it is not internally serialized. Eight bits of configuration data are loaded with every CCLK cycle, therefore this configuration mode runs at eight times the data rate of the other six modes. In this mode the XC5200 family is capable of supporting a CCLK frequency of 10 MHz, which is equivalent to an 80 MHz serial rate, because eight bits of configuration data are being loaded per CCLK cycle. An XC5210 in the Express mode, for instance, can be configured in about 2 ms. The Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

In the Express configuration mode, an external signal drives the CCLK input(s). The first byte of parallel configuration data must be available at the D inputs of the FPGA devices a short set-up time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge. See Figure 38 on page 123.

Bitstream generation currently generates a bitstream sufficient to program in all configuration modes except Express. Extra CCLK cycles are necessary to complete the configuration, since in this mode data is read at a rate of eight bits per CCLK cycle instead of one bit per cycle. Normally the entire start-up sequence requires a number of bits that is equal to the number of CCLK cycles needed. An additional five CCLKs (equivalent to 40 extra bits) will guarantee completion of configuration, regardless of the start-up options chosen.

Multiple slave devices with identical configurations can be wired with parallel D0-D7 inputs. In this way, multiple devices can be configured simultaneously.

Pseudo Daisy Chain

Multiple devices with different configurations can be connected together in a pseudo daisy chain, provided that all of the devices are in Express mode. A single combined bitstream is used to configure the chain of Express mode devices, but the input data bus must drive D0-D7 of each device. Tie High the CS1 pin of the first device to be configured, or leave it floating in the XC5200 since it has an internal pull-up. Connect the DOUT pin of each FPGA to the CS1 pin of the next device in the chain. The D0-D7 inputs are wired to each device in parallel. The DONE pins are wired together, with one or more internal DONE pull-ups activated. Alternatively, a 4.7 kΩ external resistor can be used, if desired. (See Figure 37 on page 122.) CCLK pins are tied together.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All devices in Express mode are synchronized to the DONE pin. User I/O for each device become active after the DONE pin for that device goes High. (The exact timing is determined by options to the bitstream generation software.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle.

The status pin DOUT is pulled LOW two internal-oscillator cycles (nominally 1 MHz) after $\overline{\text{INIT}}$ is recognized as High, and remains Low until the device's configuration memory is full. Then DOUT is pulled High to signal the next device in the chain to accept the configuration data on the D7-D0 bus. All devices receive and recognize the six bytes of preamble and length count, irrespective of the level on CS1; but subsequent frame data is accepted only when CS1 is High and the device's configuration memory is not already full.

Setting CCLK Frequency

For Master modes, CCLK can be generated in one of three frequencies. In the default slow mode, the frequency is nominally 1 MHz. In fast CCLK mode, the frequency is nominally 12 MHz. In medium CCLK mode, the frequency is nominally 6 MHz. The frequency range is -50% to +50%. The frequency is selected by an option when running the bitstream generation software. If an XC5200-Series Master is driving an XC3000- or XC2000-family slave, slow CCLK mode must be used. Slow mode is the default.

Table 11: XC5200 Bitstream Format

Data Type	Value	Occurrences
Fill Byte	11111111	Once per bitstream
Preamble	11110010	
Length Counter	COUNT(23:0)	
Fill Byte	11111111	

Table 11: XC5200 Bitstream Format

Data Type	Value	Occurrences
Start Byte	11111110	Once per data frame
Data Frame *	DATA(N-1:0)	
Cyclic Redundancy Check or Constant Field Check	CRC(3:0) or 0110	
Fill Nibble	1111	
Extend Write Cycle	FFFFFF	
Postamble	11111110	Once per device
Fill Bytes (30)	FFFF…FF	
Start-Up Byte	FF	Once per bitstream
*Bits per Frame (N) depends on device size, as described for table 11.		

Data Stream Format

The data stream ("bitstream") format is identical for all configuration modes, with the exception of Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode.

The data stream formats are shown in Table 11. Express mode data is shown with D0 at the left and D7 at the right. For all other modes, bit-serial data is read from left to right, and byte-parallel data is effectively assembled from this serial bitstream, with the first bit in each byte assigned to D0.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 12). Each frame begins with a start field and ends with an error check. In all modes except Express mode, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All startup bytes are don't-cares; these bytes are not included in bitstreams created by the Xilinx software.

In Express mode, only non-CRC error checking is supported. In all other modes, a selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading and the pulling down of the $\overline{\text{INIT}}$ pin. In Master modes, CCLK and address signals continue to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling Vcc.

Table 12: Internal Configuration Data Structure

Device	VersaBlock Array	PROM Size (bits)	Xilinx Serial PROM Needed
XC5202	8 x 8	42,416	XC1765E
XC5204	10 x 12	70,704	XC17128E
XC5206	14 x 14	106,288	XC17128E
XC5210	18 x 18	165,488	XC17256E
XC5215	22 x 22	237,744	XC17256E

Bits per Frame = (34 x number of Rows) + 28 for the top + 28 for the bottom + 4 splitter bits + 8 start bits + 4 error check bits + 4 fill bits * + 24 extended write bits
= (34 x number of Rows) + 100
* In the XC5202 (8 x 8), there are 8 fill bits per frame, not 4

Number of Frames = (12 x number of Columns) + 7 for the left edge + 8 for the right edge + 1 splitter bit
= (12 x number of Columns) + 16

Program Data = (Bits per Frame x Number of Frames) + 48 header bits + 8 postamble bits + 240 fill bits + 8 start-up bits
= (Bits per Frame x Number of Frames) + 304

PROM Size = Program Data

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 11. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 23. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Read Capture option not used). Statistically, one error out of 2048 might go undetected.

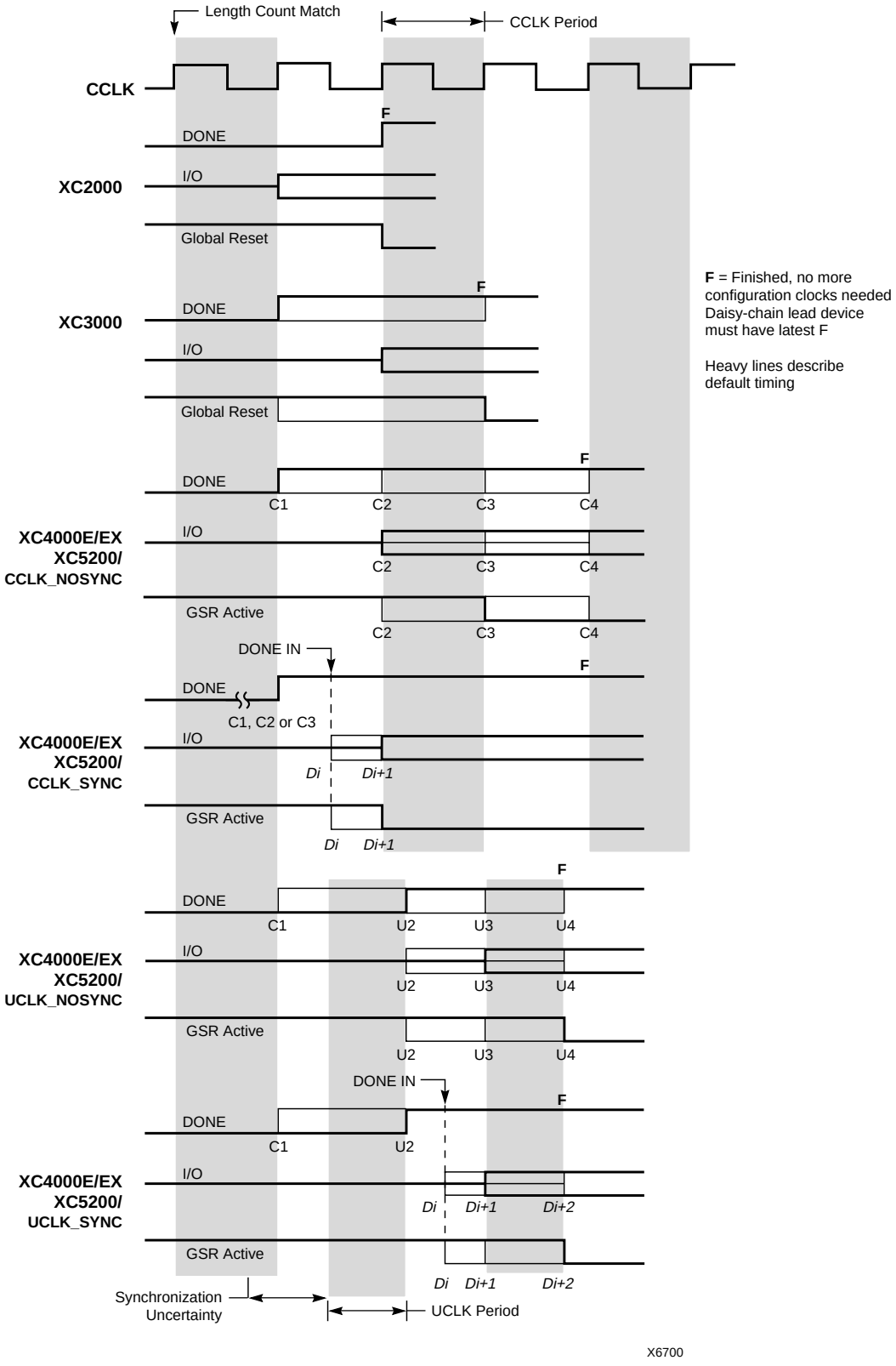


Figure 25: Start-up Timing

Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin.

There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 28 shows a full master/slave system. An XC5200-Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

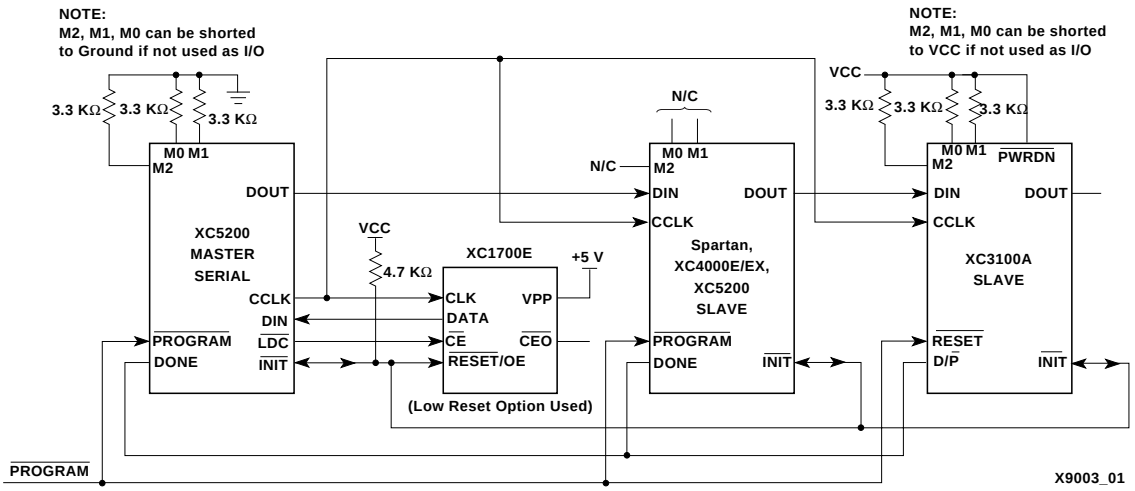
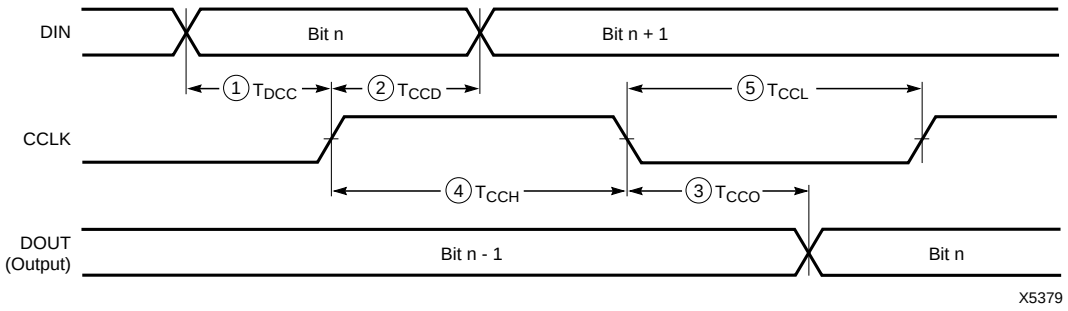


Figure 28: Master/Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 29: Slave Serial Mode Programming Switching Characteristics

Express Mode

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers. A CCLK frequency of 10 MHz is equivalent to an 80 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking.

In Express mode, an external signal drives the CCLK input of the FPGA device. The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge.

If the first device is configured in Express mode, additional devices may be daisy-chained only if every device in the chain is also configured in Express mode. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pullup). Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The status pin DOUT is pulled Low two internal-oscillator cycles after INIT is recognized as High, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using an option in the bitstream generation software.

XC5200 devices in Express mode are always synchronized to DONE. The device becomes active after DONE goes High. DONE is an open-drain output. With the DONE pins tied together, therefore, the external DONE signal stays low until all devices are configured, then all devices in the daisy chain become active simultaneously. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured.

Express mode is selected by a <010> on the mode pins (M2, M1, M0).

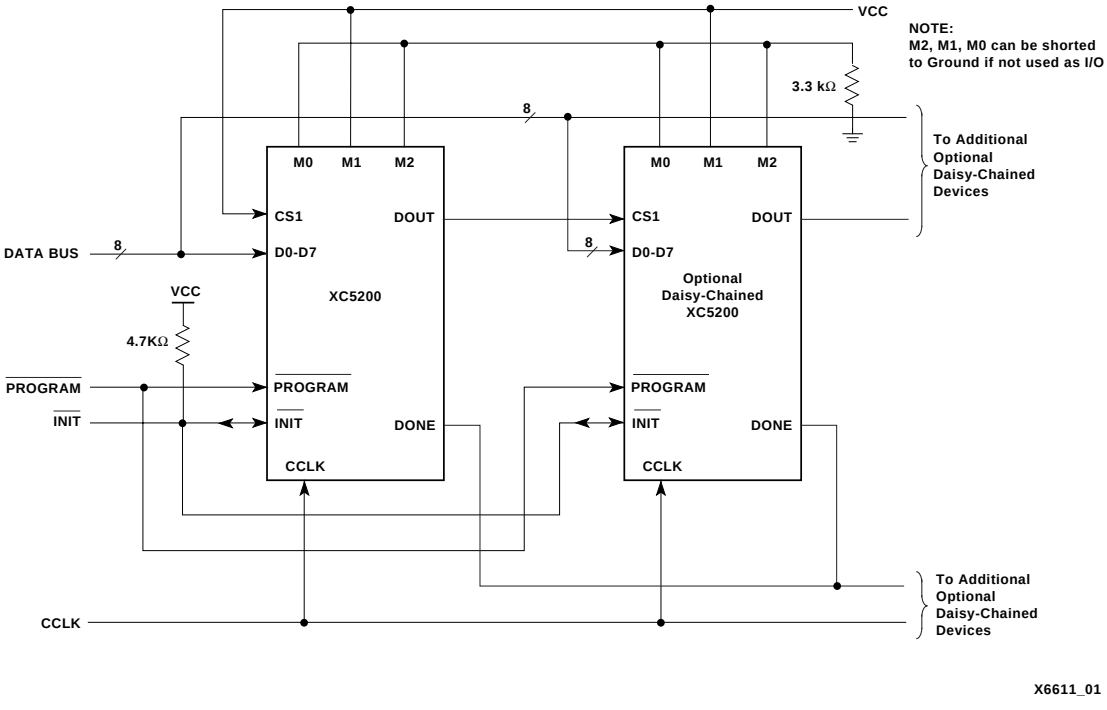
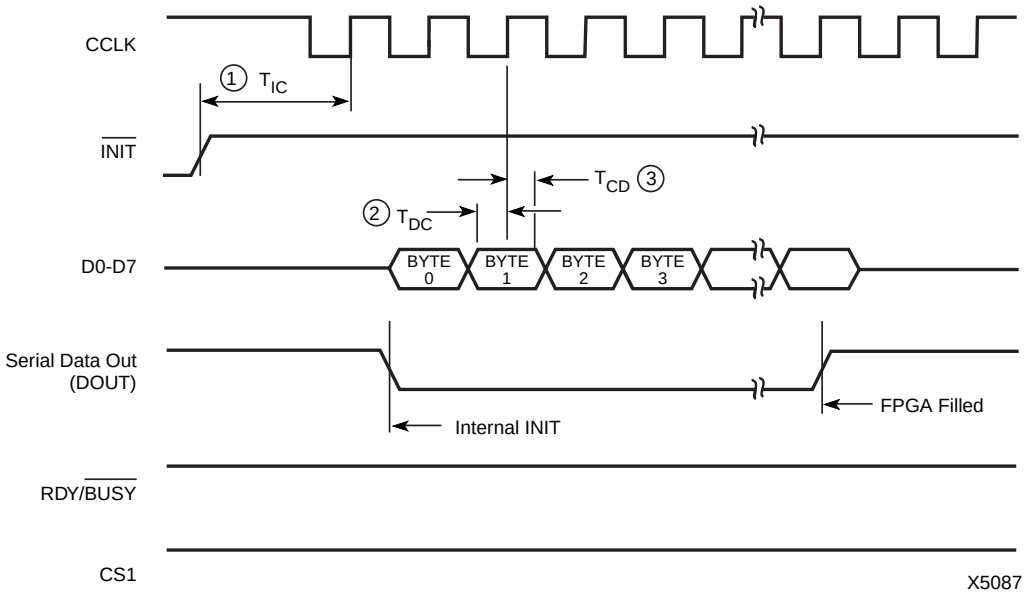


Figure 37: Express Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	INIT (High) Setup time required	1	T_{IC}	5		µs
	DIN Setup time required	2	T_{DC}	30		ns
	DIN hold time required	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	30		ns
	CCLK Low time		T_{CCL}	30		ns
	CCLK frequency		F_{CC}		10	MHz

Note: If not driven by the preceding DOUT, CS1 must remain high until the device is fully configured.

Figure 38: Express Mode Programming Switching Characteristics

Table 13. Pin Functions During Configuration

CONFIGURATION MODE: <M2:M1:M0>							USER OPERATION
SLAVE <1:1:1>	MASTER-SER <0:0:0>	SYN.PERIPH <0:1:1>	ASYN.PERIPH <1:0:1>	MASTER-HIGH <1:1:0>	MASTER-LOW <1:0:0>	EXPRESS <0:1:0>	
				A16	A16		GCK1-I/O
				A17	A17		I/O
TDI	TDI	TDI	TDI	TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK	TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS	TMS	TMS	TMS	TMS-I/O
							I/O
M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	M1 (LOW) (I)	M1 (HIGH) (I)	I/O
M0 (HIGH) (I)	M0 (LOW) (I)	M0 (HIGH) (I)	M0 (HIGH) (I)	M0 (LOW) (I)	M0 (LOW) (I)	M0 (LOW) (I)	I/O
M2 (HIGH) (I)	M2 (LOW) (I)	M2 (LOW) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (HIGH) (I)	M2 (LOW) (I)	I/O
							GCK2-I/O
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	LDC (LOW)	I/O
$\overline{\text{INIT}}$-ERROR	$\overline{\text{INIT}}$-ERROR	$\overline{\text{INIT}}$-ERROR	$\overline{\text{INIT}}$-ERROR	$\overline{\text{INIT}}$-ERROR	$\overline{\text{INIT}}$-ERROR	$\overline{\text{INIT}}$-ERROR	I/O
							I/O
DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
		DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	DATA 7 (I)	I/O
							GCK3-I/O
		DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	DATA 6 (I)	I/O
		DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	DATA 5 (I)	I/O
			$\overline{\text{CSO}}$ (I)				I/O
		DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	DATA 4 (I)	I/O
		DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	DATA 3 (I)	I/O
			$\overline{\text{RS}}$ (I)				I/O
		DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	DATA 2 (I)	I/O
		DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	DATA 1 (I)	I/O
		RDY/$\overline{\text{BUSY}}$	RDY/$\overline{\text{BUSY}}$	RCLK	RCLK		I/O
DIN (I)	DIN (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	DOUT	I/O
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (O)	CCLK (O)	CCLK (O)	CCLK (I)	CCLK (I)
TDO	TDO	TDO	TDO	TDO	TDO	TDO	TDO-I/O
			$\overline{\text{WS}}$ (I)	A0	A0		I/O
				A1	A1		GCK4-I/O
			CS1 (I)	A2	A2	CS1 (I)	I/O
				A3	A3		I/O
				A4	A4		I/O
				A5	A5		I/O
				A6	A6		I/O
				A7	A7		I/O
				A8	A8		I/O
				A9	A9		I/O
				A10	A10		I/O
				A11	A11		I/O
				A12	A12		I/O
				A13	A13		I/O
				A14	A14		I/O
				A15	A15		I/O
							ALL OTHERS

Notes: 1. A shaded table cell represents a 20-kΩ to 100-kΩ pull-up resistor before and during configuration.
2. (I) represents an input (O) represents an output.
3. INIT is an open-drain output during configuration.

XC5200 Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC5200 Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial: 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial: -40°C to 100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

XC5200 DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -8.0 mA, V_{CC} min	3.86		V
V_{OL}	Low-level output voltage @ I_{OL} = 8.0 mA, V_{CC} max		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 1)		15	mA
I_{IL}	Leakage current	-10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.30	mA

Note: 1. With no output current loads, all package pins at Vcc or GND, either TTL or CMOS inputs, and the FPGA configured with a tie option.

XC5200 Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature in plastic packages	+125	°C
	Junction temperature in ceramic packages	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
35.	I/O (HDC)	19	36	31	28	40	D14	204
36.	I/O	-	-	32	29	43	E14	207
37.	I/O (LDC)	20	37	33	30	44	C16	210
	GND	-	-	-	-	45	F14	-
38.	I/O	-	38	34	31	48	F16	216
39.	I/O	21	39	35	32	49	G14	219
40.	I/O	-	-	36	33	50	G15	222
41.	I/O	-	-	37	34	51	G16	228
42.	I/O	22	40	38	35	52	H16	231
43.	I/O ($\overline{ERR}$, $\overline{INIT}$)	23	41	39	36	53	H15	234
	VCC	24	42	40	37	54	H14	-
	GND	25	43	41	38	55	J14	-
44.	I/O	26	44	42	39	56	J15	240
45.	I/O	27	45	43	40	57	J16	243
46.	I/O	-	-	44	41	58	K16	246
47.	I/O	-	-	45	42	59	K15	252
48.	I/O	28	46	46	43	60	K14	255
49.	I/O	29	47	47	44	61	L16	258
	GND	-	-	-	-	64	L14	-
50.	I/O	-	48	48	45	65	P16	264
51.	I/O	30	49	49	46	66	M14	267
52.	I/O	-	50	50	47	69	N14	276
53.	I/O	31	51	51	48	70	R16	279
	GND	-	52	52	49	71	P14	-
	DONE	32	53	53	50	72	R15	-
	VCC	33	54	54	51	73	P13	-
	PROG	34	55	55	52	74	R14	-
54.	I/O (D7)	35	56	56	53	75	T16	288
55.	GCK3 (I/O)	36	57	57	54	76	T15	291
56.	I/O (D6)	37	58	58	55	79	T14	300
57.	I/O	-	-	59	56	80	T13	303
	GND	-	-	-	-	81	P11	-
58.	I/O (D5)	38	59	60	57	84	T10	306
59.	I/O ($\overline{CS0}$)	-	60	61	58	85	P10	312
60.	I/O	-	-	62	59	86	R10	315
61.	I/O	-	-	63	60	87	T9	318
62.	I/O (D4)	39	61	64	61	88	R9	324
63.	I/O	-	62	65	62	89	P9	327
	VCC	40	63	66	63	90	R8	-
	GND	41	64	67	64	91	P8	-
64.	I/O (D3)	42	65	68	65	92	T8	336
65.	I/O ($\overline{RS}$)	43	66	69	66	93	T7	339
66.	I/O	-	-	70	67	94	T6	342
67.	I/O	-	-	-	-	95	R7	348
68.	I/O (D2)	44	67	71	68	96	P7	351
69.	I/O	-	68	72	69	97	T5	360
	GND	-	-	-	-	100	P6	-
70.	I/O (D1)	45	69	73	70	101	T3	363
71.	I/O ($\overline{RCLK\text{-}BUSY}$/RDY)	-	70	74	71	102	P5	366
72.	I/O (D0, DIN)	46	71	75	72	105	P4	372
73.	I/O (DOUT)	47	72	76	73	106	T2	375

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
57.	I/O		-	-	-	47	E16	53	306
58.	I/O		38	34	31	48	F16	54	312
59.	I/O		39	35	32	49	G14	55	315
60.	I/O		-	36	33	50	G15	56	318
61.	I/O		-	37	34	51	G16	57	324
62.	I/O		40	38	35	52	H16	58	327
63.	I/O ($\overline{ERR}$, $\overline{INIT}$)		41	39	36	53	H15	59	330
	VCC		42	40	37	54	H14	60	-
	GND		43	41	38	55	J14	61	-
64.	I/O		44	42	39	56	J15	62	336
65.	I/O		45	43	40	57	J16	63	339
66.	I/O		-	44	41	58	K16	64	348
67.	I/O		-	45	42	59	K15	65	351
68.	I/O		46	46	43	60	K14	66	354
69.	I/O		47	47	44	61	L16	67	360
70.	I/O		-	-	-	62	M16	68	363
71.	I/O		-	-	-	63	L15	69	366
	GND		-	-	-	64	L14	70	-
72.	I/O		-	-	-	-	N16	71	372
73.	I/O		-	-	-	-	M15	72	375
74.	I/O		48	48	45	65	P16	73	378
75.	I/O		49	49	46	66	M14	74	384
76.	I/O		-	-	-	67	N15	75	387
77.	I/O		-	-	-	68	P15	76	390
78.	I/O		50	50	47	69	N14	77	396
79.	I/O		51	51	48	70	R16	78	399
	GND		52	52	49	71	P14	79	-
	DONE		53	53	50	72	R15	80	-
	VCC		54	54	51	73	P13	81	-
	PROG		55	55	52	74	R14	82	-
80.	I/O (D7)		56	56	53	75	T16	83	408
81.	GCK3 (I/O)		57	57	54	76	T15	84	411
82.	I/O		-	-	-	77	R13	85	420
83.	I/O		-	-	-	78	P12	86	423
84.	I/O (D6)		58	58	55	79	T14	87	426
85.	I/O		-	59	56	80	T13	88	432
	GND		-	-	-	81	P11	91	-
86.	I/O		-	-	-	82	R11	92	435
87.	I/O		-	-	-	83	T11	93	438
88.	I/O (D5)		59	60	57	84	T10	94	444
89.	I/O ($\overline{CS0}$)		60	61	58	85	P10	95	447
90.	I/O		-	62	59	86	R10	96	450
91.	I/O		-	63	60	87	T9	97	456
92.	I/O (D4)		61	64	61	88	R9	98	459
93.	I/O		62	65	62	89	P9	99	462
	VCC		63	66	63	90	R8	100	-
	GND		64	67	64	91	P8	101	-
94.	I/O (D3)		65	68	65	92	T8	102	468
95.	I/O ($\overline{RS}$)		66	69	66	93	T7	103	471
96.	I/O		-	70	67	94	T6	104	474
97.	I/O		-	-	-	95	R7	105	480
98.	I/O (D2)		67	71	68	96	P7	106	483

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
137.	I/O	-	-	-	-	-	R11	K12	137	708
138.	I/O	-	82	92	100	120	U13	K13	138	711
139.	I/O	-	83	93	101	121	V13	K14	139	714
	VCC	-	-	-	-	-	-	VCC*	140	-
140.	I/O (D5)	59	84	94	102	122	U12	K15	141	720
141.	I/O ($\overline{CS0}$)	60	85	95	103	123	V12	J12	142	723
142.	I/O	-	-	-	104	124	T11	J13	144	726
143.	I/O	-	-	-	105	125	U11	J14	145	732
144.	I/O	-	86	96	106	126	V11	J15	146	735
145.	I/O	-	87	97	107	127	V10	J11	147	738
146.	I/O (D4)	61	88	98	108	128	U10	H13	148	744
147.	I/O	62	89	99	109	129	T10	H14	149	747
	VCC	63	90	100	110	130	R10	VCC*	150	-
	GND	64	91	101	111	131	R9	GND*	151	-
148.	I/O (D3)	65	92	102	112	132	T9	H12	152	756
149.	I/O ($\overline{RS}$)	66	93	103	113	133	U9	H11	153	759
150.	I/O	-	94	104	114	134	V9	G14	154	768
151.	I/O	-	95	105	115	135	V8	G15	155	771
152.	I/O	-	-	-	116	136	U8	G13	156	780
153.	I/O	-	-	-	117	137	T8	G12	157	783
154.	I/O (D2)	67	96	106	118	138	V7	G11	159	786
155.	I/O	68	97	107	119	139	U7	F15	160	792
	VCC	-	-	-	-	-	-	VCC*	161	-
156.	I/O	-	98	108	120	140	V6	F14	162	795
157.	I/O	-	99	109	121	141	U6	F13	163	798
158.	I/O	-	-	-	-	-	R8	G10	164	804
159.	I/O	-	-	-	-	-	R7	E15	165	807
	GND	-	100	110	122	142	T7	GND*	166	-
160.	I/O	-	-	-	-	-	R6	E14	167	810
161.	I/O	-	-	-	-	-	R5	F12	168	816
162.	I/O	-	-	-	-	143	V5	E13	169	819
163.	I/O	-	-	-	-	144	V4	D15	170	822
164.	I/O	-	-	111	123	145	U5	F11	171	828
165.	I/O	-	-	112	124	146	T6	D14	172	831
166.	I/O (D1)	69	101	113	125	147	V3	E12	173	834
167.	I/O ($\overline{RCLK}$-$\overline{BUSY}$/RDY)	70	102	114	126	148	V2	C15	174	840
168.	I/O	-	103	115	127	149	U4	D13	175	843
169.	I/O	-	104	116	128	150	T5	C14	176	846
170.	I/O (D0, DIN)	71	105	117	129	151	U3	F10	177	855
171.	I/O (DOUT)	72	106	118	130	152	T4	B15	178	858
	CCLK	73	107	119	131	153	V1	C13	179	-
	VCC	74	108	120	132	154	R4	VCC*	180	-
172.	I/O (TDO)	75	109	121	133	159	U2	A15	181	-
	GND	76	110	122	134	160	R3	GND*	182	-
173.	I/O (A0, $\overline{WS}$)	77	111	123	135	161	T3	A14	183	9
174.	GCK4 (A1, I/O)	78	112	124	136	162	U1	B13	184	15
175.	I/O	-	113	125	137	163	P3	E11	185	18
176.	I/O	-	114	126	138	164	R2	C12	186	21
177.	I/O (CS1, A2)	79	115	127	139	165	T2	A13	187	27
178.	I/O (A3)	80	116	128	140	166	N3	B12	188	30
179.	I/O	-	-	-	-	-	P4	F9	189	33

Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
8.	I/O (A11)	148	191	221	J3	B6	B16	165
9.	I/O	-	-	-	H2	-	C17	171
10.	I/O	-	-	-	G1	-	B18	174
	VCC	-	-	222	E1	VCC*	VCC*	-
11.	I/O	-	-	223	H3	C6	C18	177
12.	I/O	-	-	224	G2	F7	D17	183
13.	I/O	149	192	225	H4	A5	A20	186
14.	I/O	150	193	226	F2	B5	B19	189
	GND	151	194	227	F1	GND*	GND*	-
15.	I/O	-	-	-	H5	-	C19	195
16.	I/O	-	-	-	G3	-	D18	198
17.	I/O	-	195	228	D1	D6	A21	201
18.	I/O	-	196	229	G4	C5	B20	207
19.	I/O	152	197	230	E2	A4	C20	210
20.	I/O	153	198	231	F3	E6	B21	213
21.	I/O (A12)	154	199	232	G5	B4	B22	219
22.	I/O (A13)	155	200	233	C1	D5	C21	222
23.	I/O	-	-	-	F4	-	D20	225
24.	I/O	-	-	-	E3	-	A23	234
25.	I/O	-	-	234	D2	A3	D21	237
26.	I/O	-	-	235	C2	C4	C22	243
27.	I/O	156	201	236	F5	B3	B24	246
28.	I/O	157	202	237	E4	F6	C23	249
29.	I/O (A14)	158	203	238	D3	A2	D22	258
30.	I/O (A15)	159	204	239	C3	C3	C24	261
	VCC	160	205	240	A2	VCC*	VCC*	-
	GND	1	2	1	B1	GND*	GND*	-
31.	GCK1 (A16, I/O)	2	4	2	D4	D4	D23	270
32.	I/O (A17)	3	5	3	B2	B1	C25	273
33.	I/O	4	6	4	B3	C2	D24	279
34.	I/O	5	7	5	E6	E5	E23	282
35.	I/O (TDI)	6	8	6	D5	D3	C26	285
36.	I/O (TCK)	7	9	7	C4	C1	E24	294
37.	I/O	-	-	-	A3	-	F24	297
38.	I/O	-	-	-	D6	-	E25	303
39.	I/O	8	10	8	E7	D2	D26	306
40.	I/O	9	11	9	B4	G6	G24	309
41.	I/O	-	12	10	C5	E4	F25	315
42.	I/O	-	13	11	A4	D1	F26	318
43.	I/O	-	-	12	D7	E3	H23	321
44.	I/O	-	-	13	C6	E2	H24	327
45.	I/O	-	-	-	E8	-	G25	330
46.	I/O	-	-	-	B5	-	G26	333
	GND	10	14	14	A5	GND*	GND*	-
47.	I/O	11	15	15	B6	F5	J23	339
48.	I/O	12	16	16	D8	E1	J24	342
49.	I/O (TMS)	13	17	17	C7	F4	H25	345
50.	I/O	14	18	18	B7	F3	K23	351
	VCC	-	-	19	A6	VCC*	VCC*	-
51.	I/O	-	-	20	C8	F2	L24	354
52.	I/O	-	-	21	E9	F1	K25	357
53.	I/O	-	-	-	B8	-	L25	363

Product Availability

	PINS	64	84	100	100	144	156	160	176	191	208	208	223	225	240	240	299	352
	TYPE	Plast. VQFP	Plast. PLCC	Plast. PQFP	Plast. VQFP	Plast. TQFP	Ceram. PGA	Plast. PQFP	Plast. TQFP	Ceram. PGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	Plast. BGA	High-Perf. QFP	Plast. PQFP	Ceram. PGA	Plast. BGA
	CODE	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	PQ160	TQ176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	BG352
XC5202	-6	CI	CI	CI	CI	CI	CI											
	-5	CI	CI	CI	CI	CI	CI											
	-4	C	C	C	C	C	C											
	-3	C	C	C	C	C	C											
XC5204	-6		CI	CI	CI	CI	CI	CI										
	-5		CI	CI	CI	CI	CI	CI										
	-4		C	C	C	C	C	C										
	-3		C	C	C	C	C	C										
XC5206	-6		CI	CI	CI	CI		CI	CI	CI		CI						
	-5		CI	CI	CI	CI		CI	CI	CI		CI						
	-4		C	C	C	C		C	C	C		C						
	-3		C	C	C	C		C	C	C		C						
XC5210	-6		CI			CI		CI	CI			CI	CI	CI		CI		
	-5		CI			CI		CI	CI			CI	CI	CI		CI		
	-4		C			C		C	C			C	C	C		C		
	-3		C			C		C	C			C	C	C		C		
XC5215	-6							CI			CI			CI	CI		CI	CI
	-5							C			C			C	C		C	C
	-4							C			C			C	C		C	C
	-3							C			C			C	C		C	C

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C = Commercial T_J = 0° to +85°C

I= Industrial T_J = -40°C to +100°C

* VQ64 package supports Master Serial, Slave Serial, and Express configuration modes only.

User I/O Per Package

Device	Max I/O	Package Type																
		VQ64	PC84	PQ100	VQ100	TQ144	PG156	PQ160	TQ176	PG191	HQ208	PQ208	PG223	BG225	HQ240	PQ240	PG299	BG352
XC5202	84	52	65	81	81	84	84											
XC5204	124		65	81	81	117	124	124										
XC5206	148		65	81	81	117		133	148	148		148						
XC5210	196		65			117		133	149			164	196	196		196		
XC5215	244							133			164			196	197		244	244

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Ordering Information