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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	324
Number of Logic Elements/Cells	1296
Total RAM Bits	-
Number of I/O	133
Number of Gates	16000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	160-BQFP
Supplier Device Package	160-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc5210-4pq160c

XC3000 family: XC5200 devices support an additional programming mode: Peripheral Synchronous.

XC3000 family: The XC5200 family does not support Power-down, but offers a Global 3-state input that does not reset any flip-flops.

XC3000 family: The XC5200 family does not provide an on-chip crystal oscillator amplifier, but it does provide an internal oscillator from which a variety of frequencies up to 12 MHz are available.

Architectural Overview

Figure 1 presents a simplified, conceptual overview of the XC5200 architecture. Similar to conventional FPGAs, the XC5200 family consists of programmable IOBs, programmable logic blocks, and programmable interconnect. Unlike other FPGAs, however, the logic and local routing resources of the XC5200 family are combined in flexible VersaBlocks (Figure 2). General-purpose routing connects to the VersaBlock through the General Routing Matrix (GRM).

VersaBlock: Abundant Local Routing Plus Versatile Logic

The basic logic element in each VersaBlock structure is the Logic Cell, shown in Figure 3. Each LC contains a 4-input function generator (F), a storage device (FD), and control logic. There are five independent inputs and three outputs to each LC. The independence of the inputs and outputs allows the software to maximize the resource utilization within each LC. Each Logic Cell also contains a direct feedthrough path that does not sacrifice the use of either the function generator or the register; this feature is a first for FPGAs. The storage device is configurable as either a D flip-flop or a latch. The control logic consists of carry logic for fast implementation of arithmetic functions, which can also be configured as a cascade chain allowing decode of very wide input functions.

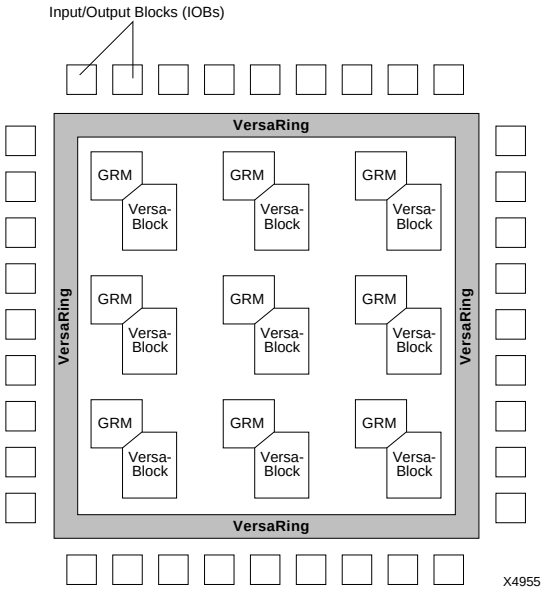


Figure 1: XC5200 Architectural Overview

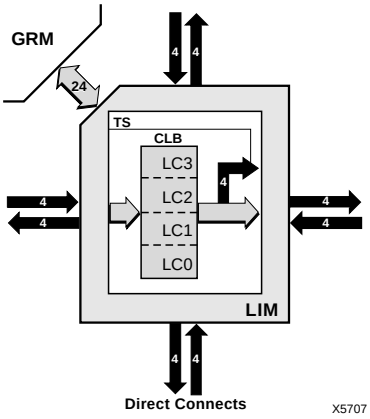


Figure 2: VersaBlock

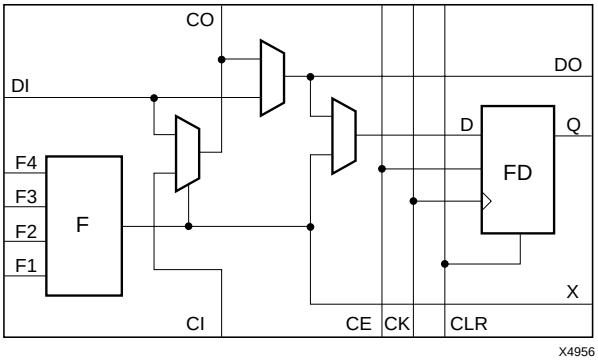


Figure 3: XC5200 Logic Cell (Four LCs per CLB)

single-length lines, double-length lines, and Longlines all routed through the GRM. The direct connects, LIM, and logic-cell feedthrough are contained within each Versa-Block. Throughout the XC5200 interconnect, an efficient multiplexing scheme, in combination with three layer metal (TLM), was used to improve the overall efficiency of silicon usage.

Performance Overview

The XC5200 family has been benchmarked with many designs running synchronous clock rates beyond 66 MHz. The performance of any design depends on the circuit to be implemented, and the delay through the combinatorial and sequential logic elements, plus the delay in the interconnect routing. A rough estimate of timing can be made by assuming 3-6 ns per logic level, which includes direct-connect routing delays, depending on speed grade. More accurate estimations can be made using the information in the Switching Characteristic Guideline section.

Taking Advantage of Reconfiguration

FPGA devices can be reconfigured to change logic function while resident in the system. This capability gives the system designer a new degree of freedom not available with any other type of logic.

Hardware can be changed as easily as software. Design updates or modifications are easy, and can be made to products already in the field. An FPGA can even be reconfigured dynamically to perform different functions at different times.

Reconfigurable logic can be used to implement system self-diagnostics, create systems capable of being reconfigured for different environments or operations, or implement multi-purpose hardware for a given application. As an added benefit, using reconfigurable FPGA devices simplifies hardware design and debugging and shortens product time-to-market.

Detailed Functional Description

Configurable Logic Blocks (CLBs)

Figure 4 shows the logic in the XC5200 CLB, which consists of four Logic Cells (LC[3:0]). Each Logic Cell consists of an independent 4-input Lookup Table (LUT), and a D-Type flip-flop or latch with common clock, clock enable, and clear, but individually selectable clock polarity. Additional logic features provided in the CLB are:

- An independent 5-input LUT by combining two 4-input LUTs.
- High-speed carry propagate logic.
- High-speed pattern decoding.
- High-speed direct connection to flip-flop D-inputs.
- Individual selection of either a transparent, level-sensitive latch or a D flip-flop.
- Four 3-state buffers with a shared Output Enable.

5-Input Functions

Figure 5 illustrates how the outputs from the LUTs from LC0 and LC1 can be combined with a 2:1 multiplexer (F5_MUX) to provide a 5-input function. The outputs from the LUTs of LC2 and LC3 can be similarly combined.

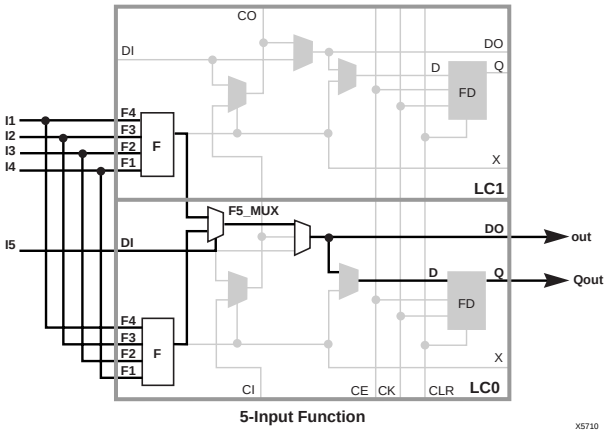


Figure 5: Two LUTs in Parallel Combined to Create a 5-input Function

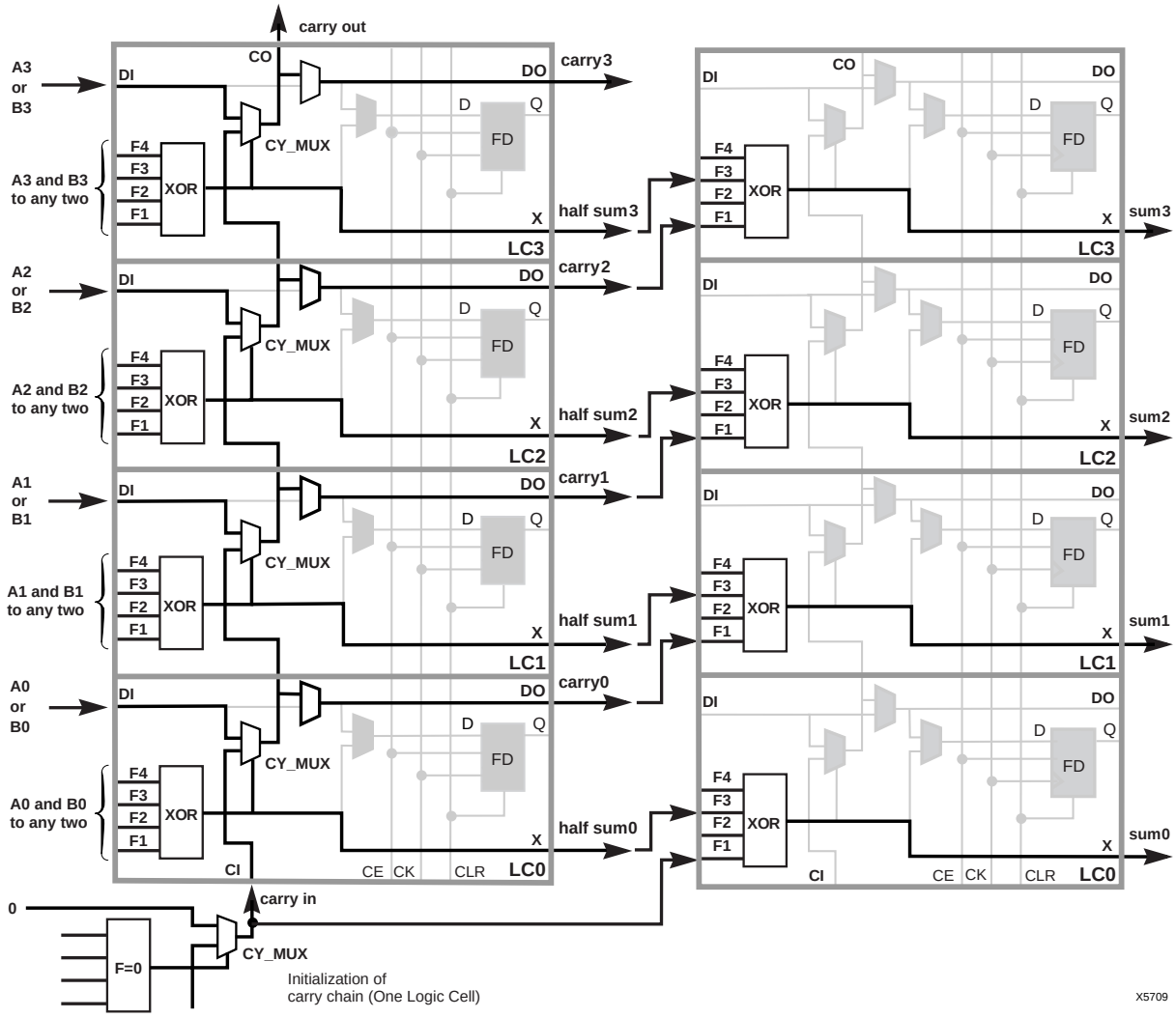


Figure 6: XC5200 CY_MUX Used for Adder Carry Propagate

Carry Function

The XC5200 family supports a carry-logic feature that enhances the performance of arithmetic functions such as counters, adders, etc. A carry multiplexer (CY_MUX) symbol is used to indicate the XC5200 carry logic. This symbol represents the dedicated 2:1 multiplexer in each LC that performs the one-bit high-speed carry propagate per logic cell (four bits per CLB).

While the carry propagate is performed inside the LC, an adjacent LC must be used to complete the arithmetic function. Figure 6 represents an example of an adder function. The carry propagate is performed on the CLB shown, which also generates the half-sum for the four-bit adder. An adjacent CLB is responsible for XORing the half-sum with the corresponding carry-out. Thus an adder or counter requires two LCs per bit. Notice that the carry chain requires an initialization stage, which the XC5200 family accomplishes using the carry initialize (CY_INIT) macro and one additional LC. The carry chain can propagate vertically up a column of CLBs.

The XC5200 library contains a set of Relationally-Placed Macros (RPMs) and arithmetic functions designed to take advantage of the dedicated carry logic. Using and modifying these macros makes it much easier to implement cus-

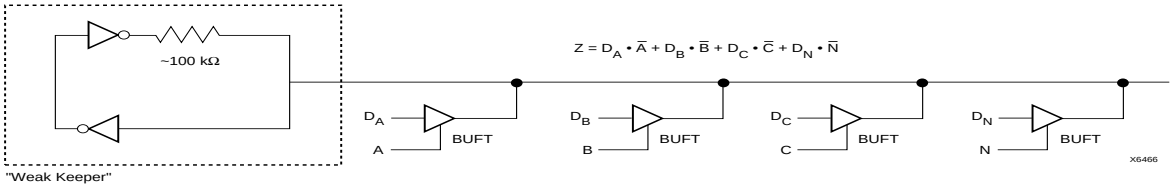


Figure 10: 3-State Buffers Implement a Multiplexer

Input/Output Blocks

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals.

The I/O block, shown in Figure 11, consists of an input buffer and an output buffer. The output driver is an 8-mA full-rail CMOS buffer with 3-state control. Two slew-rate control modes are supported to minimize bus transients. Both the output buffer and the 3-state control are invertible. The input buffer has globally selected CMOS or TTL input thresholds. The input buffer is invertible and also provides a programmable delay line to assure reliable chip-to-chip set-up and hold times. Minimum ESD protection is 3 KV using the Human Body Model.

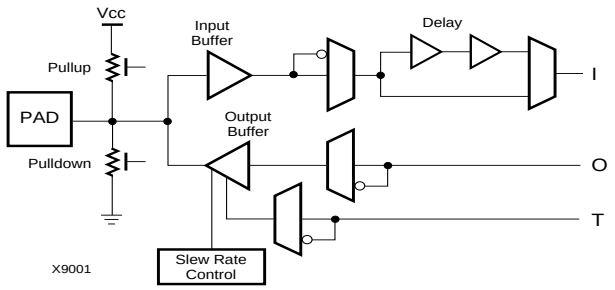


Figure 11: XC5200 I/O Block

IOB Input Signals

The XC5200 inputs can be globally configured for either TTL (1.2V) or CMOS thresholds, using an option in the bitstream generation software. There is a slight hysteresis of about 300mV.

The inputs of XC5200-Series 5-Volt devices can be driven by the outputs of any 3.3-Volt device, if the 5-Volt inputs are in TTL mode.

Supported sources for XC5200-Series device inputs are shown in Table 5.

Table 5: Supported Sources for XC5200-Series Device Inputs

Source	XC5200 Input Mode	
	5 V, TTL	5 V, CMOS
Any device, Vcc = 3.3 V, CMOS outputs	√	**Unreliable Data**
Any device, Vcc = 5 V, TTL outputs	√	
Any device, Vcc = 5 V, CMOS outputs	√	√

Optional Delay Guarantees Zero Hold Time

XC5200 devices do not have storage elements in the IOBs. However, XC5200 IOBs can be efficiently routed to CLB flip-flops or latches to store the I/O signals.

The data input to the register can optionally be delayed by several nanoseconds. With the delay enabled, the setup time of the input flip-flop is increased so that normal clock routing does not result in a positive hold-time requirement. A positive hold time requirement can lead to unreliable, temperature- or processing-dependent operation.

The input flip-flop setup time is defined between the data measured at the device I/O pin and the clock input at the CLB (not at the clock pin). Any routing delay from the device clock pin to the clock input of the CLB must, therefore, be subtracted from this setup time to arrive at the real setup time requirement relative to the device pins. A short specified setup time might, therefore, result in a negative setup time at the device pins, i.e., a positive hold-time requirement.

When a delay is inserted on the data line, more clock delay can be tolerated without causing a positive hold-time requirement. Sufficient delay eliminates the possibility of a data hold-time requirement at the external pin. The maximum delay is therefore inserted as the software default.

The XC5200 IOB has a one-tap delay element: either the delay is inserted (default), or it is not. The delay guarantees a zero hold time with respect to clocks routed through any of the XC5200 global clock buffers. (See "Global Lines" on page 96 for a description of the global clock buffers in the XC5200.) For a shorter input register setup time, with

VersaRing Input/Output Interface

The VersaRing, shown in Figure 18, is positioned between the core logic and the pad ring; it has all the routing resources of a VersaBlock without the CLB logic. The VersaRing decouples the core logic from the I/O pads. Each VersaRing Cell provides up to four pad-cell connections on one side, and connects directly to the CLB ports on the other side.

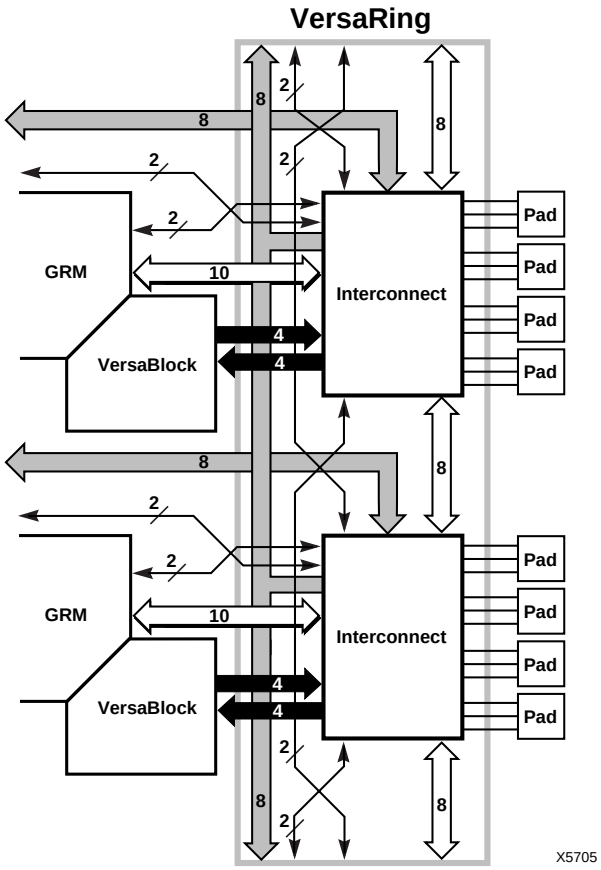


Figure 18: VersaRing I/O Interface

Boundary Scan

The “bed of nails” has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE boundary scan standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can imbed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan-compatible IC. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

XC5200 devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP can also support two USERCODE instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output.

Boundary-scan operation is independent of individual IOB configuration and package type. All IOBs are treated as independently controlled bidirectional pins, including any unbonded IOBs. Retaining the bidirectional test capability after configuration provides flexibility for interconnect testing.

Also, internal signals can be captured during EXTEST by connecting them to unbonded IOBs, or to the unused outputs in IOBs used as unidirectional input pins. This technique partially compensates for the lack of INTEST support.

The user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in Xilinx devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note XAPP 017: *“Boundary Scan in XC4000 and XC5200 Series devices”*

Figure 19 on page 99 is a diagram of the XC5200-Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

The public boundary-scan instructions are always available prior to configuration. After configuration, the public instructions and any USERCODE instructions are only available if specified in the design. While SAMPLE and BYPASS are available during configuration, it is recommended that boundary-scan operations not be performed during this transitory period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA device, and to read back the configuration data.

All of the XC4000 boundary-scan modes are supported in the XC5200 family. Three additional outputs for the User-Register are provided (Reset, Update, and Shift), repre-

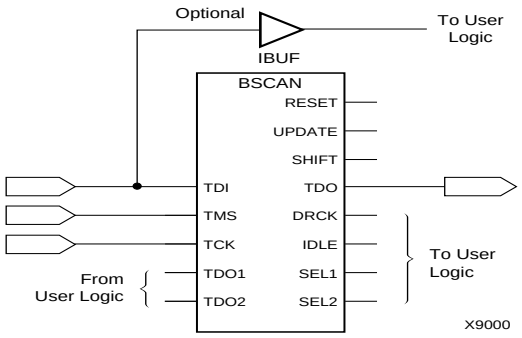


Figure 20: Boundary Scan Schematic Example

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note XAPP 017, "*Boundary Scan in XC4000 and XC5200 Devices*."

Power Distribution

Power for the FPGA is distributed through a grid to achieve high noise immunity and isolation between logic and I/O. Inside the FPGA, a dedicated Vcc and Ground ring surrounding the logic array provides power to the I/O drivers, as shown in Figure 21. An independent matrix of Vcc and Ground lines supplies the interior logic of the device.

This power distribution grid provides a stable supply and ground for all internal logic, providing the external package power pins are all connected and appropriately decoupled. Typically, a 0.1 µF capacitor connected near the Vcc and Ground pins of the package will provide adequate decoupling.

Output buffers capable of driving/sinking the specified 8 mA loads under specified worst-case conditions may be capable of driving/sinking up to 10 times as much current under best case conditions.

Noise can be reduced by minimizing external load capacitance and reducing simultaneous output transitions in the same direction. It may also be beneficial to locate heavily loaded output buffers near the Ground pads. The I/O Block output buffers have a slew-rate limited mode (default) which should be used where output rise and fall times are not speed-critical.

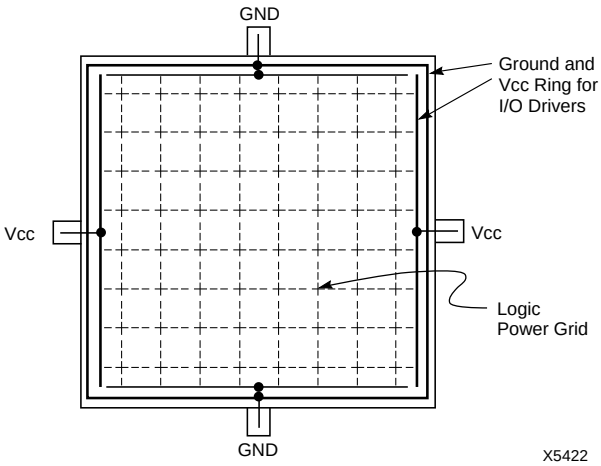


Figure 21: XC5200-Series Power Distribution

Pin Descriptions

There are three types of pins in the XC5200-Series devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated and pulled high with a 20 kΩ - 100 kΩ pull-up resistor.

After configuration, if an IOB is unused it is configured as an input with a 20 kΩ - 100 kΩ pull-up resistor.

Device pins for XC5200-Series devices are described in Table 9. Pin functions during configuration for each of the seven configuration modes are summarized in "Pin Func-

Table 9: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor (20 kΩ - 100 kΩ) that defines the logic level as High.

Configuration

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. XC5200-Series devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Special Purpose Pins

Three configuration mode pins (M2, M1, M0) are sampled prior to configuration to determine the configuration mode. After configuration, these pins can be used as auxiliary I/O connections. The development system does not use these resources unless they are explicitly specified in the design entry. This is done by placing a special pad symbol called MD2, MD1, or MD0 instead of the input or output pad symbol.

In XC5200-Series devices, the mode pins have weak pull-up resistors during configuration. With all three mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the mode pins can be left unconnected. (Note, however, that the internal pull-up resistor value can be as high as 100 kΩ.) After configuration, these pins can individually have weak pull-up or pull-down resistors, as specified in the design. A pull-down resistor value of 3.3kΩ is recommended.

These pins are located in the lower left chip corner and are near the readback nets. This location allows convenient routing if compatibility with the XC2000 and XC3000 family conventions of M0/RT, M1/RD is desired.

Configuration Modes

XC5200 devices have seven configuration modes. These modes are selected by a 3-bit input code applied to the M2, M1, and M0 inputs. There are three self-loading Master modes, two Peripheral modes, and a Serial Slave mode,

Table 10: Configuration Modes

Mode	M2	M1	M0	CCLK	Data
Master Serial	0	0	0	output	Bit-Serial
Slave Serial	1	1	1	input	Bit-Serial
Master Parallel Up	1	0	0	output	Byte-Wide, increment from 00000
Master Parallel Down	1	1	0	output	Byte-Wide, decrement from 3FFFF
Peripheral Synchronous*	0	1	1	input	Byte-Wide
Peripheral Asynchronous	1	0	1	output	Byte-Wide
Express	0	1	0	input	Byte-Wide
Reserved	0	0	1	—	—

Note :*Peripheral Synchronous can be considered byte-wide Slave Parallel

which is used primarily for daisy-chained devices. The seventh mode, called Express mode, is an additional slave mode that allows high-speed parallel configuration. The coding for mode selection is shown in Table 10.

Note that the smallest package, VQ64, only supports the Master Serial, Slave Serial, and Express modes.A detailed description of each configuration mode, with timing information, is included later in this data sheet. During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 13 on page 124.

Master Modes

The three Master modes use an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices. They also generate address and timing for external PROM(s) containing the configuration data.

Master Parallel (Up or Down) modes generate the CCLK signal and PROM addresses and receive byte parallel data. The data is internally serialized into the FPGA data-frame format. The up and down selection generates starting addresses at either zero or 3FFFF, for compatibility with different microprocessor addressing conventions. The

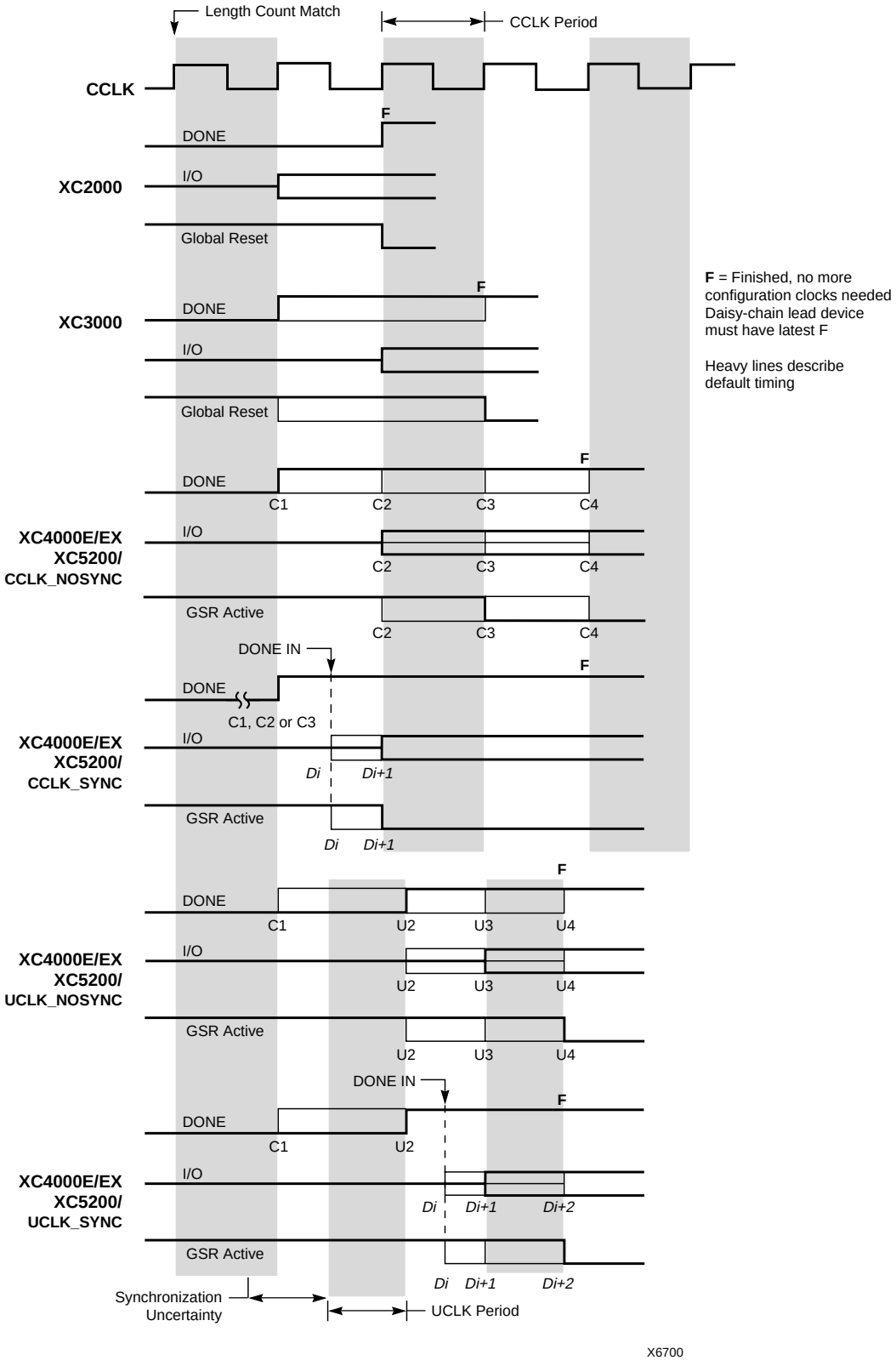


Figure 25: Start-up Timing

DONE High to active user I/O is controlled by an option to the bitstream generation software.

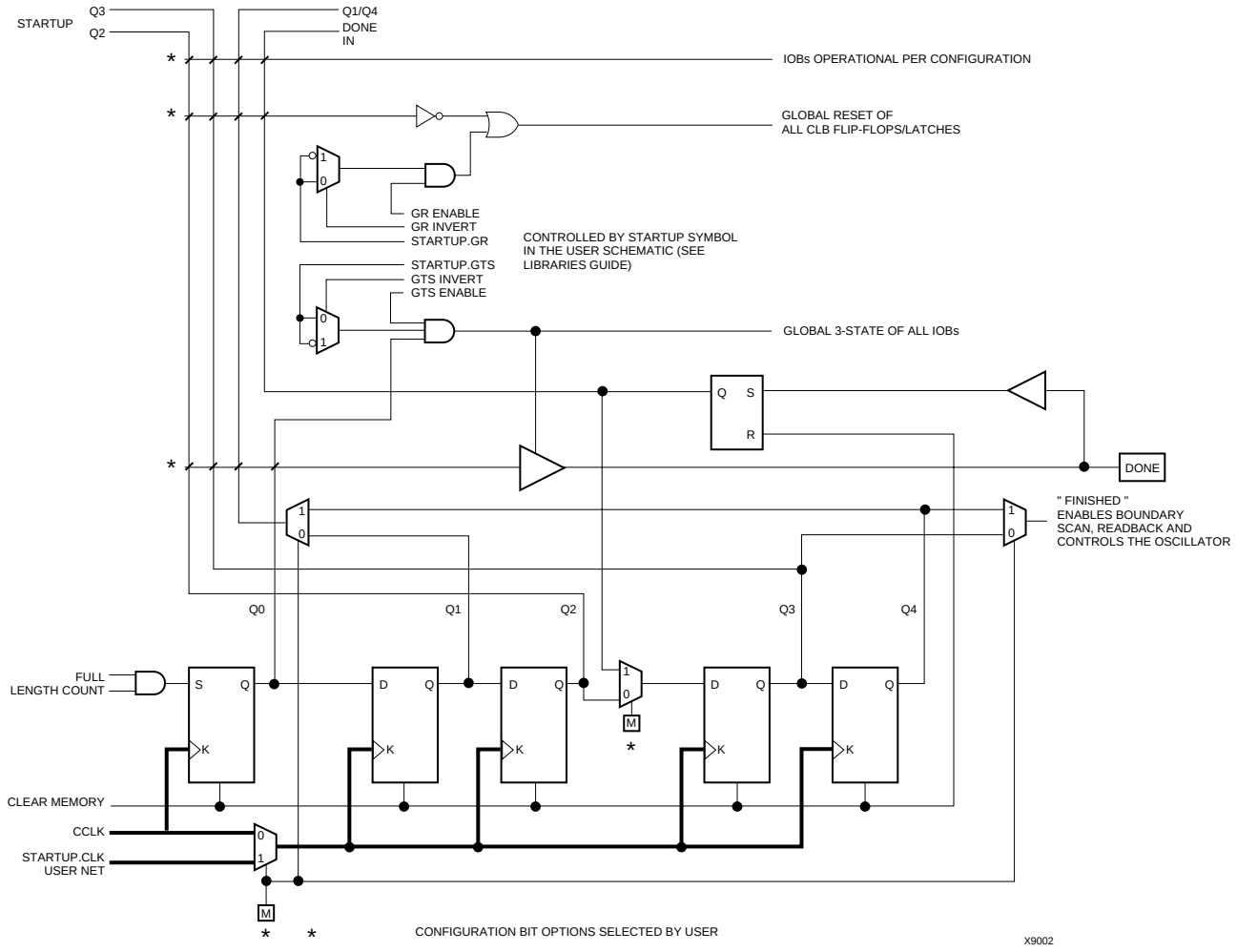


Figure 26: Start-up Logic

Release of Global Reset After DONE Goes High

By default, Global Reset (GR) is released two CCLK cycles after the DONE pin goes High. If CCLK is not clocked twice after DONE goes High, all flip-flops are held in their initial reset state. The delay from DONE High to GR inactive is controlled by an option to the bitstream generation software.

Configuration Complete After DONE Goes High

Three full CCLK cycles are required after the DONE pin goes High, as shown in Figure 25 on page 109. If CCLK is not clocked three times after DONE goes High, readback cannot be initiated and most boundary scan instructions cannot be used.

Configuration Through the Boundary Scan Pins

XC5200-Series devices can be configured through the boundary scan pins.

For detailed information, refer to the Xilinx application note XAPP017, "*Boundary Scan in XC4000 and XC5200 Devices*."

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs.

Configuration Timing

The seven configuration modes are discussed in detail in this section. Timing specifications are included.

Slave Serial Mode

In Slave Serial mode, an external signal drives the CCLK input of the FPGA. The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin.

There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 28 shows a full master/slave system. An XC5200-Series device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial mode is selected by a <111> on the mode pins (M2, M1, M0). Slave Serial is the default mode if the mode pins are left unconnected, as they have weak pull-up resistors during configuration.

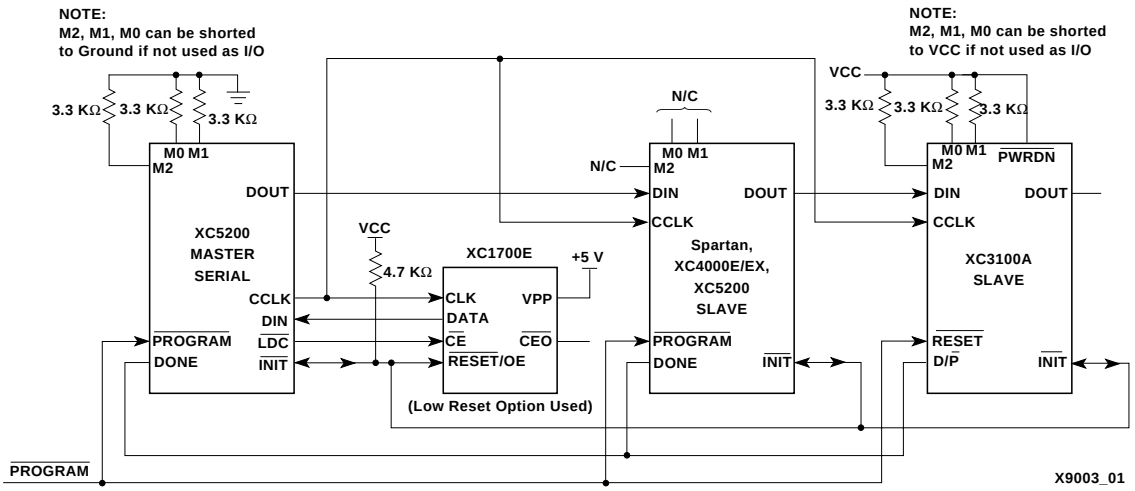
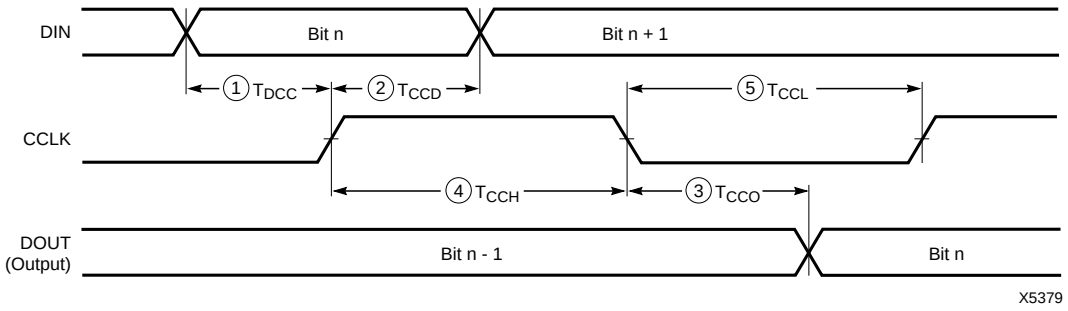


Figure 28: Master/Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 29: Slave Serial Mode Programming Switching Characteristics

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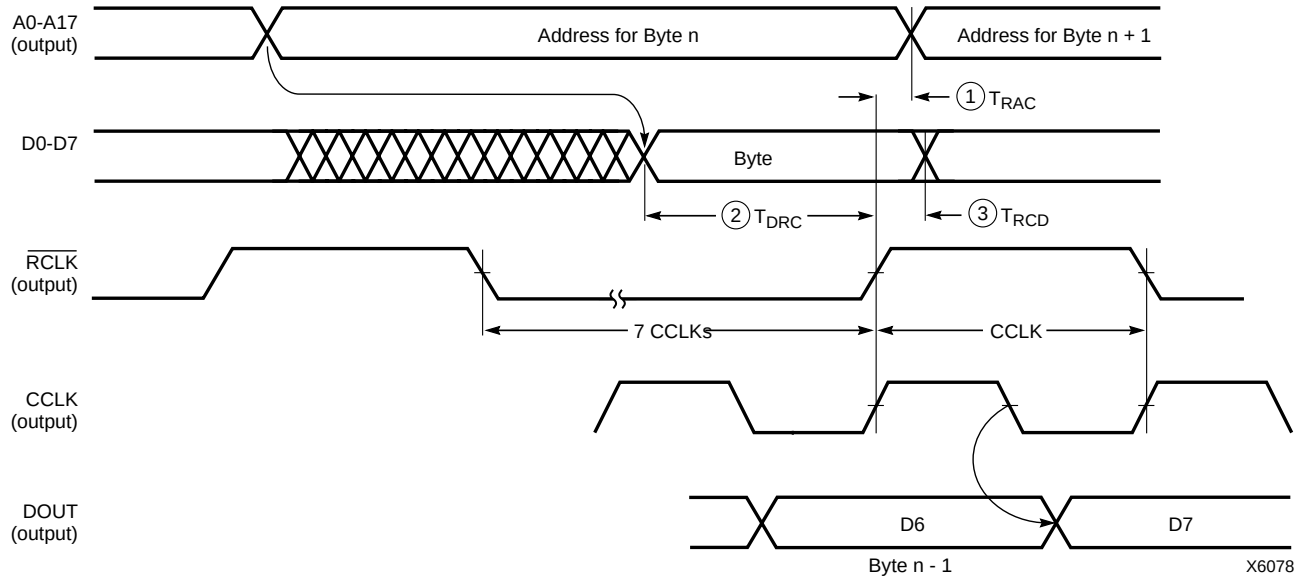


	Description	Symbol		Min	Max	Units
CCLK	Delay to Address valid	1	T_{RAC}	0	200	ns
	Data setup time	2	T_{DRC}	60		ns
	Data hold time	3	T_{RCD}	0		ns

Note: 1. At power-up, V_{CC} must rise from 2.0 V to V_{CC} min in less then 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is Valid.
2. The first Data byte is loaded and CCLK starts at the end of the first $\overline{\text{RCLK}}$ active cycle (rising edge).

This timing diagram shows that the EPROM requirements are extremely relaxed. EPROM access time can be longer than 500 ns. EPROM data output has no hold-time requirements.

Figure 32: Master Parallel Mode Programming Switching Characteristics

Synchronous Peripheral Mode

Synchronous Peripheral mode can also be considered Slave Parallel mode. An external signal drives the CCLK input(s) of the FPGA(s). The first byte of parallel configuration data must be available at the Data inputs of the lead FPGA a short setup time before the rising CCLK edge. Subsequent data bytes are clocked in on every eighth consecutive rising CCLK edge.

The same CCLK edge that accepts data, also causes the RDY/BUSY output to go High for one CCLK period. The pin name is a misnomer. In Synchronous Peripheral mode it is really an ACKNOWLEDGE signal. Synchronous operation does not require this response, but it is a meaningful signal for test purposes. Note that RDY/BUSY is pulled High with a high-impedance pullup prior to INIT going High.

The lead FPGA serializes the data and presents the preamble data (and all data that overflows the lead device) on its DOUT pin. There is an internal delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

In order to complete the serial shift operation, 10 additional CCLK rising edges are required after the last data byte has been loaded, plus one more CCLK cycle for each daisy-chained device.

Synchronous Peripheral mode is selected by a <011> on the mode pins (M2, M1, M0).

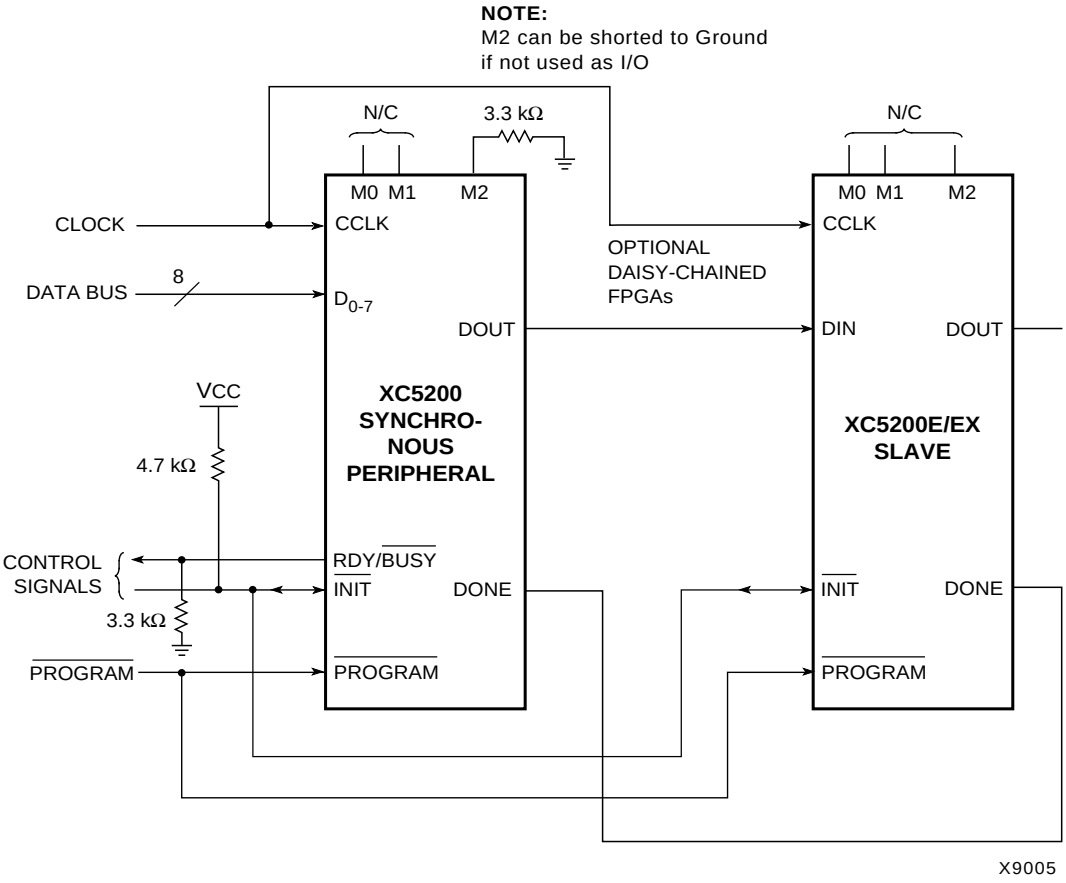
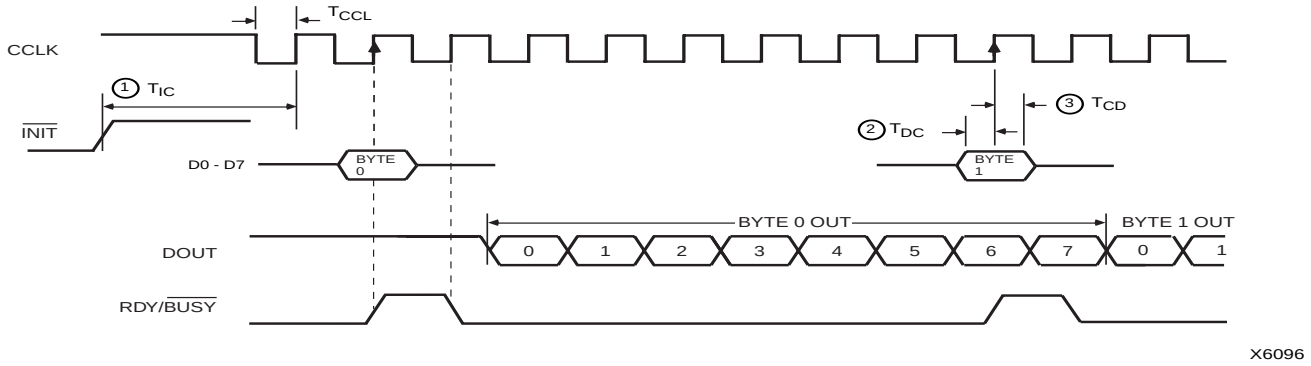


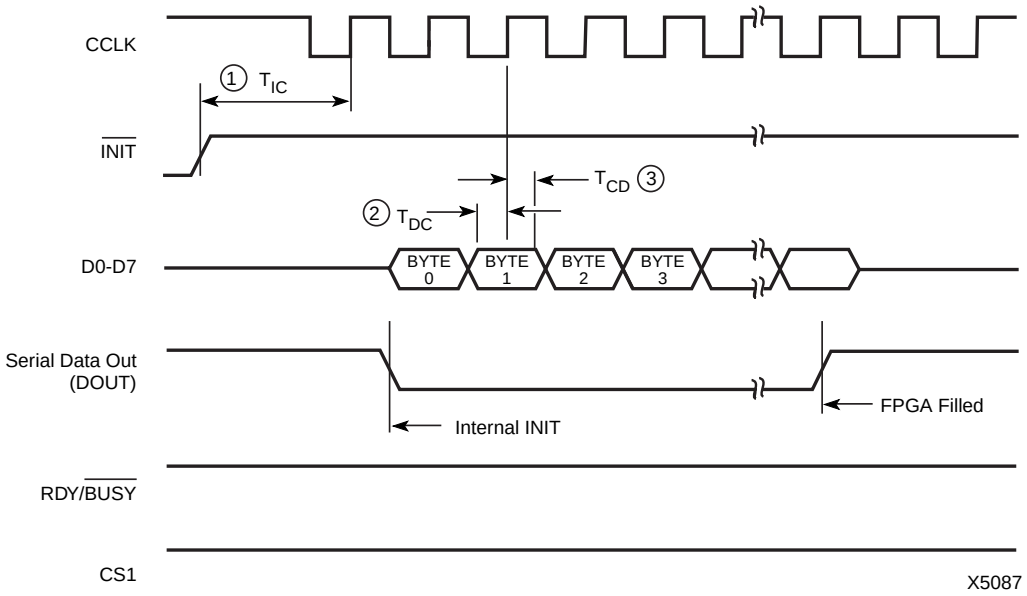
Figure 33: Synchronous Peripheral Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	INIT (High) setup time	1	T_{IC}	5		µs
	D0 - D7 setup time	2	T_{DC}	60		ns
	D0 - D7 hold time	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	50		ns
	CCLK Low time		T_{CCL}	60		ns
	CCLK Frequency		F_{CC}		8	MHz

Notes: 1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes high. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
2. The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
3. The pin name RDY/BUSY is a misnomer. In synchronous peripheral mode this is really an ACKNOWLEDGE signal.
4.Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 34: Synchronous Peripheral Mode Programming Switching Characteristics



	Description	Symbol		Min	Max	Units
CCLK	INIT (High) Setup time required	1	T_{IC}	5		µs
	DIN Setup time required	2	T_{DC}	30		ns
	DIN hold time required	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	30		ns
	CCLK Low time		T_{CCL}	30		ns
	CCLK frequency		F_{CC}		10	MHz

Note: If not driven by the preceding DOUT, CS1 must remain high until the device is fully configured.

Figure 38: Express Mode Programming Switching Characteristics

XC5200 Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC5200 Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial: 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial: -40°C to 100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

XC5200 DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -8.0 mA, V_{CC} min	3.86		V
V_{OL}	Low-level output voltage @ I_{OL} = 8.0 mA, V_{CC} max		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 1)		15	mA
I_{IL}	Leakage current	-10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.30	mA

Note: 1. With no output current loads, all package pins at Vcc or GND, either TTL or CMOS inputs, and the FPGA configured with a tie option.

XC5200 Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature in plastic packages	+125	°C
	Junction temperature in ceramic packages	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Device-Specific Pinout Tables

Device-specific tables include all packages for each XC5200-Series device. They follow the pad locations around the die, and include boundary scan register locations.

Pin Locations for XC5202 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	VCC	-	2	92	89	128	H3	-
1.	I/O (A8)	57	3	93	90	129	H1	51
2.	I/O (A9)	58	4	94	91	130	G1	54
3.	I/O	-	-	95	92	131	G2	57
4.	I/O	-	-	96	93	132	G3	63
5.	I/O (A10)	-	5	97	94	133	F1	66
6.	I/O (A11)	59	6	98	95	134	F2	69
	GND	-	-	-	-	137	F3	-
7.	I/O (A12)	60	7	99	96	138	E3	78
8.	I/O (A13)	61	8	100	97	139	C1	81
9.	I/O (A14)	62	9	1	98	142	B1	90
10.	I/O (A15)	63	10	2	99	143	B2	93
	VCC	64	11	3	100	144	C3	-
	GND	-	12	4	1	1	C4	-
11.	GCK1 (A16, I/O)	1	13	5	2	2	B3	102
12.	I/O (A17)	2	14	6	3	3	A1	105
13.	I/O (TDI)	3	15	7	4	6	B4	111
14.	I/O (TCK)	4	16	8	5	7	A3	114
	GND	-	-	-	-	8	C6	-
15.	I/O (TMS)	5	17	9	6	11	A5	117
16.	I/O	6	18	10	7	12	C7	123
17.	I/O	-	-	-	-	13	B7	126
18.	I/O	-	-	11	8	14	A6	129
19.	I/O	-	19	12	9	15	A7	135
20.	I/O	7	20	13	10	16	A8	138
	GND	8	21	14	11	17	C8	-
	VCC	9	22	15	12	18	B8	-
21.	I/O	-	23	16	13	19	C9	141
22.	I/O	10	24	17	14	20	B9	147
23.	I/O		-	18	15	21	A9	150
24.	I/O		-	-	-	22	B10	153
25.	I/O	-	25	19	16	23	C10	159
26.	I/O	11	26	20	17	24	A10	162
	GND		-	-	-	27	C11	-
27.	I/O	12	27	21	18	28	B12	165
28.	I/O		-	22	19	29	A13	171
29.	I/O	13	28	23	20	32	B13	174
30.	I/O	14	29	24	21	33	B14	177
31.	M1 (I/O)	15	30	25	22	34	A15	186
	GND	-	31	26	23	35	C13	-
32.	M0 (I/O)	16	32	27	24	36	A16	189
	VCC	-	33	28	25	37	C14	-
33.	M2 (I/O)	17	34	29	26	38	B15	192
34.	GCK2 (I/O)	18	35	30	27	39	B16	195

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
14.	I/O		-	-	-	141	D3	157	129
15.	I/O (A14)		9	1	98	142	B1	158	138
16.	I/O (A15)		10	2	99	143	B2	159	141
	VCC		11	3	100	144	C3	160	-
	GND		12	4	1	1	C4	1	-
17.	GCK1 (A16, I/O)		13	5	2	2	B3	2	150
18.	I/O (A17)		14	6	3	3	A1	3	153
19.	I/O		-	-	-	4	A2	4	159
20.	I/O		-	-	-	5	C5	5	162
21.	I/O (TDI)		15	7	4	6	B4	6	165
22.	I/O (TCK)		16	8	5	7	A3	7	171
	GND		-	-	-	8	C6	10	-
23.	I/O		-	-	-	9	B5	11	174
24.	I/O		-	-	-	10	B6	12	177
25.	I/O (TMS)		17	9	6	11	A5	13	180
26.	I/O		18	10	7	12	C7	14	183
27.	I/O		-	-	-	13	B7	15	186
28.	I/O		-	11	8	14	A6	16	189
29.	I/O		19	12	9	15	A7	17	195
30.	I/O		20	13	10	16	A8	18	198
	GND		21	14	11	17	C8	19	-
	VCC		22	15	12	18	B8	20	-
31.	I/O		23	16	13	19	C9	21	201
32.	I/O		24	17	14	20	B9	22	207
33.	I/O		-	18	15	21	A9	23	210
34.	I/O		-	-	-	22	B10	24	213
35.	I/O		25	19	16	23	C10	25	219
36.	I/O		26	20	17	24	A10	26	222
37.	I/O		-	-	-	25	A11	27	225
38.	I/O		-	-	-	26	B11	28	231
	GND		-	-	-	27	C11	29	-
39.	I/O		27	21	18	28	B12	32	234
40.	I/O		-	22	19	29	A13	33	237
41.	I/O		-	-	-	30	A14	34	240
42.	I/O		-	-	-	31	C12	35	243
43.	I/O		28	23	20	32	B13	36	246
44.	I/O		29	24	21	33	B14	37	249
45.	M1 (I/O)		30	25	22	34	A15	38	258
	GND		31	26	23	35	C13	39	-
46.	M0 (I/O)		32	27	24	36	A16	40	261
	VCC		33	28	25	37	C14	41	-
47.	M2 (I/O)		34	29	26	38	B15	42	264
48.	GCK2 (I/O)		35	30	27	39	B16	43	267
49.	I/O (HDC)		36	31	28	40	D14	44	276
50.	I/O		-	-	-	41	C15	45	279
51.	I/O		-	-	-	42	D15	46	282
52.	I/O		-	32	29	43	E14	47	288
53.	I/O (LDC)		37	33	30	44	C16	48	291
54.	I/O		-	-	-	-	E15	49	294
55.	I/O		-	-	-	-	D16	50	300
	GND		-	-	-	45	F14	51	-
56.	I/O		-	-	-	46	F15	52	303

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
57.	I/O		-	-	-	47	E16	53	306
58.	I/O		38	34	31	48	F16	54	312
59.	I/O		39	35	32	49	G14	55	315
60.	I/O		-	36	33	50	G15	56	318
61.	I/O		-	37	34	51	G16	57	324
62.	I/O		40	38	35	52	H16	58	327
63.	I/O ($\overline{ERR}$, $\overline{INIT}$)		41	39	36	53	H15	59	330
	VCC		42	40	37	54	H14	60	-
	GND		43	41	38	55	J14	61	-
64.	I/O		44	42	39	56	J15	62	336
65.	I/O		45	43	40	57	J16	63	339
66.	I/O		-	44	41	58	K16	64	348
67.	I/O		-	45	42	59	K15	65	351
68.	I/O		46	46	43	60	K14	66	354
69.	I/O		47	47	44	61	L16	67	360
70.	I/O		-	-	-	62	M16	68	363
71.	I/O		-	-	-	63	L15	69	366
	GND		-	-	-	64	L14	70	-
72.	I/O		-	-	-	-	N16	71	372
73.	I/O		-	-	-	-	M15	72	375
74.	I/O		48	48	45	65	P16	73	378
75.	I/O		49	49	46	66	M14	74	384
76.	I/O		-	-	-	67	N15	75	387
77.	I/O		-	-	-	68	P15	76	390
78.	I/O		50	50	47	69	N14	77	396
79.	I/O		51	51	48	70	R16	78	399
	GND		52	52	49	71	P14	79	-
	DONE		53	53	50	72	R15	80	-
	VCC		54	54	51	73	P13	81	-
	PROG		55	55	52	74	R14	82	-
80.	I/O (D7)		56	56	53	75	T16	83	408
81.	GCK3 (I/O)		57	57	54	76	T15	84	411
82.	I/O		-	-	-	77	R13	85	420
83.	I/O		-	-	-	78	P12	86	423
84.	I/O (D6)		58	58	55	79	T14	87	426
85.	I/O		-	59	56	80	T13	88	432
	GND		-	-	-	81	P11	91	-
86.	I/O		-	-	-	82	R11	92	435
87.	I/O		-	-	-	83	T11	93	438
88.	I/O (D5)		59	60	57	84	T10	94	444
89.	I/O ($\overline{CS0}$)		60	61	58	85	P10	95	447
90.	I/O		-	62	59	86	R10	96	450
91.	I/O		-	63	60	87	T9	97	456
92.	I/O (D4)		61	64	61	88	R9	98	459
93.	I/O		62	65	62	89	P9	99	462
	VCC		63	66	63	90	R8	100	-
	GND		64	67	64	91	P8	101	-
94.	I/O (D3)		65	68	65	92	T8	102	468
95.	I/O ($\overline{RS}$)		66	69	66	93	T7	103	471
96.	I/O		-	70	67	94	T6	104	474
97.	I/O		-	-	-	95	R7	105	480
98.	I/O (D2)		67	71	68	96	P7	106	483

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
42.	I/O	-	-	-	-	-	28	C11	32	273
43.	I/O	25	19	16	23	25	29	B11	33	279
44.	I/O	26	20	17	24	26	30	A12	34	282
45.	I/O	-	-	-	25	27	31	B12	35	285
46.	I/O	-	-	-	26	28	32	A13	36	291
	GND	-	-	-	27	29	33	C12	37	-
47.	I/O	-	-	-	-	30	34	A15	40	294
48.	I/O	-	-	-	-	31	35	C13	41	297
49.	I/O	27	21	18	28	32	36	B14	42	303
50.	I/O	-	22	19	29	33	37	A16	43	306
51.	I/O	-	-	-	30	34	38	B15	44	309
52.	I/O	-	-	-	31	35	39	C14	45	315
53.	I/O	28	23	20	32	36	40	A17	46	318
54.	I/O	29	24	21	33	37	41	B16	47	321
55.	M1 (I/O)	30	25	22	34	38	42	C15	48	330
	GND	31	26	23	35	39	43	D15	49	-
56.	M0 (I/O)	32	27	24	36	40	44	A18	50	333
	VCC	33	28	25	37	41	45	D16	55	-
57.	M2 (I/O)	34	29	26	38	42	46	C16	56	336
58.	GCK2 (I/O)	35	30	27	39	43	47	B17	57	339
59.	I/O (HDC)	36	31	28	40	44	48	E16	58	348
60.	I/O	-	-	-	41	45	49	C17	59	351
61.	I/O	-	-	-	42	46	50	D17	60	354
62.	I/O	-	32	29	43	47	51	B18	61	360
63.	I/O (LDC)	37	33	30	44	48	52	E17	62	363
64.	I/O	-	-	-	-	49	53	F16	63	372
65.	I/O	-	-	-	-	50	54	C18	64	375
	GND	-	-	-	45	51	55	G16	67	-
66.	I/O	-	-	-	46	52	56	E18	68	378
67.	I/O	-	-	-	47	53	57	F18	69	384
68.	I/O	38	34	31	48	54	58	G17	70	387
69.	I/O	39	35	32	49	55	59	G18	71	390
70.	I/O	-	-	-	-	-	60	H16	72	396
71.	I/O	-	-	-	-	-	61	H17	73	399
72.	I/O	-	36	33	50	56	62	H18	74	402
73.	I/O	-	37	34	51	57	63	J18	75	408
74.	I/O	40	38	35	52	58	64	J17	76	411
75.	I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	41	39	36	53	59	65	J16	77	414
	VCC	42	40	37	54	60	66	J15	78	-
	GND	43	41	38	55	61	67	K15	79	-
76.	I/O	44	42	39	56	62	68	K16	80	420
77.	I/O	45	43	40	57	63	69	K17	81	423
78.	I/O	-	44	41	58	64	70	K18	82	426
79.	I/O	-	45	42	59	65	71	L18	83	432
80.	I/O	-	-	-	-	-	72	L17	84	435
81.	I/O	-	-	-	-	-	73	L16	85	438
82.	I/O	46	46	43	60	66	74	M18	86	444
83.	I/O	47	47	44	61	67	75	M17	87	447
84.	I/O	-	-	-	62	68	76	N18	88	450
85.	I/O	-	-	-	63	69	77	P18	89	456
	GND	-	-	-	64	70	78	M16	90	-
86.	I/O	-	-	-	-	71	79	T18	93	459

Pin	Description	PC84	TQ144	PQ160	TQ176	PQ208	PG223	BG225	PQ240	Boundary Scan Order
180.	I/O	-	-	-	-	-	N4	D11	190	39
181.	I/O	-	117	129	141	167	P2	A12	191	42
182.	I/O	-	-	130	142	168	T1	C11	192	45
183.	I/O	-	-	-	-	169	R1	B11	193	51
184.	I/O	-	-	-	-	170	N2	E10	194	54
	-	-	-	-	-	-	-	GND*		-
	GND	-	118	131	143	171	M3	-	196	-
185.	I/O	-	119	132	144	172	P1	A11	197	57
186.	I/O	-	120	133	145	173	N1	D10	198	66
187.	I/O	-	-	-	-	-	M4	C10	199	69
188.	I/O	-	-	-	-	-	L4	B10	200	75
	VCC	-	-	-	-	-	-	VCC*	201	-
189.	I/O (A4)	81	121	134	146	174	M2	A10	202	78
190.	I/O (A5)	82	122	135	147	175	M1	D9	203	81
191.	I/O	-	-	-	148	176	L3	C9	205	87
192.	I/O	-	-	136	149	177	L2	B9	206	90
193.	I/O	-	123	137	150	178	L1	A9	207	93
194.	I/O	-	124	138	151	179	K1	E9	208	99
195.	I/O (A6)	83	125	139	152	180	K2	C8	209	102
196.	I/O (A7)	84	126	140	153	181	K3	B8	210	105
	GND	1	127	141	154	182	K4	GND*	211	-

Additional No Connect (N.C.) Connections for PQ208 and PQ240 Packages

PQ208					PQ240		
1	53	105	157	208	22	143	219
3	54	107	158		37	158	
51	102	155	206		83	195	
52	104	156	207		98	204	

Notes: * Pins labeled VCC* are internally bonded to a VCC plane within the BG225 package. The external pins are: B2, D8, H15, R8, B14, R1, H1, and R15.
Pins labeled GND* are internally bonded to a ground plane within the BG225 package. The external pins are: A1, D12, G7, G9, H6, H8, H10, J8, K8, A8, F8, G8, H2, H7, H9, J7, J9, M8.
Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

Pin Locations for XC5215 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
	VCC	142	183	212	K1	VCC*	VCC*	-
1.	I/O (A8)	143	184	213	K2	E8	D14	138
2.	I/O (A9)	144	185	214	K3	B7	C14	141
3.	I/O	145	186	215	K5	A7	A15	147
4.	I/O	146	187	216	K4	C7	B15	150
5.	I/O	-	188	217	J1	D7	C15	153
6.	I/O	-	189	218	J2	E7	D15	159
7.	I/O (A10)	147	190	220	H1	A6	A16	162