AMD Xilinx - XC5210-5PQ240C Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	324
Number of Logic Elements/Cells	1296
Total RAM Bits	-
Number of I/O	196
Number of Gates	16000
Voltage - Supply	4.75V ~ 5.25V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	240-BFQFP
Supplier Device Package	240-PQFP (32x32)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc5210-5pq240c

can also be independently disabled for any flip-flop. CLR is active High. It is not invertible within the CLB.

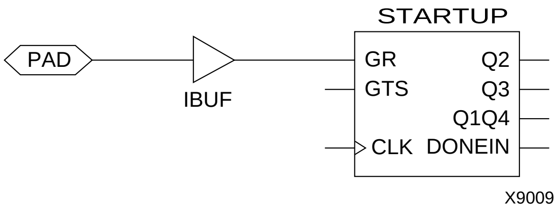


Figure 8: Schematic Symbols for Global Reset

Global Reset

A separate Global Reset line clears each storage element during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GR) does not compete with other routing resources; it uses a dedicated distribution network.

GR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GR pin of the STARTUP symbol. (See Figure 9.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global Reset signal. Alternatively, GR can be driven from any internal node.

Using FPGA Flip-Flops and Latches

The abundance of flip-flops in the XC5200 Series invites pipelined designs. This is a powerful way of increasing performance by breaking the function into smaller subfunctions and executing them in parallel, passing on the results through pipeline flip-flops. This method should be seriously considered wherever throughput is more important than latency.

To include a CLB flip-flop, place the appropriate library symbol. For example, FDCE is a D-type flip-flop with clock enable and asynchronous clear. The corresponding latch symbol is called LDCE.

In XC5200-Series devices, the flip-flops can be used as registers or shift registers without blocking the function generators from performing a different, perhaps unrelated task. This ability increases the functional capacity of the devices.

The CLB setup time is specified between the function generator inputs and the clock input CK. Therefore, the specified CLB flip-flop setup time includes the delay through the function generator.

Three-State Buffers

The XC5200 family has four dedicated Three-State Buffers (TBUFs, or BUFTs in the schematic library) per CLB (see Figure 9). The four buffers are individually configurable through four configuration bits to operate as simple non-inverting buffers or in 3-state mode. When in 3-state mode the CLB output enable (TS) control signal drives the enable to all four buffers. Each TBUF can drive up to two horizontal and/or two vertical Longlines. These 3-state buffers can be used to implement multiplexed or bidirectional buses on the horizontal or vertical longlines, saving logic resources.

The 3-state buffer enable is an active-High 3-state (i.e. an active-Low enable), as shown in Table 4.

Table 4: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN

Another 3-state buffer with similar access is located near each I/O block along the right and left edges of the array.

The longlines driven by the 3-state buffers have a weak keeper at each end. This circuit prevents undefined floating levels. However, it is overridden by any driver. To ensure the longline goes high when no buffers are on, add an additional BUFT to drive the output High during all of the previously undefined states.

Figure 10 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

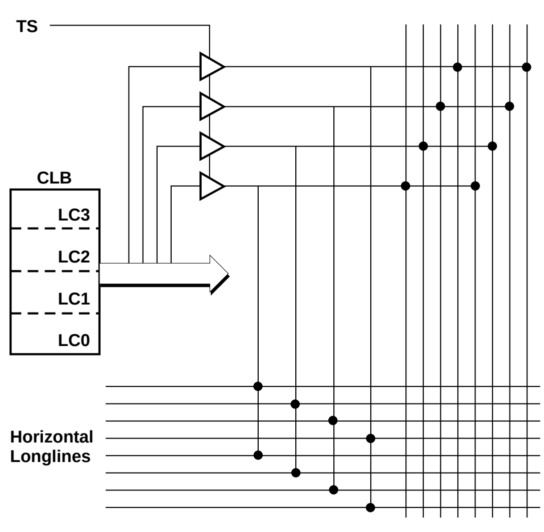


Figure 9: XC5200 3-State Buffers

to Vcc. The configurable pull-down resistor is an n-channel transistor that pulls to Ground.

The value of these resistors is 20 kΩ – 100 kΩ. This high value makes them unsuitable as wired-AND pull-up resistors.

The pull-up resistors for most user-programmable IOBs are active during the configuration process. See Table 13 on page 124 for a list of pins with pull-ups active before and during configuration.

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

JTAG Support

Embedded logic attached to the IOBs contains test structures compatible with IEEE Standard 1149.1 for boundary scan testing, simplifying board-level testing. More information is provided in “Boundary Scan” on page 98.

Oscillator

XC5200 devices include an internal oscillator. This oscillator is used to clock the power-on time-out, clear configuration memory, and source CCLK in Master configuration modes. The oscillator runs at a nominal 12 MHz frequency that varies with process, Vcc, and temperature. The output CCLK frequency is selectable as 1 MHz (default), 6 MHz, or 12 MHz.

The XC5200 oscillator divides the internal 12-MHz clock or a user clock. The user then has the choice of dividing by 4, 16, 64, or 256 for the “OSC1” output and dividing by 2, 8, 32, 128, 1024, 4096, 16384, or 65536 for the “OSC2” output. The division is specified via a “DIVIDEn_BY=x” attribute on the symbol, where n=1 for OSC1, or n=2 for OSC2. These frequencies can vary by as much as -50% or + 50%.

The OSC5 macro is used where an internal oscillator is required. The CK_DIV macro is applicable when a user clock input is specified (see Figure 13).

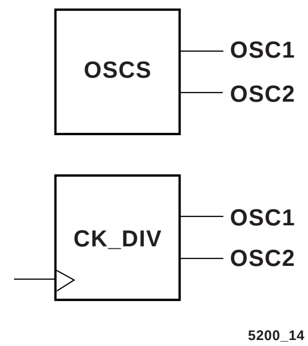


Figure 13: XC5200 Oscillator Macros

VersaBlock Routing

The General Routing Matrix (GRM) connects to the Versa-Block via 24 bidirectional ports (M0-M23). Excluding direct connections, global nets, and 3-statable Longlines, all VersaBlock inputs and outputs connect to the GRM via these 24 ports. Four 3-statable unidirectional signals (TQ0-TQ3) drive out of the VersaBlock directly onto the horizontal and vertical Longlines. Two horizontal global nets and two vertical global nets connect directly to every CLB clock pin; they can connect to other CLB inputs via the GRM. Each CLB also has four unidirectional direct connects to each of its four neighboring CLBs. These direct connects can also feed directly back to the CLB (see Figure 14).

In addition, each CLB has 16 direct inputs, four direct connections from each of the neighboring CLBs. These direct connections provide high-speed local routing that bypasses the GRM.

Local Interconnect Matrix

The Local Interconnect Matrix (LIM) is built from input and output multiplexers. The 13 CLB outputs (12 LC outputs plus a V_{CC}/GND signal) connect to the eight VersaBlock outputs via the output multiplexers, which consist of eight fully populated 13-to-1 multiplexers. Of the eight VersaBlock outputs, four signals drive each neighboring CLB directly, and provide a direct feedback path to the input multiplexers. The four remaining multiplexer outputs can drive the GRM through four TBUFs (TQ0-TQ3). All eight multiplexer outputs can connect to the GRM through the bidirectional M0-M23 signals. All eight signals also connect to the input multiplexers and are potential inputs to that CLB.

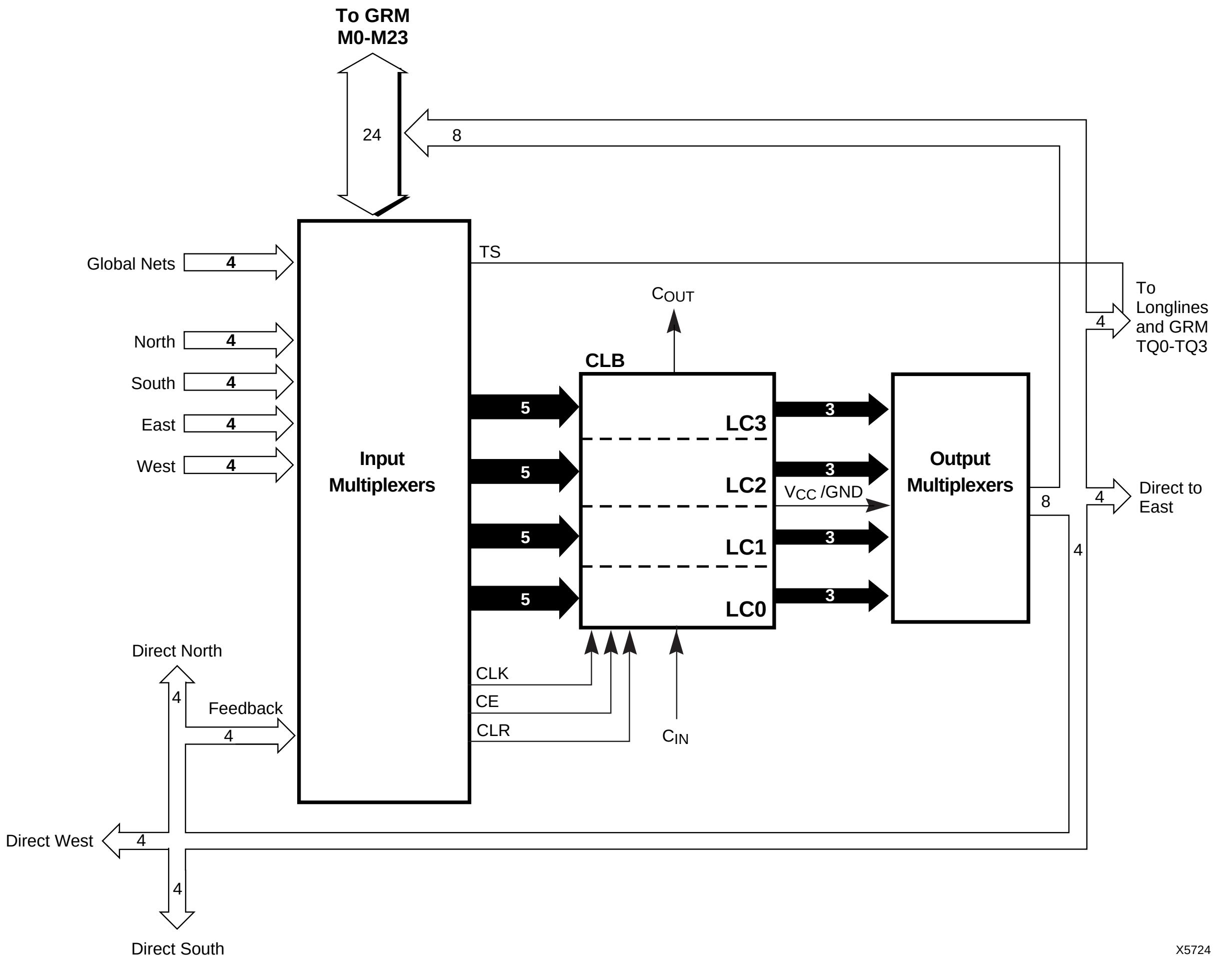


Figure 14: VersaBlock Details

CLB inputs have several possible sources: the 24 signals from the GRM, 16 direct connections from neighboring VersaBlocks, four signals from global, low-skew buffers, and the four signals from the CLB output multiplexers. Unlike the output multiplexers, the input multiplexers are not fully populated; i.e., only a subset of the available signals can be connected to a given CLB input. The flexibility of LUT input swapping and LUT mapping compensates for this limitation. For example, if a 2-input NAND gate is required, it can be mapped into any of the four LUTs, and use any two of the four inputs to the LUT.

Direct Connects

The unidirectional direct-connect segments are connected to the logic input/output pins through the CLB input and output multiplexer arrays, and thus bypass the general routing matrix altogether. These lines increase the routing channel utilization, while simultaneously reducing the delay incurred in speed-critical connections.

The direct connects also provide a high-speed path from the edge CLBs to the VersaRing input/output buffers, and thus reduce pin-to-pin set-up time, clock-to-out, and combinational propagation delay. Direct connects from the input buffers to the CLB DI pin (direct flip-flop input) are only available on the left and right edges of the device. CLB look-up table inputs and combinatorial/registered outputs have direct connects to input/output buffers on all four sides.

The direct connects are ideal for developing customized RPM cells. Using direct connects improves the macro performance, and leaves the other routing channels intact for improved routing. Direct connects can also route through a CLB using one of the four cell-feedthrough paths.

General Routing Matrix

The General Routing Matrix, shown in Figure 15, provides flexible bidirectional connections to the Local Interconnect

Matrix through a hierarchy of different-length metal segments in both the horizontal and vertical directions. A pro-

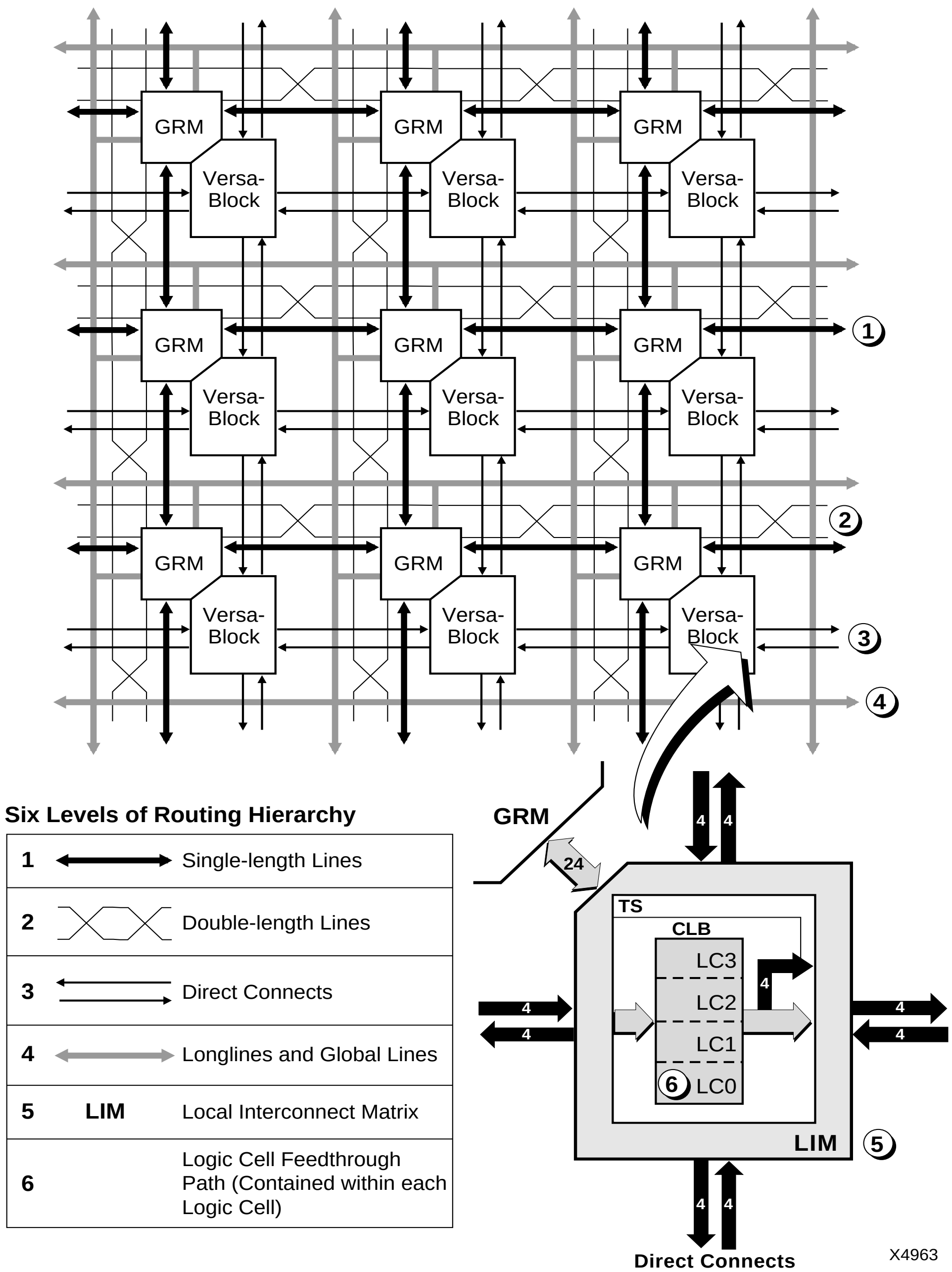


Figure 15: XC5200 Interconnect Structure

grammable interconnect point (PIP) establishes an electrical connection between two wire segments. The PIP, consisting of a pass transistor switch controlled by a memory element, provides bidirectional (in some cases, unidirectional) connection between two adjoining wires. A collection of PIPs inside the General Routing Matrix and in the Local Interconnect Matrix provides connectivity between various types of metal segments. A hierarchy of PIPs and associated routing segments combine to provide a powerful interconnect hierarchy:

- Forty bidirectional single-length segments per CLB provide ten routing channels to each of the four neighboring CLBs in four directions.
- Sixteen bidirectional double-length segments per CLB provide four routing channels to each of four other (non-neighboring) CLBs in four directions.
- Eight horizontal and eight vertical bidirectional Longline

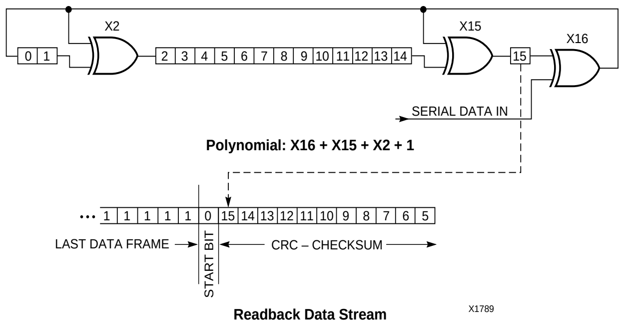


Figure 23: Circuit for Generating CRC-16

Configuration Sequence

There are four major steps in the XC5200-Series power-up configuration sequence.

- Power-On Time-Out
- Initialization
- Configuration
- Start-Up

The full process is illustrated in Figure 24.

Power-On Time-Out

An internal power-on reset circuit is triggered when power is applied. When V_{CC} reaches the voltage at which portions of the FPGA begin to operate (i.e., performs a write-and-read test of a sample pair of configuration memory bits), the programmable I/O buffers are 3-stated with active high-impedance pull-up resistors. A time-out delay — nominally 4 ms — is initiated to allow the power-supply voltage to stabilize. For correct operation the power supply must reach V_{CC}(min) by the end of the time-out, and must not dip below it thereafter.

There is no distinction between master and slave modes with regard to the time-out delay. Instead, the INIT line is used to ensure that all daisy-chained devices have completed initialization. Since XC2000 devices do not have this signal, extra care must be taken to guarantee proper operation when daisy-chaining them with XC5200 devices. For proper operation with XC3000 devices, the RESET signal, which is used in XC3000 to delay configuration, should be connected to INIT.

If the time-out delay is insufficient, configuration should be delayed by holding the INIT pin Low until the power supply has reached operating levels.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the PROGRAM pin Low. During all three phases — Power-on, Initialization, and Configuration — DONE is held Low; HDC, LDC, and INIT are active; DOUT is driven; and all I/O buffers are disabled.

Initialization

This phase clears the configuration memory and establishes the configuration mode.

The configuration memory is cleared at the rate of one frame per internal clock cycle (nominally 1 MHz). An open-drain bidirectional signal, INIT, is released when the configuration memory is completely cleared. The device then tests for the absence of an external active-low level on INIT. The mode lines are sampled two internal clock cycles later (nominally 2 µs).

The master device waits an additional 32 µs to 256 µs (nominally 64-128 µs) to provide adequate time for all of the slave devices to recognize the release of INIT as well. Then the master device enters the Configuration phase.

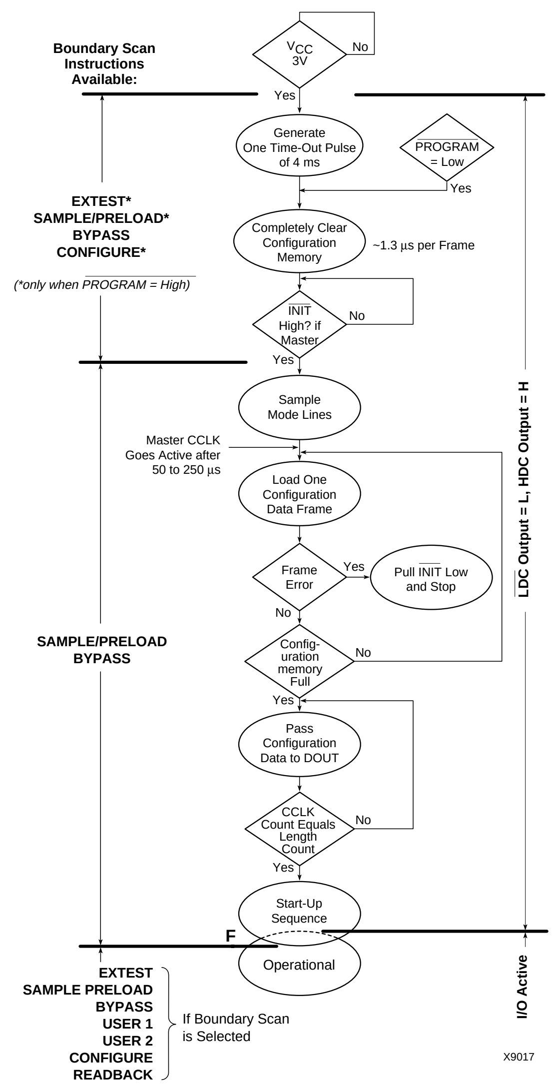
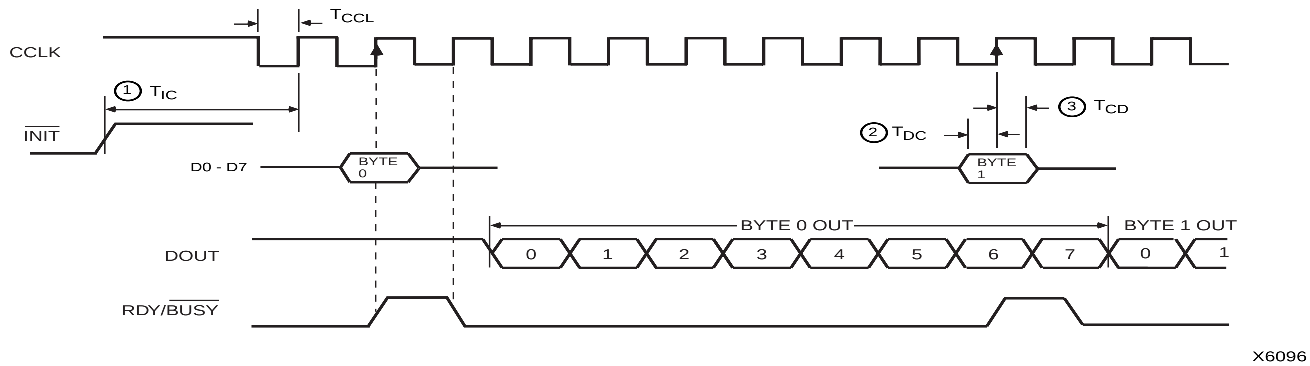


Figure 24: Configuration Sequence



	Description	Symbol		Min	Max	Units
CCLK	INIT (High) setup time	1	T_{IC}	5		µs
	D0 - D7 setup time	2	T_{DC}	60		ns
	D0 - D7 hold time	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	50		ns
	CCLK Low time		T_{CCL}	60		ns
	CCLK Frequency		F_{CC}		8	MHz

Notes:
1. Peripheral Synchronous mode can be considered Slave Parallel mode. An external CCLK provides timing, clocking in the **first** data byte on the **second** rising edge of CCLK after INIT goes high. Subsequent data bytes are clocked in on every eighth consecutive rising edge of CCLK.
2. The RDY/BUSY line goes High for one CCLK period after data has been clocked in, although synchronous operation does not require such a response.
3. The pin name RDY/BUSY is a misnomer. In synchronous peripheral mode this is really an ACKNOWLEDGE signal.
4. Note that data starts to shift out serially on the DOUT pin 0.5 CCLK periods after it was loaded in parallel. Therefore, additional CCLK pulses are clearly required after the last byte has been loaded.

Figure 34: Synchronous Peripheral Mode Programming Switching Characteristics

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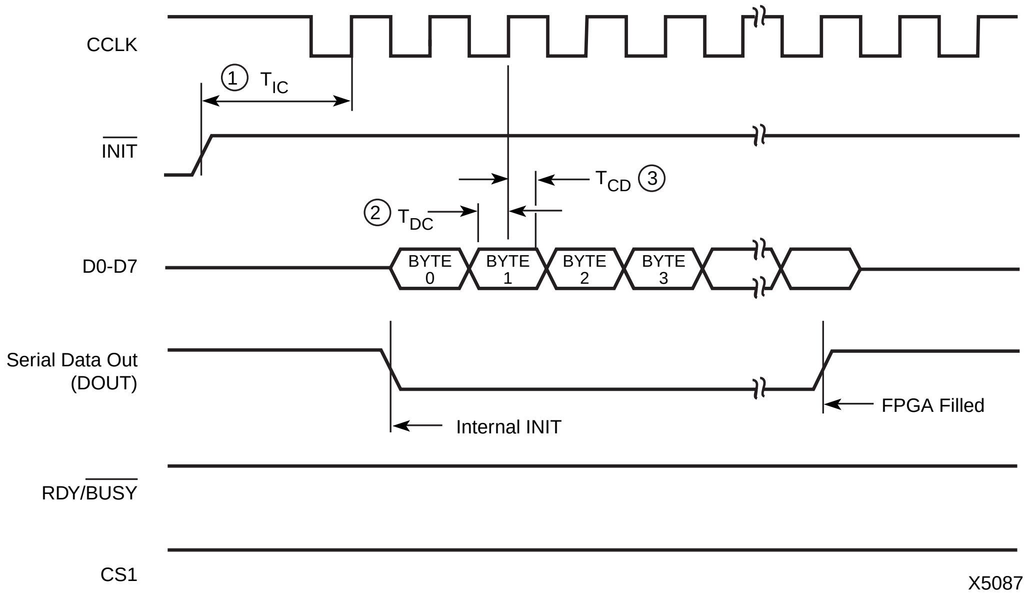

	Description	Symbol		Min	Max	Units
CCLK	INIT (High) Setup time required	1	T_{IC}	5		µs
	DIN Setup time required	2	T_{DC}	30		ns
	DIN hold time required	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	30		ns
	CCLK Low time		T_{CCL}	30		ns
	CCLK frequency		F_{CC}		10	MHz

Note: If not driven by the preceding DOUT, CS1 must remain high until the device is fully configured.

Figure 38: Express Mode Programming Switching Characteristics

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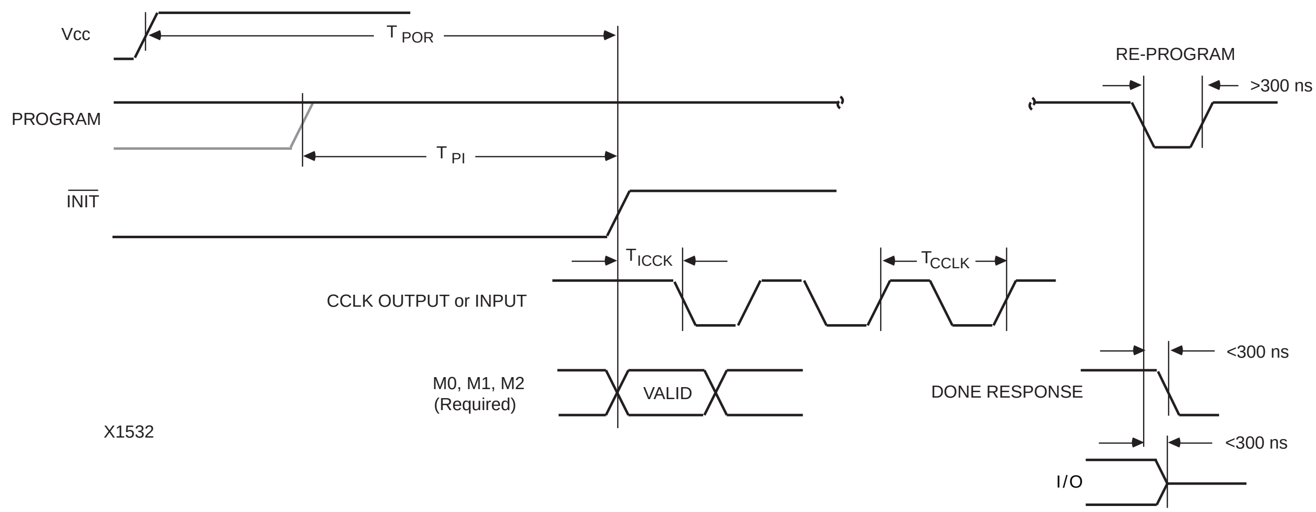
Configuration Switching Characteristics



Master Modes

Description	Symbol	Min	Max	Units
Power-On-Reset	T_{POR}	2	15	ms
Program Latency	T_{PI}	6	70	µs per CLB column
CCLK (output) Delay period (slow) period (fast)	T_{ICCK} T_{CCLK} T_{CCLK}	40 640 100	375 3000 375	µs ns ns

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Slave and Peripheral Modes

Description	Symbol	Min	Max	Units
Power-On-Reset	T_{POR}	2	15	ms
Program Latency	T_{PI}	6	70	µs per CLB column
CCLK (input) Delay (required) period (required)	T_{ICCK} T_{CCLK}	5 100		µs ns

Note: At power-up, V_{CC} must rise from 2.0 to V_{CC} min in less than 15 ms, otherwise delay configuration using $\overline{\text{PROGRAM}}$ until V_{CC} is valid.

XC5200 Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.[1]

XC5200 Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial: 0°C to 85°C junction	4.75	5.25	V
	Supply voltage relative to GND Industrial: -40°C to 100°C junction	4.5	5.5	V
V_{IHT}	High-level input voltage — TTL configuration	2.0	V_{CC}	V
V_{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V_{IHC}	High-level input voltage — CMOS configuration	70%	100%	V_{CC}
V_{ILC}	Low-level input voltage — CMOS configuration	0	20%	V_{CC}
T_{IN}	Input signal transition time		250	ns

XC5200 DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -8.0 mA, V_{CC} min	3.86		V
V_{OL}	Low-level output voltage @ I_{OL} = 8.0 mA, V_{CC} max		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 1)		15	mA
I_{IL}	Leakage current	-10	+10	µA
C_{IN}	Input capacitance (sample tested)		15	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02	0.30	mA

Note: 1. With no output current loads, all package pins at Vcc or GND, either TTL or CMOS inputs, and the FPGA configured with a tie option.

XC5200 Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature in plastic packages	+125	°C
	Junction temperature in ceramic packages	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

1. Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Product Obsolete or Under Obsolescence

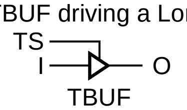
XC5200 Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-6	-5	-4	-3
Description	**Symbol**	**Device**	**Max (ns)**	**Max (ns)**	**Max (ns)**	**Max (ns)**
Global Signal Distribution From pad through global buffer, to any clock (CK)	T_{BUFG}	XC5202	9.1	8.5	8.0	6.9
		XC5204	9.3	8.7	8.2	7.6
		XC5206	9.4	8.8	8.3	7.7
		XC5210	9.4	8.8	8.5	7.7
		XC5215	10.5	9.9	9.8	9.6

XC5200 Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

		Speed Grade	-6	-5	-4	-3
Description	**Symbol**	**Device**	**Max (ns)**	**Max (ns)**	**Max (ns)**	**Max (ns)**
TBUF driving a Longline  I to Longline, while TS is Low; i.e., buffer is constantly active	T_{IO}	XC5202	6.0	3.8	3.0	2.0
		XC5204	6.4	4.1	3.2	2.3
		XC5206	6.6	4.2	3.3	2.7
		XC5210	6.6	4.2	3.3	2.9
		XC5215	7.3	4.6	3.8	3.2
TS going Low to Longline going from floating High or Low to active Low or High	T_{ON}	XC5202	7.8	5.6	4.7	4.0
		XC5204	8.3	5.9	4.9	4.3
		XC5206	8.4	6.0	5.0	4.4
		XC5210	8.4	6.0	5.0	4.4
		XC5215	8.9	6.3	5.3	4.5
TS going High to TBUF going inactive, not driving Longline	T_{OFF}	XC52xx	3.0	2.8	2.6	2.4

Note: 1. Die-size-dependent parameters are based upon XC5215 characterization. Production specifications will vary with array size.

XC5200 CLB Switching Characteristic Guidelines

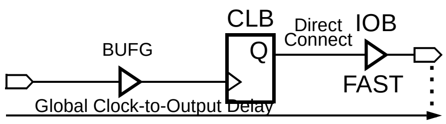
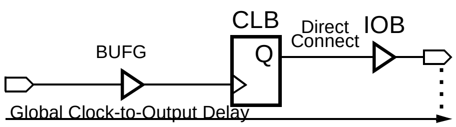
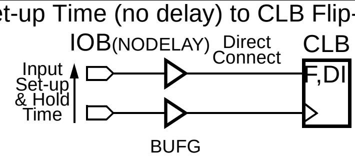
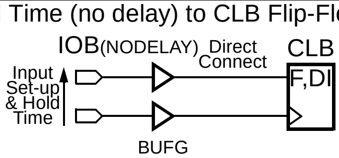
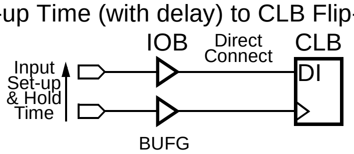
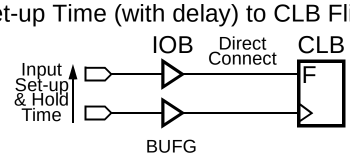
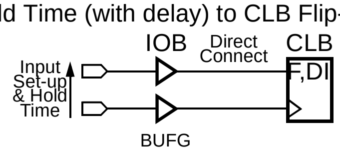
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the timing calculator and used in the simulator.

Speed Grade		-6		-5		-4		-3	
Description	**Symbol**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**	**Min (ns)**	**Max (ns)**
Combinatorial Delays									
F inputs to X output	T_{ILO}		5.6		4.6		3.8		3.0
F inputs via transparent latch to Q	T_{ITO}		8.0		6.6		5.4		4.3
DI inputs to DO output (Logic-Cell Feedthrough)	T_{IDO}		4.3		3.5		2.8		2.4
F inputs via F5_MUX to DO output	T_{IMO}		7.2		5.8		5.0		4.3
Carry Delays									
Incremental delay per bit	T_{CY}		0.7		0.6		0.5		0.5
Carry-in overhead from DI	T_{CYDI}		1.8		1.6		1.5		1.4
Carry-in overhead from F	T_{CYL}		3.7		3.2		2.9		2.4
Carry-out overhead to DO	T_{CYO}		4.0		3.2		2.5		2.1
Sequential Delays									
Clock (CK) to out (Q) (Flip-Flop)	T_{CKO}		5.8		4.9		4.0		4.0
Gate (Latch enable) going active to out (Q)	T_{GO}		9.2		7.4		5.9		5.5
Set-up Time Before Clock (CK)									
F inputs	T_{ICK}	2.3		1.8		1.4		1.3	
F inputs via F5_MUX	T_{MICK}	3.8		3.0		2.5		2.4	
DI input	T_{DICK}	0.8		0.5		0.4		0.4	
CE input	T_{EICK}	1.6		1.2		0.9		0.9	
Hold Times After Clock (CK)									
F inputs	T_{CKI}	0		0		0		0	
F inputs via F5_MUX	T_{CKMI}	0		0		0		0	
DI input	T_{CKDI}	0		0		0		0	
CE input	T_{CKEI}	0		0		0		0	
Clock Widths									
Clock High Time	T_{CH}	6.0		6.0		6.0		6.0	
Clock Low Time	T_{CL}	6.0		6.0		6.0		6.0	
Toggle Frequency (MHz) (Note 3)	F_{TOG}		83		83		83		83
Reset Delays									
Width (High)	T_{CLRW}	6.0		6.0		6.0		6.0	
Delay from CLR to Q (Flip-Flop)	T_{CLR}		7.7		6.3		5.1		4.0
Delay from CLR to Q (Latch)	T_{CLRL}		6.5		5.2		4.2		3.0
Global Reset Delays									
Width (High)	T_{GCLRW}	6.0		6.0		6.0		6.0	
Delay from internal GR to Q	T_{GCLR}		14.7		12.1		9.1		8.0

Note:
1. The CLB K to Q output delay (T_{CKO}) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold-time requirement (T_{CKDI}) of any CLB on the same die.
2. Timing is based upon the XC5215 device. For other devices, see Timing Calculator.
3. Maximum flip-flop toggle rate for export control purposes.

XC5200 Guaranteed Input and Output Parameters (Pin-to-Pin)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the Global Buffer specifications. The delay calculator uses this indirect method, and may overestimate because of worst-case assumptions. When there is a discrepancy between these two methods, the values listed below should be used, and the derived values should be considered conservative overestimates.

		Speed Grade	-6	-5	-4	-3
Description	**Symbol**	**Device**	**Max (ns)**	**Max (ns)**	**Max (ns)**	**Max (ns)**
Global Clock to Output Pad (fast) 	T_{ICKOF}	XC5202	16.9	15.1	10.9	9.8
		XC5204	17.1	15.3	11.3	9.9
	(Max)	XC5206	17.2	15.4	11.9	10.8
		XC5210	17.2	15.4	12.8	11.2
		XC5215	19.0	17.0	12.8	11.7
Global Clock to Output Pad (slew-limited) 	T_{ICKO}	XC5202	21.4	18.7	12.6	11.5
		XC5204	21.6	18.9	13.3	11.9
	(Max)	XC5206	21.7	19.0	13.6	12.5
		XC5210	21.7	19.0	15.0	12.9
		XC5215	24.3	21.2	15.0	13.1
Input Set-up Time (no delay) to CLB Flip-Flop 	T_{PSUF}	XC5202	2.5	2.0	1.9	1.9
		XC5204	2.3	1.9	1.9	1.9
	(Min)	XC5206	2.2	1.9	1.9	1.9
		XC5210	2.2	1.9	1.9	1.8
		XC5215	2.0	1.8	1.7	1.7
Input Hold Time (no delay) to CLB Flip-Flop 	T_{PHF}	XC5202	3.8	3.8	3.5	3.5
		XC5204	3.9	3.9	3.8	3.6
	(Min)	XC5206	4.4	4.4	4.4	4.3
		XC5210	5.1	5.1	4.9	4.8
		XC5215	5.8	5.8	5.7	5.6
Input Set-up Time (with delay) to CLB Flip-Flop DI Input 	T_{PSU}	XC5202	7.3	6.6	6.6	6.6
		XC5204	7.3	6.6	6.6	6.6
		XC5206	7.2	6.5	6.4	6.3
		XC5210	7.2	6.5	6.0	6.0
		XC5215	6.8	5.7	5.7	5.7
Input Set-up Time (with delay) to CLB Flip-Flop F Input 	T_{PSUL}	XC5202	8.8	7.7	7.5	7.5
		XC5204	8.6	7.5	7.5	7.5
	(Min)	XC5206	8.5	7.4	7.4	7.4
		XC5210	8.5	7.4	7.4	7.3
		XC5215	8.5	7.4	7.4	7.2
Input Hold Time (with delay) to CLB Flip-Flop 	T_{PH} (Min)	XC52xx	0	0	0	0

Note:
1. These measurements assume that the CLB flip-flop uses a direct interconnect to or from the IOB. The INREG/ OUTREG properties, or XACT-Performance, can be used to assure that direct connects are used. t_{PSU} applies only to the CLB input DI that bypasses the look-up table, which only offers direct connects to IOBs on the left and right edges of the die. t_{PSUL} applies to the CLB inputs F that feed the look-up table, which offers direct connect to IOBs on all four edges, as do the CLB Q outputs.
2. When testing outputs (fast or slew-limited), half of the outputs on one side of the device are switching.

Device-Specific Pinout Tables

Device-specific tables include all packages for each XC5200-Series device. They follow the pad locations around the die, and include boundary scan register locations.

Pin Locations for XC5202 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	VCC	-	2	92	89	128	H3	-
1.	I/O (A8)	57	3	93	90	129	H1	51
2.	I/O (A9)	58	4	94	91	130	G1	54
3.	I/O	-	-	95	92	131	G2	57
4.	I/O	-	-	96	93	132	G3	63
5.	I/O (A10)	-	5	97	94	133	F1	66
6.	I/O (A11)	59	6	98	95	134	F2	69
	GND	-	-	-	-	137	F3	-
7.	I/O (A12)	60	7	99	96	138	E3	78
8.	I/O (A13)	61	8	100	97	139	C1	81
9.	I/O (A14)	62	9	1	98	142	B1	90
10.	I/O (A15)	63	10	2	99	143	B2	93
	VCC	64	11	3	100	144	C3	-
	GND	-	12	4	1	1	C4	-
11.	GCK1 (A16, I/O)	1	13	5	2	2	B3	102
12.	I/O (A17)	2	14	6	3	3	A1	105
13.	I/O (TDI)	3	15	7	4	6	B4	111
14.	I/O (TCK)	4	16	8	5	7	A3	114
	GND	-	-	-	-	8	C6	-
15.	I/O (TMS)	5	17	9	6	11	A5	117
16.	I/O	6	18	10	7	12	C7	123
17.	I/O	-	-	-	-	13	B7	126
18.	I/O	-	-	11	8	14	A6	129
19.	I/O	-	19	12	9	15	A7	135
20.	I/O	7	20	13	10	16	A8	138
	GND	8	21	14	11	17	C8	-
	VCC	9	22	15	12	18	B8	-
21.	I/O	-	23	16	13	19	C9	141
22.	I/O	10	24	17	14	20	B9	147
23.	I/O		-	18	15	21	A9	150
24.	I/O		-	-	-	22	B10	153
25.	I/O	-	25	19	16	23	C10	159
26.	I/O	11	26	20	17	24	A10	162
	GND		-	-	-	27	C11	-
27.	I/O	12	27	21	18	28	B12	165
28.	I/O		-	22	19	29	A13	171
29.	I/O	13	28	23	20	32	B13	174
30.	I/O	14	29	24	21	33	B14	177
31.	M1 (I/O)	15	30	25	22	34	A15	186
	GND	-	31	26	23	35	C13	-
32.	M0 (I/O)	16	32	27	24	36	A16	189
	VCC	-	33	28	25	37	C14	-
33.	M2 (I/O)	17	34	29	26	38	B15	192
34.	GCK2 (I/O)	18	35	30	27	39	B16	195

Pin	Description	VQ64*	PC84	PQ100	VQ100	TQ144	PG156	Boundary Scan Order
	CCLK	48	73	77	74	107	R2	-
	VCC	-	74	78	75	108	P3	-
74.	I/O (TDO)	49	75	79	76	109	T1	0
	GND	-	76	80	77	110	N3	-
75.	I/O (A0, $\overline{\text{WS}}$)	50	77	81	78	111	R1	9
76.	GCK4 (A1, I/O)	51	78	82	79	112	P2	15
77.	I/O (A2, CS1)	52	79	83	80	115	P1	18
78.	I/O (A3)	-	80	84	81	116	N1	21
	GND	-	-	-	-	118	L3	-
79.	I/O (A4)	-	81	85	82	121	K3	27
80.	I/O (A5)	53	82	86	83	122	K2	30
81.	I/O	-	-	87	84	123	K1	33
82.	I/O	-	-	88	85	124	J1	39
83.	I/O (A6)	54	83	89	86	125	J2	42
84.	I/O (A7)	55	84	90	87	126	J3	45
	GND	56	1	91	88	127	H2	-

* VQ64 package supports Master Serial, Slave Serial, and Express configuration modes only.

Additional No Connect (N.C.) Connections on TQ144 Package

TQ144					
135	9	41	67	98	117
136	10	42	68	99	119
140	25	46	77	103	120
141	26	47	78	104	
4	30	62	82	113	
5	31	63	83	114	

Notes: Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

Pin Locations for XC5204 Devices

The following table may contain pinout information for unsupported device/package combinations. Please see the availability charts elsewhere in the XC5200 Series data sheet for availability information.

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
	VCC		2	92	89	128	H3	142	-
1.	I/O (A8)		3	93	90	129	H1	143	78
2.	I/O (A9)		4	94	91	130	G1	144	81
3.	I/O		-	95	92	131	G2	145	87
4.	I/O		-	96	93	132	G3	146	90
5.	I/O (A10)		5	97	94	133	F1	147	93
6.	I/O (A11)		6	98	95	134	F2	148	99
7.	I/O		-	-	-	135	E1	149	102
8.	I/O		-	-	-	136	E2	150	105
	GND		-	-	-	137	F3	151	-
9.	I/O		-	-	-	-	D1	152	111
10.	I/O		-	-	-	-	D2	153	114
11.	I/O (A12)		7	99	96	138	E3	154	117
12.	I/O (A13)		8	100	97	139	C1	155	123
13.	I/O		-	-	-	140	C2	156	126

Pin	Description		PC84	PQ100	VQ100	TQ144	PG156	PQ160	Boundary Scan Order
99.	I/O		68	72	69	97	T5	107	486
100.	I/O		-	-	-	98	R6	108	492
101.	I/O		-	-	-	99	T4	109	495
	GND		-	-	-	100	P6	110	-
102.	I/O (D1)		69	73	70	101	T3	113	498
103.	I/O (RCLK-BUSY/RDY)		70	74	71	102	P5	114	504
104.	I/O		-	-	-	103	R4	115	507
105.	I/O		-	-	-	104	R3	116	510
106.	I/O (D0, DIN)		71	75	72	105	P4	117	516
107.	I/O (DOUT)		72	76	73	106	T2	118	519
	CCLK		73	77	74	107	R2	119	-
	VCC		74	78	75	108	P3	120	-
108.	I/O (TDO)		75	79	76	109	T1	121	0
	GND		76	80	77	110	N3	122	-
109.	I/O (A0, $\overline{\text{WS}}$)		77	81	78	111	R1	123	9
110.	GCK4 (A1, I/O)		78	82	79	112	P2	124	15
111.	I/O		-	-	-	113	N2	125	18
112.	I/O		-	-	-	114	M3	126	21
113.	I/O (A2, CS1)		79	83	80	115	P1	127	27
114.	I/O (A3)		80	84	81	116	N1	128	30
115.	I/O		-	-	-	117	M2	129	33
116.	I/O		-	-	-	-	M1	130	39
	GND		-	-	-	118	L3	131	-
117.	I/O		-	-	-	119	L2	132	42
118.	I/O		-	-	-	120	L1	133	45
119.	I/O (A4)		81	85	82	121	K3	134	51
120.	I/O (A5)		82	86	83	122	K2	135	54
121.	I/O		-	87	84	123	K1	137	57
122.	I/O		-	88	85	124	J1	138	63
123.	I/O (A6)		83	89	86	125	J2	139	66
124.	I/O (A7)		84	90	87	126	J3	140	69
	GND		1	91	88	127	H2	141	-

Additional No Connect (N.C.) Connections for PQ160 Package

PQ160				
8	30	89	111	136
9	31	90	112	

Notes: Boundary Scan Bit 0 = TDO.T
Boundary Scan Bit 1 = TDO.O
Boundary Scan Bit 1056 = BSCAN.UPD

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
42.	I/O	-	-	-	-	-	28	C11	32	273
43.	I/O	25	19	16	23	25	29	B11	33	279
44.	I/O	26	20	17	24	26	30	A12	34	282
45.	I/O	-	-	-	25	27	31	B12	35	285
46.	I/O	-	-	-	26	28	32	A13	36	291
	GND	-	-	-	27	29	33	C12	37	-
47.	I/O	-	-	-	-	30	34	A15	40	294
48.	I/O	-	-	-	-	31	35	C13	41	297
49.	I/O	27	21	18	28	32	36	B14	42	303
50.	I/O	-	22	19	29	33	37	A16	43	306
51.	I/O	-	-	-	30	34	38	B15	44	309
52.	I/O	-	-	-	31	35	39	C14	45	315
53.	I/O	28	23	20	32	36	40	A17	46	318
54.	I/O	29	24	21	33	37	41	B16	47	321
55.	M1 (I/O)	30	25	22	34	38	42	C15	48	330
	GND	31	26	23	35	39	43	D15	49	-
56.	M0 (I/O)	32	27	24	36	40	44	A18	50	333
	VCC	33	28	25	37	41	45	D16	55	-
57.	M2 (I/O)	34	29	26	38	42	46	C16	56	336
58.	GCK2 (I/O)	35	30	27	39	43	47	B17	57	339
59.	I/O (HDC)	36	31	28	40	44	48	E16	58	348
60.	I/O	-	-	-	41	45	49	C17	59	351
61.	I/O	-	-	-	42	46	50	D17	60	354
62.	I/O	-	32	29	43	47	51	B18	61	360
63.	I/O (LDC)	37	33	30	44	48	52	E17	62	363
64.	I/O	-	-	-	-	49	53	F16	63	372
65.	I/O	-	-	-	-	50	54	C18	64	375
	GND	-	-	-	45	51	55	G16	67	-
66.	I/O	-	-	-	46	52	56	E18	68	378
67.	I/O	-	-	-	47	53	57	F18	69	384
68.	I/O	38	34	31	48	54	58	G17	70	387
69.	I/O	39	35	32	49	55	59	G18	71	390
70.	I/O	-	-	-	-	-	60	H16	72	396
71.	I/O	-	-	-	-	-	61	H17	73	399
72.	I/O	-	36	33	50	56	62	H18	74	402
73.	I/O	-	37	34	51	57	63	J18	75	408
74.	I/O	40	38	35	52	58	64	J17	76	411
75.	I/O ($\overline{\text{ERR}}$, $\overline{\text{INIT}}$)	41	39	36	53	59	65	J16	77	414
	VCC	42	40	37	54	60	66	J15	78	-
	GND	43	41	38	55	61	67	K15	79	-
76.	I/O	44	42	39	56	62	68	K16	80	420
77.	I/O	45	43	40	57	63	69	K17	81	423
78.	I/O	-	44	41	58	64	70	K18	82	426
79.	I/O	-	45	42	59	65	71	L18	83	432
80.	I/O	-	-	-	-	-	72	L17	84	435
81.	I/O	-	-	-	-	-	73	L16	85	438
82.	I/O	46	46	43	60	66	74	M18	86	444
83.	I/O	47	47	44	61	67	75	M17	87	447
84.	I/O	-	-	-	62	68	76	N18	88	450
85.	I/O	-	-	-	63	69	77	P18	89	456
	GND	-	-	-	64	70	78	M16	90	-
86.	I/O	-	-	-	-	71	79	T18	93	459

Pin	Description	PC84	PQ100	VQ100	TQ144	PQ160	TQ176	PG191	PQ208	Boundary Scan Order
87.	I/O	-	-	-	-	72	80	P17	94	468
88.	I/O	48	48	45	65	73	81	N16	95	471
89.	I/O	49	49	46	66	74	82	T17	96	480
90.	I/O	-	-	-	67	75	83	R17	97	483
91.	I/O	-	-	-	68	76	84	P16	98	486
92.	I/O	50	50	47	69	77	85	U18	99	492
93.	I/O	51	51	48	70	78	86	T16	100	495
	GND	52	52	49	71	79	87	R16	101	-
	DONE	53	53	50	72	80	88	U17	103	-
	VCC	54	54	51	73	81	89	R15	106	-
	PROG	55	55	52	74	82	90	V18	108	-
94.	I/O (D7)	56	56	53	75	83	91	T15	109	504
95.	GCK3 (I/O)	57	57	54	76	84	92	U16	110	507
96.	I/O	-	-	-	77	85	93	T14	111	516
97.	I/O	-	-	-	78	86	94	U15	112	519
98.	I/O (D6)	58	58	55	79	87	95	V17	113	522
99.	I/O	-	59	56	80	88	96	V16	114	528
100.	I/O	-	-	-	-	89	97	T13	115	531
101.	I/O	-	-	-	-	90	98	U14	116	534
	GND	-	-	-	81	91	99	T12	119	-
102.	I/O	-	-	-	82	92	100	U13	120	540
103.	I/O	-	-	-	83	93	101	V13	121	543
104.	I/O (D5)	59	60	57	84	94	102	U12	122	552
105.	I/O ($\overline{\text{CS0}}$)	60	61	58	85	95	103	V12	123	555
106.	I/O	-	-	-	-	-	104	T11	124	558
107.	I/O	-	-	-	-	-	105	U11	125	564
108.	I/O	-	62	59	86	96	106	V11	126	567
109.	I/O	-	63	60	87	97	107	V10	127	570
110.	I/O (D4)	61	64	61	88	98	108	U10	128	576
111.	I/O	62	65	62	89	99	109	T10	129	579
	VCC	63	66	63	90	100	110	R10	130	-
	GND	64	67	64	91	101	111	R9	131	-
112.	I/O (D3)	65	68	65	92	102	112	T9	132	588
113.	I/O ($\overline{\text{RS}}$)	66	69	66	93	103	113	U9	133	591
114.	I/O	-	70	67	94	104	114	V9	134	600
115.	I/O	-	-	-	95	105	115	V8	135	603
116.	I/O	-	-	-	-	-	116	U8	136	612
117.	I/O	-	-	-	-	-	117	T8	137	615
118.	I/O (D2)	67	71	68	96	106	118	V7	138	618
119.	I/O	68	72	69	97	107	119	U7	139	624
120.	I/O	-	-	-	98	108	120	V6	140	627
121.	I/O	-	-	-	99	109	121	U6	141	630
	GND	-	-	-	100	110	122	T7	142	-
122.	I/O	-	-	-	-	111	123	U5	145	636
123.	I/O	-	-	-	-	112	124	T6	146	639
124.	I/O (D1)	69	73	70	101	113	125	V3	147	642
125.	I/O (RCLK-$\overline{\text{BUSY/RDY}}$)	70	74	71	102	114	126	V2	148	648
126.	I/O	-	-	-	103	115	127	U4	149	651
127.	I/O	-	-	-	104	116	128	T5	150	654
128.	I/O (D0, DIN)	71	75	72	105	117	129	U3	151	660
129.	I/O (DOUT)	72	76	73	106	118	130	T4	152	663

Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
54.	I/O	-	-	-	A8	-	L26	366
55.	I/O	-	19	23	C9	G4	M23	369
56.	I/O	-	20	24	B9	G3	M24	375
57.	I/O	15	21	25	E10	G2	M25	378
58.	I/O	16	22	26	A9	G1	M26	381
59.	I/O	17	23	27	D10	G5	N24	390
60.	I/O	18	24	28	C10	H3	N25	393
	GND	19	25	29	A10	GND*	GND*	-
	VCC	20	26	30	A11	VCC*	VCC*	-
61.	I/O	21	27	31	B10	H4	N26	399
62.	I/O	22	28	32	B11	H5	P25	402
63.	I/O	23	29	33	C11	J2	P23	405
64.	I/O	24	30	34	E11	J1	P24	411
65.	I/O	-	31	35	D11	J3	R26	414
66.	I/O	-	32	36	A12	J4	R25	417
67.	I/O	-	-	-	B12	-	R24	423
68.	I/O	-	-	-	A13	-	R23	426
69.	I/O	-	-	38	E12	J5	T26	429
70.	I/O	-	-	39	B13	K1	T25	435
	VCC	-	-	40	A16	VCC*	VCC*	-
71.	I/O	25	33	41	A14	K2	U24	438
72.	I/O	26	34	42	C13	K3	V25	441
73.	I/O	27	35	43	B14	J6	V24	447
74.	I/O	28	36	44	D13	L1	U23	450
	GND	29	37	45	A15	GND*	GND*	-
75.	I/O	-	-	-	B15	-	Y26	453
76.	I/O	-	-	-	E13	-	W25	459
77.	I/O	-	-	46	C14	L2	W24	462
78.	I/O	-	-	47	A17	K4	V23	465
79.	I/O	-	38	48	D14	L3	AA26	471
80.	I/O	-	39	49	B16	M1	Y25	474
81.	I/O	30	40	50	C15	K5	Y24	477
82.	I/O	31	41	51	E14	M2	AA25	483
83.	I/O	-	-	-	A18	-	AB25	486
84.	I/O	-	-	-	D15	-	AA24	489
85.	I/O	32	42	52	C16	L4	Y23	495
86.	I/O	33	43	53	B17	N1	AC26	498
87.	I/O	34	44	54	B18	M3	AA23	501
88.	I/O	35	45	55	E15	N2	AB24	507
89.	I/O	36	46	56	D16	K6	AD25	510
90.	I/O	37	47	57	C17	P1	AC24	513
91.	M1 (I/O)	38	48	58	A20	N3	AB23	522
	GND	39	49	59	A19	GND*	GND*	-
92.	M0 (I/O)	40	50	60	C18	P2	AD24	525
	VCC	41	55	61	B20	VCC*	VCC*	-
93.	M2 (I/O)	42	56	62	D17	M4	AC23	528
94.	GCK2 (I/O)	43	57	63	B19	R2	AE24	531
95.	I/O (HDC)	44	58	64	C19	P3	AD23	540
96.	I/O	45	59	65	F16	L5	AC22	543
97.	I/O	46	60	66	E17	N4	AF24	546
98.	I/O	47	61	67	D18	R3	AD22	552
99.	I/O (LDC)	48	62	68	C20	P4	AE23	555

Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
100.	I/O	-	-	-	F17	-	AE22	558
101.	I/O	-	-	-	G16	-	AF23	564
102.	I/O	49	63	69	D19	K7	AD20	567
103.	I/O	50	64	70	E18	M5	AE21	570
104.	I/O	-	65	71	D20	R4	AF21	576
105.	I/O	-	66	72	G17	N5	AC19	579
106.	I/O	-	-	73	F18	P5	AD19	582
107.	I/O	-	-	74	H16	L6	AE20	588
108.	I/O	-	-	-	E19	-	AF20	591
109.	I/O	-	-	-	F19	-	AC18	594
	GND	51	67	75	E20	GND*	GND*	-
110.	I/O	52	68	76	H17	R5	AD18	600
111.	I/O	53	69	77	G18	M6	AE19	603
112.	I/O	54	70	78	G19	N6	AC17	606
113.	I/O	55	71	79	H18	P6	AD17	612
	VCC	-	-	80	F20	VCC*	VCC*	-
114.	I/O	-	72	81	J16	R6	AE17	615
115.	I/O	-	73	82	G20	M7	AE16	618
116.	I/O	-	-	-	H20	-	AF16	624
117.	I/O	-	-	-	J18	-	AC15	627
118.	I/O	-	-	84	J19	N7	AD15	630
119.	I/O	-	-	85	K16	P7	AE15	636
120.	I/O	56	74	86	J20	R7	AF15	639
121.	I/O	57	75	87	K17	L7	AD14	642
122.	I/O	58	76	88	K18	N8	AE14	648
123.	I/O (ERR, INIT)	59	77	89	K19	P8	AF14	651
	VCC	60	78	90	L20	VCC*	VCC*	-
	GND	61	79	91	K20	GND*	GND*	-
124.	I/O	62	80	92	L19	L8	AE13	660
125.	I/O	63	81	93	L18	P9	AC13	663
126.	I/O	64	82	94	L16	R9	AD13	672
127.	I/O	65	83	95	L17	N9	AF12	675
128.	I/O	-	84	96	M20	M9	AE12	678
129.	I/O	-	85	97	M19	L9	AD12	684
130.	I/O	-	-	-	N20	-	AC12	687
131.	I/O	-	-	-	M18	-	AF11	690
132.	I/O	-	-	99	N19	R10	AE11	696
133.	I/O	-	-	100	P20	P10	AD11	699
	VCC	-	-	101	T20	VCC*	VCC*	-
134.	I/O	66	86	102	N18	N10	AE9	702
135.	I/O	67	87	103	P19	K9	AD9	708
136.	I/O	68	88	104	N17	R11	AC10	711
137.	I/O	69	89	105	R19	P11	AF7	714
	GND	70	90	106	R20	GND*	GND*	-
138.	I/O	-	-	-	N16	-	AE8	720
139.	I/O	-	-	-	P18	-	AD8	723
140.	I/O	-	-	107	U20	M10	AC9	726
141.	I/O	-	-	108	P17	N11	AF6	732
142.	I/O	-	91	109	T19	R12	AE7	735
143.	I/O	-	92	110	R18	L10	AD7	738
144.	I/O	71	93	111	P16	P12	AE6	744
145.	I/O	72	94	112	V20	M11	AE5	747

Pin	Description	PQ160	HQ208	HQ240	PG299	BG225	BG352	Boundary Scan Order
146.	I/O	-	-	-	R17	-	AD6	750
147.	I/O	-	-	-	T18	-	AC7	756
148.	I/O	73	95	113	U19	R13	AF4	759
149.	I/O	74	96	114	V19	N12	AF3	768
150.	I/O	75	97	115	R16	P13	AD5	771
151.	I/O	76	98	116	T17	K10	AE3	774
152.	I/O	77	99	117	U18	R14	AD4	780
153.	I/O	78	100	118	X20	N13	AC5	783
	GND	79	101	119	W20	GND*	GND*	-
	DONE	80	103	120	V18	P14	AD3	-
	VCC	81	106	121	X19	VCC*	VCC*	-
	PROG	82	108	122	U17	M12	AC4	-
154.	I/O (D7)	83	109	123	W19	P15	AD2	792
155.	GCK3 (I/O)	84	110	124	W18	N14	AC3	795
156.	I/O	85	111	125	T15	L11	AB4	804
157.	I/O	86	112	126	U16	M13	AD1	807
158.	I/O	-	-	127	V17	N15	AA4	810
159.	I/O	-	-	128	X18	M14	AA3	816
160.	I/O	-	-	-	U15	-	AB2	819
161.	I/O	-	-	-	T14	-	AC1	828
162.	I/O (D6)	87	113	129	W17	J10	Y3	831
163.	I/O	88	114	130	V16	L12	AA2	834
164.	I/O	89	115	131	X17	M15	AA1	840
165.	I/O	90	116	132	U14	L13	W4	843
166.	I/O	-	117	133	V15	L14	W3	846
167.	I/O	-	118	134	T13	K11	Y2	852
168.	I/O	-	-	-	W16	-	Y1	855
169.	I/O	-	-	-	W15	-	V4	858
	GND	91	119	135	X16	GND*	GND*	-
170.	I/O	-	-	136	U13	L15	V3	864
171.	I/O	-	-	137	V14	K12	W2	867
172.	I/O	92	120	138	W14	K13	U4	870
173.	I/O	93	121	139	V13	K14	U3	876
	VCC	-	-	140	X15	VCC*	VCC*	-
174.	I/O (D5)	94	122	141	T12	K15	V2	879
175.	I/O ($\overline{\text{CS0}}$)	95	123	142	X14	J12	V1	882
176.	I/O	-	-	-	X13	-	T1	888
177.	I/O	-	-	-	V12	-	R4	891
178.	I/O	-	124	144	W12	J13	R3	894
179.	I/O	-	125	145	T11	J14	R2	900
180.	I/O	96	126	146	X12	J15	R1	903
181.	I/O	97	127	147	U11	J11	P3	906
182.	I/O (D4)	98	128	148	V11	H13	P2	912
183.	I/O	99	129	149	W11	H14	P1	915
	VCC	100	130	150	X10	VCC*	VCC*	-
	GND	101	131	151	X11	GND*	GND*	-
184.	I/O (D3)	102	132	152	W10	H12	N2	924
185.	I/O ($\overline{\text{RS}}$)	103	133	153	V10	H11	N4	927
186.	I/O	104	134	154	T10	G14	N3	936
187.	I/O	105	135	155	U10	G15	M1	939
188.	I/O	-	136	156	X9	G13	M2	942
189.	I/O	-	137	157	W9	G12	M3	948