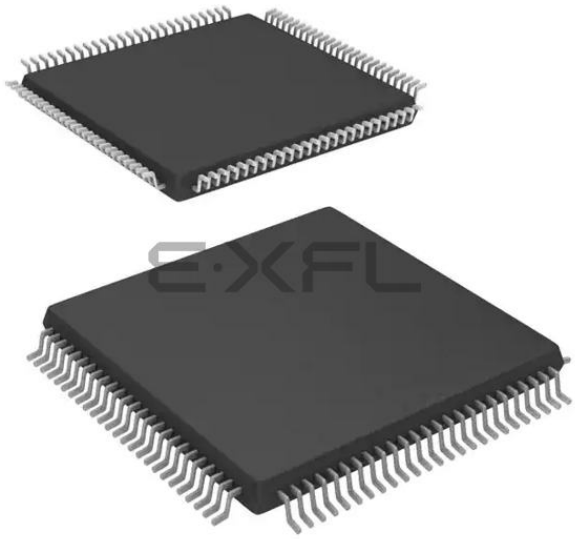

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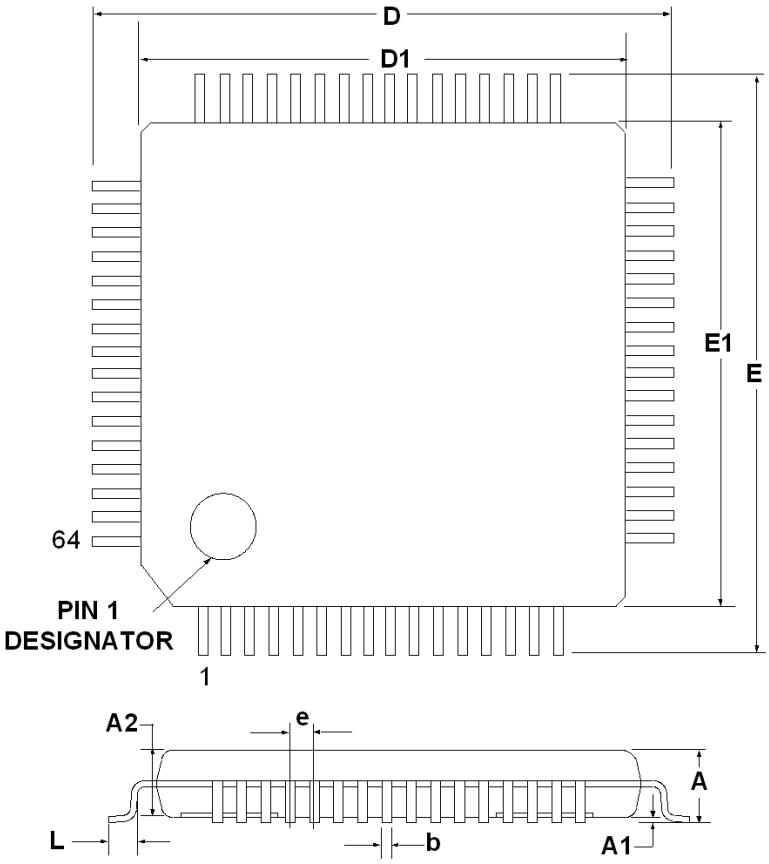
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 13x12b; D/A 2x10b, 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f040r

Figure 1.3. C8051F044/6 Block Diagram



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	-	1.05
b	0.17	0.22	0.27
D	-	12.00	-
D1	-	10.00	-
e	-	0.50	-
E	-	12.00	-
E1	-	10.00	-
L	0.45	0.6	0.75

Figure 4.4. TQFP-64 Package Drawing

SFR Definition 5.1. AMX0CF: AMUX0 Configuration

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	PORT3IC	HVDA2C	AIN23IC	AIN01IC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

SFR Address: 0xBA
SFR Page: 0

Bits7-4: UNUSED. Read = 0000b; Write = don't care
Bit3: PORT3IC: Port 3 even/odd Pin Input Pair Configuration Bit
0: Port 3 even and odd input channels are independent single-ended inputs
1: Port 3 even and odd input channels are (respectively) +, - difference input pair
Bit2: HVDA2C: HVDA 2's Compliment Bit
0: HVDA output measured as an independent single-ended input
1: HVDA result for 2's compliment value
Bit1: AIN23IC: AIN0.2, AIN0.3 Input Pair Configuration Bit
0: AIN0.2 and AIN0.3 are independent single-ended inputs
1: AIN0.2, AIN0.3 are (respectively) +, - difference input pair
Bit0: AIN01IC: AIN0.0, AIN0.1 Input Pair Configuration Bit
0: AIN0.0 and AIN0.1 are independent single-ended inputs
1: AIN0.0, AIN0.1 are (respectively) +, - difference input pair

NOTE: The ADC0 Data Word is in 2's complement format for channels configured as difference.

SFR Definition 5.2. AMX0SL: AMUX0 Channel Select

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX0AD3	AMX0AD2	AMX0AD1	AMX0AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

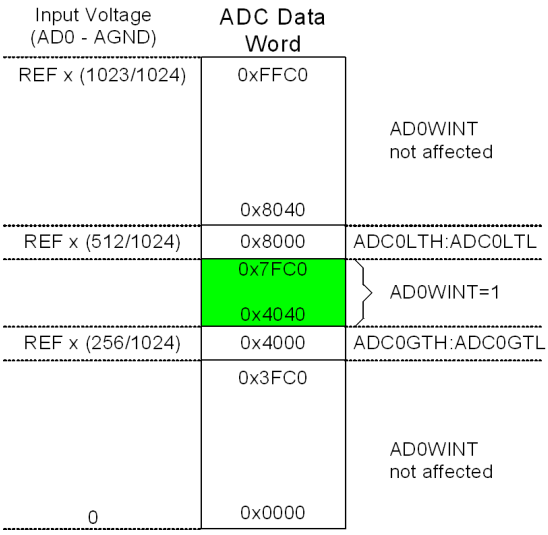
SFR Address: 0xBB
SFR Page: 0

Bits7-4: UNUSED. Read = 0000b; Write = don't care
Bits3-0: AMX0AD3-0: AMX0 Address Bits
0000-1111b: ADC Inputs selected per Table 5.1.

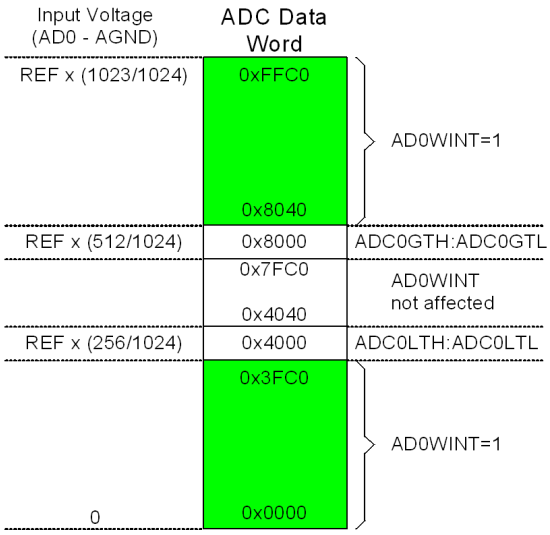
Table 5.3. High-Voltage Difference Amplifier Electrical Characteristics

V_{DD} = 3.0 V, AV+ = 3.0 V, V_{REF} = 3.0 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Inputs					
Differential range	peak-to-peak	—	—	60	V
Common Mode Range	(HVAIN+) – (HVAIN–) = 0 V	–60	—	+60	V
Analog Output					
Output Voltage Range		0.1	—	2.9	V
DC Performance					
Common Mode Rejection Ratio	Vcm= –10 V to +10 V, Rs=0	44	52	—	dB
Offset Voltage		—	±3	—	mV
Noise	HVCAP floating	—	500	—	nV/rtHz
Nonlinearity	G = 1	—	72	—	dB
Dynamic Performance					
Small Signal Bandwidth	G = 0.05	—	3	—	MHz
Small Signal Bandwidth	G = 1	—	150	—	kHz
Slew Rate		—	2	—	V/ —s
Settling Time	0.01%, G = 0.05, 10 V step	—	10	—	—s
Input/Output Impedance					
Differential (HVAIN+) input		—	105	—	kΩ
Differential (HVAIN-) input		—	98	—	kΩ
Common Mode input		—	51	—	kΩ
HVCAP		—	5	—	kΩ
Power Specification					
Quiescent Current		—	450	1000	—A



Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x8000,
ADC0GTH:ADC0GTL = 0x4000.
An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x8000 and > 0x4000.



Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x4000,
ADC0GTH:ADC0GTL = 0x8000.
An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x4000 or > 0x8000.

Figure 6.10. 10-Bit ADC0 Window Interrupt Example:
Left Justified Single-Ended Data

7.2. ADC2 Modes of Operation

ADC2 has a maximum conversion speed of 500 ksps. The ADC2 conversion clock (SAR2 clock) is a divided version of the system clock, determined by the AD2SC bits in the ADC2CF register (system clock divided by (AD2SC + 1) for $0 \leq AD2SC \leq 31$). The maximum ADC2 conversion clock is 7.5 MHz.

7.2.1. Starting a Conversion

A conversion can be initiated in one of five ways, depending on the programmed states of the ADC2 Start of Conversion Mode bits (AD2CM2–0) in ADC2CN. Conversions may be initiated by the following:

- Writing a '1' to the AD2BUSY bit of ADC2CN;
- A Timer 3 overflow (i.e., timed continuous conversions);
- A rising edge detected on the external ADC convert start signal, CNVSTR2 or CNVSTR0 (see important note below);
- A Timer 2 overflow (i.e., timed continuous conversions);
- Writing a '1' to the AD0BUSY of register ADC0CN (initiate conversion of ADC2 and ADC0 with a single software command).

An important note about external convert start (CNVSTR0 and CNVSTR2): If CNVSTR2 is enabled in the digital crossbar ( ), CNVSTR2 will be the external convert start signal for ADC2. However, if only CNVSTR0 is enabled in the digital crossbar and CNVSTR2 is not enabled, then CNVSTR0 may serve as the start of conversion for both ADC0 and ADC2. This permits synchronous sampling of both ADC0 and ADC2.

During conversion, the AD2BUSY bit is set to logic 1 and restored to 0 when conversion is complete. The falling edge of AD2BUSY triggers an interrupt (when enabled) and sets the interrupt flag in ADC2CN. Converted data is available in the ADC2 data word, ADC2.

When a conversion is initiated by writing a '1' to AD2BUSY, it is recommended to poll AD2INT to determine when the conversion is complete. The recommended procedure is:

Step 1. Write a '0' to AD2INT;
Step 2. Write a '1' to AD2BUSY;
Step 3. Poll AD2INT for '1';
Step 4. Process ADC2 data.

7.2.2. Tracking Modes

According to Table 7.2, each ADC2 conversion must be preceded by a minimum tracking time for the converted result to be accurate. The AD2TM bit in register ADC2CN controls the ADC2 track-and-hold mode. In its default state, the ADC2 input is continuously tracked, except when a conversion is in progress. When the AD2TM bit is logic 1, ADC2 operates in low-power tracking mode. In this mode, each conversion is preceded by a tracking period of 3 SAR clocks (after the start-of-conversion signal). When the CNVSTR2 (or CNVSTR0, See Section 7.2.1 above) signal is used to initiate conversions in low-power tracking mode, ADC2 tracks only when CNVSTR2 is low; conversion begins on the rising edge of CNVSTR2 (see Figure 7.2). Tracking can also be disabled (shutdown) when the entire chip is in low power standby or sleep modes. Low-power Track-and-Hold mode is also useful when AMUX or PGA settings are frequently changed, due to the settling time requirements described in

.

Table 7.1. AMUX Selection Chart (AMX2AD2-0 and AMX2CF3-0 bits)

		AMX2AD2-0							
		000	001	010	011	100	101	110	111
AMX2CF Bits 3-0	0000	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
	0001	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
	0010	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	P1.6	P1.7
	0011	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	P1.6	P1.7
	0100	P1.0	P1.1	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	0101	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	0110	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	0111	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	1000	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1001	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1010	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1011	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1100	P1.0	P1.1	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1101	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1110	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1111	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)

SFR Definition 19.5. SMB0STA: SMBus0 Status

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
STA7	STA6	STA5	STA4	STA3	STA2	STA1	STA0	11111000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC1
SFR Page: 0

Bits7-3: STA7-STA3: SMBus0 Status Code.
These bits contain the SMBus0 Status Code. There are 28 possible status codes; each status code corresponds to a single SMBus state. A valid status code is present in SMB0STA when the SI flag (SMB0CN.3) is set to logic 1. The content of SMB0STA is not defined when the SI flag is logic 0. Writing to the SMB0STA register at any time will yield indeterminate results.

Bits2-0: STA2-STA0: The three least significant bits of SMB0STA are always read as logic 0 when the SI flag is logic 1.

24.2.3. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/ Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

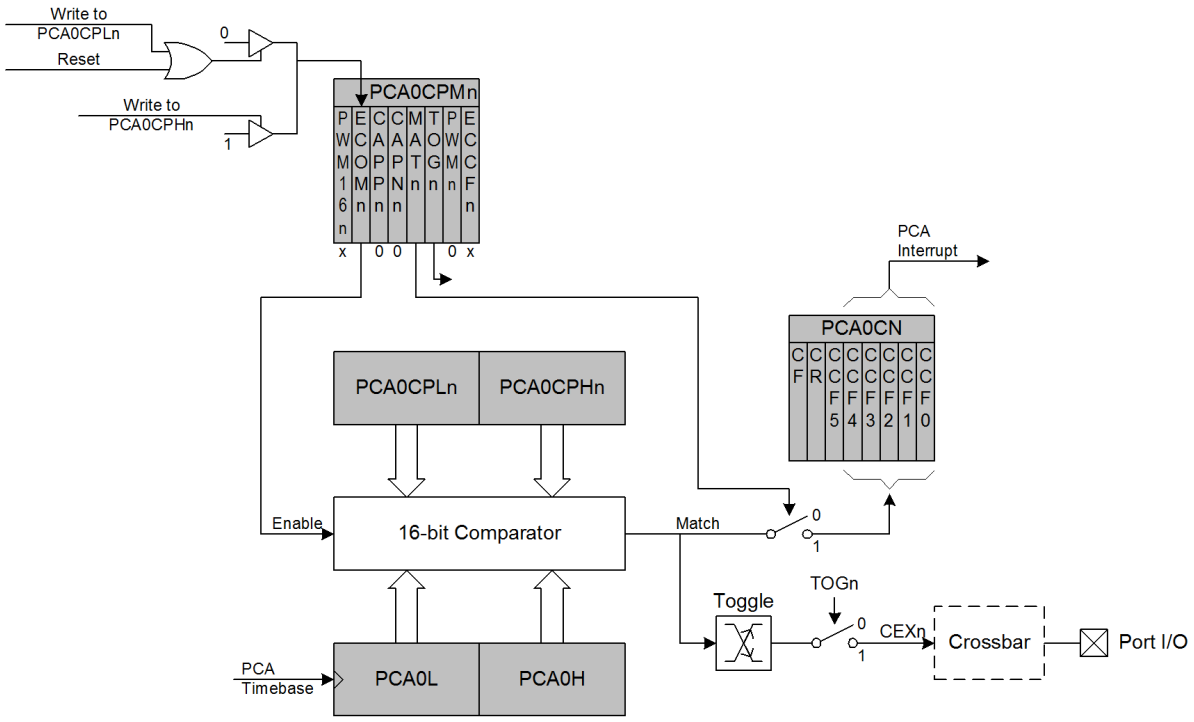


Figure 24.6. PCA High-Speed Output Mode Diagram

24.2.5. 8-Bit Pulse Width Modulator Mode

Each module can be used independently to generate pulse width modulated (PWM) outputs on its associated CEXn pin. The frequency of the output is dependent on the timebase for the PCA0 counter/timer. The duty cycle of the PWM output signal is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA0 counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be high. When the count value in PCA0L overflows, the CEXn output will be low (see Figure 24.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the counter/timer's high byte (PCA0H) without software intervention. Setting the ECOMn and PWMn bits in the PCA0CPMn register enables 8-Bit Pulse Width Modulator mode. The duty cycle for 8-Bit PWM Mode is given by Equation 24.2.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to '0'; writing to PCA0CPHn sets ECOMn to '1'.

$$DutyCycle = \frac{(256 - PCA0CPHn)}{256}$$

Equation 24.2. 8-Bit PWM Duty Cycle

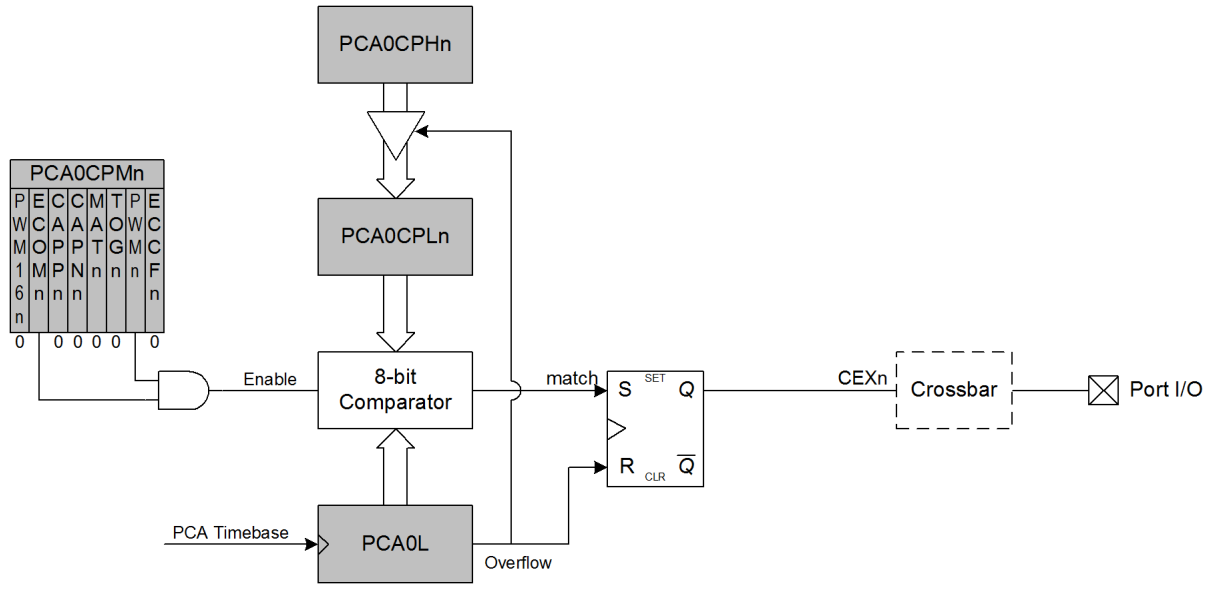


Figure 24.8. PCA 8-Bit PWM Mode Diagram