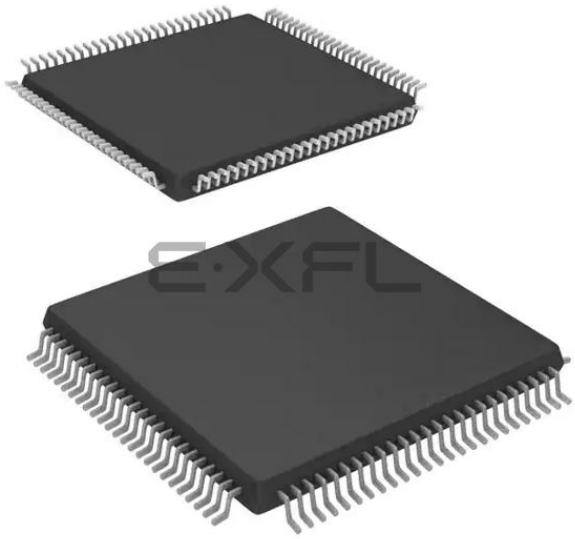

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 13x10b; D/A 2x10b, 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f042-gq

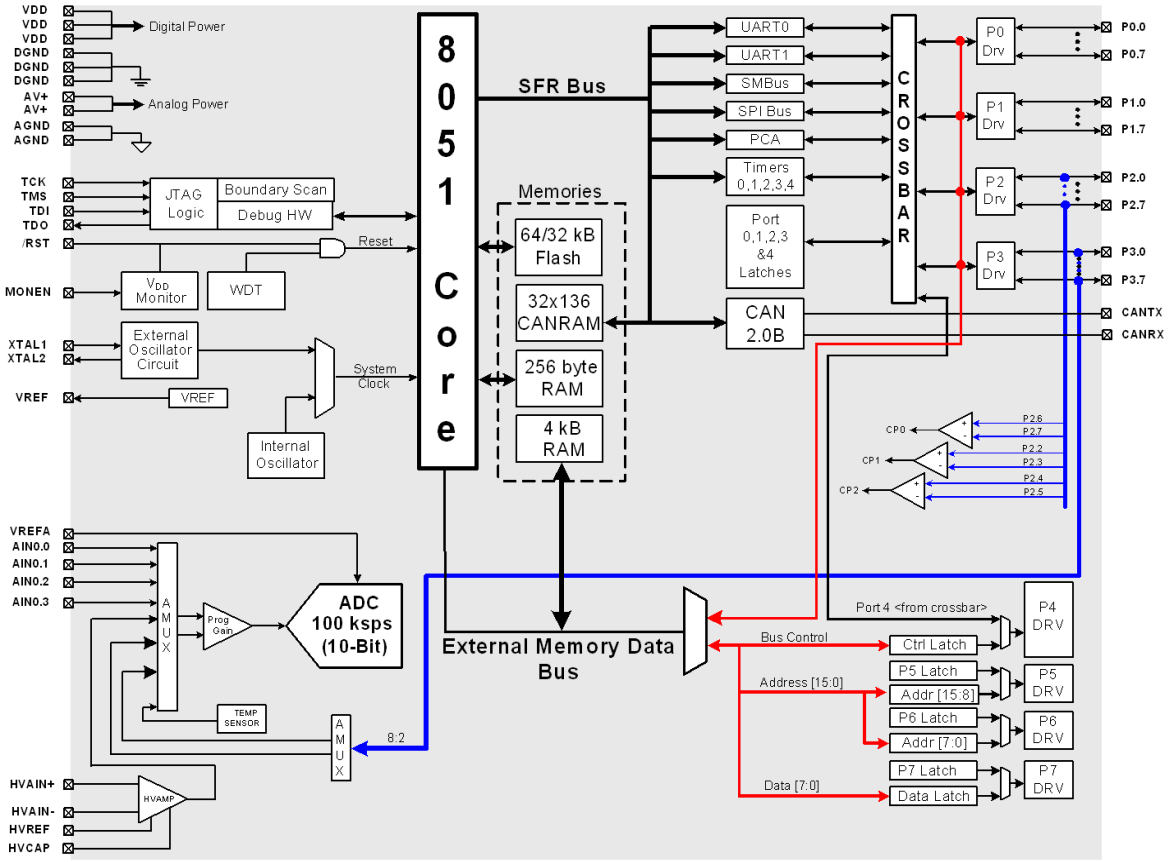


Figure 1.4. C8051F045/7 Block Diagram

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Pin (except V_{DD}, Port I/O, and JTAG pins) with respect to DGND		–0.3	—	V_{DD} + 0.3	V
Voltage on any Port I/O Pin, /RST, and JTAG pins with respect to DGND		–0.3	—	5.8	V
Voltage on V_{DD} with respect to DGND		–0.3	—	4.2	V
Maximum Total current through V_{DD}, AV+, DGND, and AGND		—	—	800	mA
Maximum output current sunk by any Port pin		—	—	100	mA
Maximum output current sunk by any other I/O pin		—	—	50	mA
Maximum output current sourced by any Port pin		—	—	100	mA
Maximum output current sourced by any other I/O pin		—	—	50	mA

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Due to special I/O design requirements of the High Voltage Difference Amplifier, undue electrical over-voltage stress (i.e., ESD) experienced by these pads may result in impedance degradation of these inputs (HVAIN+ and HVAIN–). For this reason, care should be taken to ensure proper handling and use as typically required to prevent ESD damage to electrostatically sensitive CMOS devices (e.g., static-free workstations, use of grounding straps, over-voltage protection in end-applications, etc.)

3. Global DC Electrical Characteristic

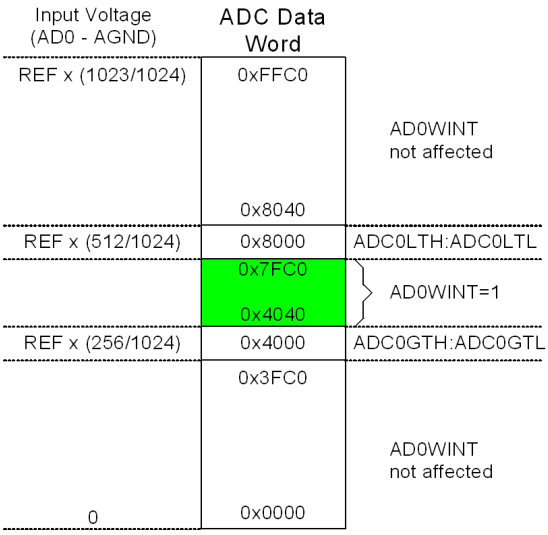
Table 3.1. Global DC Electrical Characteristics

–40 to +85 °C, 25 MHz System Clock unless otherwise specified.

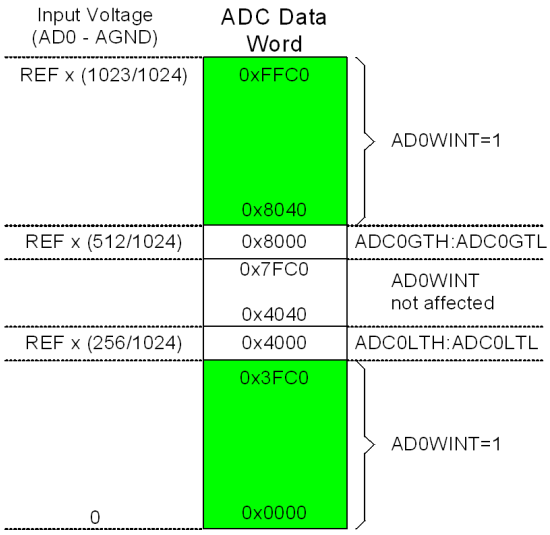
Parameter	Conditions	Min	Typ	Max	Units
Analog Supply Voltage[1]		2.7	3.0	3.6	V
Analog Supply Current	Internal REF, ADC, DAC, Comparators all active	—	1.7	—	mA
Analog Supply Current with analog sub-systems inactive	Internal REF, ADC, DAC, Comparators all disabled, oscillator disabled	—	0.2	—	µA
Analog-to-Digital Supply Delta ($\|V_{DD}$ - AV+$\|$)		—	—	0.5	V
Digital Supply Voltage		2.7	3.0	3.6	V
Digital Supply Current with CPU active (Normal Mode)	V_{DD} = 2.7 V, Clock = 25 MHz V_{DD} = 2.7 V, Clock = 1 MHz V_{DD} = 2.7 V, Clock = 32 kHz	— — —	10 0.5 20	— — —	mA mA µA
Digital Supply Current with CPU inactive (not accessing Flash) (Idle Mode)	V_{DD} = 2.7 V, Clock = 25 MHz V_{DD} = 2.7 V, Clock = 1 MHz V_{DD} = 2.7 V, Clock = 32 kHz	— — —	5 0.2 10	— — —	mA mA µA
Digital Supply Current (shutdown) (Stop Mode)	Oscillator not running	—	0.2	—	µA
Digital Supply RAM Data Retention Voltage		—	1.5	—	V
Specified Operating Temperature Range		–40	—	+85	°C
SYSCLK (system clock frequency)[2]		0	—	25	MHz
Tsysl (SYSCLK low time)		18	—	—	ns
Tsysh (SYSCLK high time)		18	—	—	ns

Notes:

1. Analog Supply AV+ must be greater than 1 V for V_{DD} monitor to operate.
2. SYSCLK must be at least 32 kHz to enable debugging.



Given:
AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x8000,
ADC0GTH:ADC0GTL = 0x4000.
An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x8000 and > 0x4000.
Given:



AMX0SL = 0x00, AMX0CF = 0x00, ADLJST = 1,
ADC0LTH:ADC0LTL = 0x4000,
ADC0GTH:ADC0GTL = 0x8000.
An ADC End of Conversion will cause an ADC Window Compare Interrupt (ADWINT=1) if the resulting ADC Data Word is < 0x4000 or > 0x8000.

Figure 6.10. 10-Bit ADC0 Window Interrupt Example: Left Justified Single-Ended Data

Table 6.2. 10-Bit ADC0 Electrical Characteristics

V_{DD} = 3.0 V, AV+ = 3.0 V, V_{REF} = 2.40 V (REFBE = 0), PGA Gain = 1, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			10		bits
Integral Nonlinearity		—	—	±1	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±1	LSB
Offset Error		—	0.2±1	—	LSB
Full Scale Error	Differential mode	—	0.1±1	—	LSB
Offset Temperature Coefficient		—	±0.25	—	ppm/°C
Dynamic Performance (10 kHz sine-wave input, 0 to 1 dB below Full Scale, 100 ksps)					
Signal-to-Noise Plus Distortion		59	—	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	–70	—	dB
Spurious-Free Dynamic Range		—	80	—	dB
Conversion Rate					
SAR Clock Frequency		—	—	2.5	MHz
Conversion Time in SAR Clocks		16	—	—	clocks
Track/Hold Acquisition Time		1.5	—	—	µs
Throughput Rate		—	—	100	ksps
Analog Inputs					
Input Voltage Range	Single-ended operation	0	—	VREF	V
Common-mode Voltage Range	Differential operation	AGND	—	AV+	V
Input Capacitance		—	10	—	pF
Temperature Sensor					
Nonlinearity[1,2]		—	±1	—	°C
Absolute Accuracy[1,2]		—	±3	—	°C
Gain[1,2]		—	2.86 ±0.034	—	mV/°C
Offset[1,2]	Temp = 0 °C	—	0.776 ±0.009	—	V
Power Specifications					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100 ksps	—	450	900	µA
Power Supply Rejection		—	±0.3	—	mV/V

Notes:
1. Represents one standard deviation from the mean.
2. Includes ADC offset, gain, and linearity variations.

7.3. ADC2 Programmable Window Detector

The ADC2 Programmable Window Detector continuously compares the ADC2 output to user-programmed limits, and notifies the system when an out-of-bound condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD2WINT in ADC2CN) can also be used in polled mode. The reference words are loaded into the ADC2 Greater-Than and ADC2 Less-Than registers (ADC2GT and ADC2LT). Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC2GT and ADC2LT registers.

SFR Definition 7.6. ADC2GT: ADC2 Greater-Than Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC4
SFR Page: 2

Bits7-0: High byte of ADC2 Greater-Than Data Word.

SFR Definition 7.7. ADC2LT: ADC2 Less-Than Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC6
SFR Page: 2

Bits7-0: Low byte of ADC2 Greater-Than Data Word.

7.3.1. Window Detector in Single-Ended Mode

Figure 7.5 shows two example window comparisons for Single-ended mode, with ADC2LT = 0x20 and ADC2GT = 0x10. In Single-ended mode, the codes vary from 0 to VREF x (255/256) and are represented as 8-bit unsigned integers. In the left example, an AD2WINT interrupt will be generated if the ADC2 conversion word (ADC2) is within the range defined by ADC2GT and ADC2LT (if 0x10 < ADC2 < 0x20). In the right example, and AD2WINT interrupt will be generated if ADC2 is outside of the range defined by ADC2GT and ADC2LT (if ADC2 < 0x10 or ADC2 > 0x20).

Table 12.1. CIP-51 Instruction Set Summary (Continued)

Mnemonic	Description	Bytes	Clock Cycles
JNZ rel	Jump if A does not equal zero	2	2/3
CJNE A, direct, rel	Compare direct byte to A and jump if not equal	3	3/4
CJNE A, #data, rel	Compare immediate to A and jump if not equal	3	3/4
CJNE Rn, #data, rel	Compare immediate to Register and jump if not equal	3	3/4
CJNE @Ri, #data, rel	Compare immediate to indirect and jump if not equal	3	4/5
DJNZ Rn, rel	Decrement Register and jump if not zero	2	2/3
DJNZ direct, rel	Decrement direct byte and jump if not zero	3	3/4
NOP	No operation	1	1

Notes on Registers, Operands and Addressing Modes:

Rn - Register R0-R7 of the currently selected register bank.

@Ri - Data RAM location addressed indirectly through R0 or R1.

rel - 8-bit, signed (two's complement) offset relative to the first byte of the following instruction. Used by SJMP and all conditional jumps.

direct - 8-bit internal data location's address. This could be a direct-access Data RAM location (0x00-0x7F) or an SFR (0x80-0xFF).

#data - 8-bit constant

#data16 - 16-bit constant

bit - Direct-accessed bit in Data RAM or SFR

addr11 - 11-bit destination address used by ACALL and AJMP. The destination must be within the same 2K-byte page of program memory as the first byte of the following instruction.

addr16 - 16-bit destination address used by LCALL and LJMP. The destination may be anywhere within the 64 kB program memory space.

There is one unused opcode (0xA5) that performs the same function as NOP.

SFR Definition 12.8. PSW: Program Status Word

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
CY	AC	F0	RS1	RS0	OV	F1	PARITY	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xD0
SFR Page: All Pages

Bit7: CY: Carry Flag.
This bit is set when the last arithmetic operation resulted in a carry (addition) or a borrow (subtraction). It is cleared to 0 by all other arithmetic operations.

Bit6: AC: Auxiliary Carry Flag
This bit is set when the last arithmetic operation resulted in a carry into (addition) or a borrow from (subtraction) the high order nibble. It is cleared to 0 by all other arithmetic operations.

Bit5: F0: User Flag 0.
This is a bit-addressable, general purpose flag for use under software control.

Bits4-3: RS1-RS0: Register Bank Select.
These bits select which register bank is used during register accesses.

RS1	RS0	Register Bank	Address
0	0	0	0x00–0x07
0	1	1	0x08–0x0F
1	0	2	0x10–0x17
1	1	3	0x18–0x1F

Bit2: OV: Overflow Flag.
This bit is set to 1 under the following circumstances:
- An ADD, ADDC, or SUBB instruction causes a sign-change overflow.
- A MUL instruction results in an overflow (result is greater than 255).
- A DIV instruction causes a divide-by-zero condition.

The OV bit is cleared to 0 by the ADD, ADDC, SUBB, MUL, and DIV instructions in all other cases.

Bit1: F1: User Flag 1.
This is a bit-addressable, general purpose flag for use under software control.

Bit0: PARITY: Parity Flag.
This bit is set to 1 if the sum of the eight bits in the accumulator is odd and cleared if the sum is even.

SFR Definition 12.15. EIP1: Extended Interrupt Priority 1

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	PCP2	PCP1	PCP0	PPCA0	PWADC0	PSMB0	PSPI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF6
SFR Page: All Pages

Bit7: Reserved.

Bit6: PCP2: Comparator2 (CP2) Interrupt Priority Control.
This bit sets the priority of the CP2 interrupt.
0: CP2 interrupt set to low priority level.
1: CP2 interrupt set to high priority level.

Bit5: PCP1: Comparator1 (CP1) Interrupt Priority Control.
This bit sets the priority of the CP1 interrupt.
0: CP1 interrupt set to low priority level.
1: CP1 interrupt set to high priority level.

Bit4: PCP0: Comparator0 (CP0) Interrupt Priority Control.
This bit sets the priority of the CP0 interrupt.
0: CP0 interrupt set to low priority level.
1: CP0 interrupt set to high priority level.

Bit3: PPCA0: Programmable Counter Array (PCA0) Interrupt Priority Control.
This bit sets the priority of the PCA0 interrupt.
0: PCA0 interrupt set to low priority level.
1: PCA0 interrupt set to high priority level.

Bit2: PWADC0: ADC0 Window Comparator Interrupt Priority Control.
This bit sets the priority of the ADC0 Window interrupt.
0: ADC0 Window interrupt set to low priority level.
1: ADC0 Window interrupt set to high priority level.

Bit1: PSMB0: System Management Bus (SMBus0) Interrupt Priority Control.
This bit sets the priority of the SMBus0 interrupt.
0: SMBus interrupt set to low priority level.
1: SMBus interrupt set to high priority level.

Bit0: PSPI0: Serial Peripheral Interface (SPI0) Interrupt Priority Control.
This bit sets the priority of the SPI0 interrupt.
0: SPI0 interrupt set to low priority level.
1: SPI0 interrupt set to high priority level.

13.7.1. Enable/Reset WDT

The watchdog timer is both enabled and reset by writing 0xA5 to the WDTCN register. The user's application software should include periodic writes of 0xA5 to WDTCN as needed to prevent a watchdog timer overflow. The WDT is enabled and reset as a result of any system reset.

13.7.2. Disable WDT

Writing 0xDE followed by 0xAD to the WDTCN register disables the WDT. The following code segment illustrates disabling the WDT:

```
CLR    EA            ; disable all interrupts
MOV    WDTCN,#0DEh   ; disable software watchdog timer
MOV    WDTCN,#0ADh
SETB   EA            ; re-enable interrupts
```

The writes of 0xDE and 0xAD must occur within 4 clock cycles of each other, or the disable operation is ignored. Interrupts should be disabled during this procedure to avoid delay between the two writes.

13.7.3. Disable WDT Lockout

Writing 0xFF to WDTCN locks out the disable feature. Once locked out, the disable operation is ignored until the next system reset. Writing 0xFF does not enable or reset the watchdog timer. Applications always intending to use the watchdog should write 0xFF to WDTCN in the initialization code.

13.7.4. Setting WDT Interval

WDTCN.[2:0] control the watchdog timeout interval. The interval is given by the following equation:

$4^{3 + WDTCN[2-0]} \times T_{sysclk}$; where T_{sysclk} is the system clock period.

For a 3 MHz system clock, this provides an interval range of 0.021 ms to 349.5 ms. WDTCN.7 must be logic 0 when setting this interval. Reading WDTCN returns the programmed interval. WDTCN.[2:0] reads 111b after a system reset.

14. Oscillators

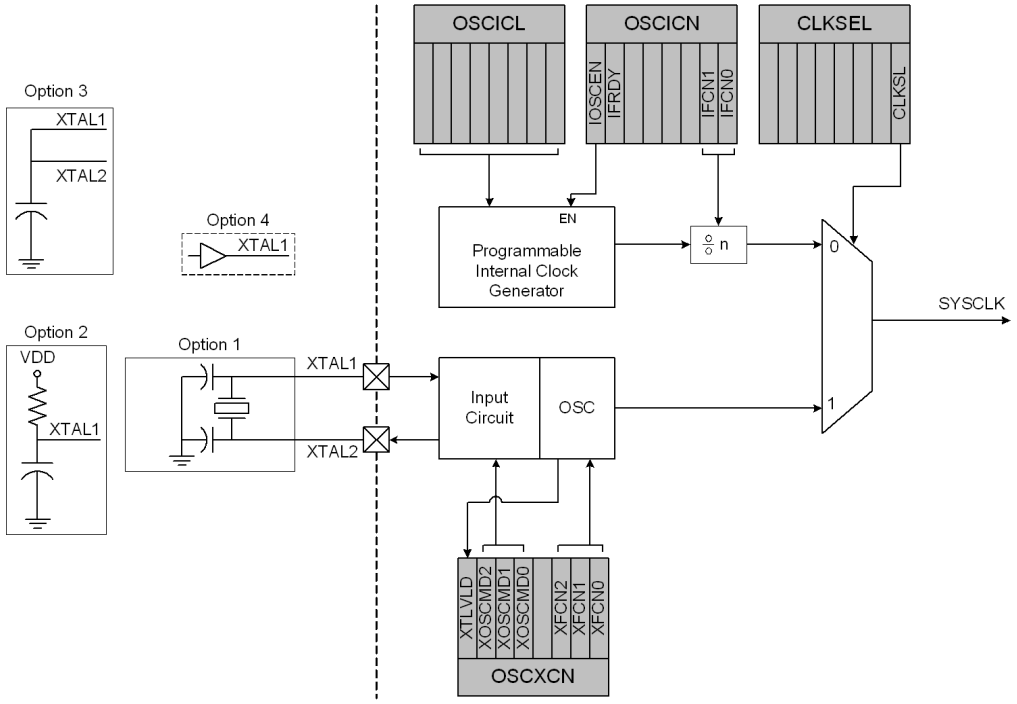


Figure 14.1. Oscillator Diagram

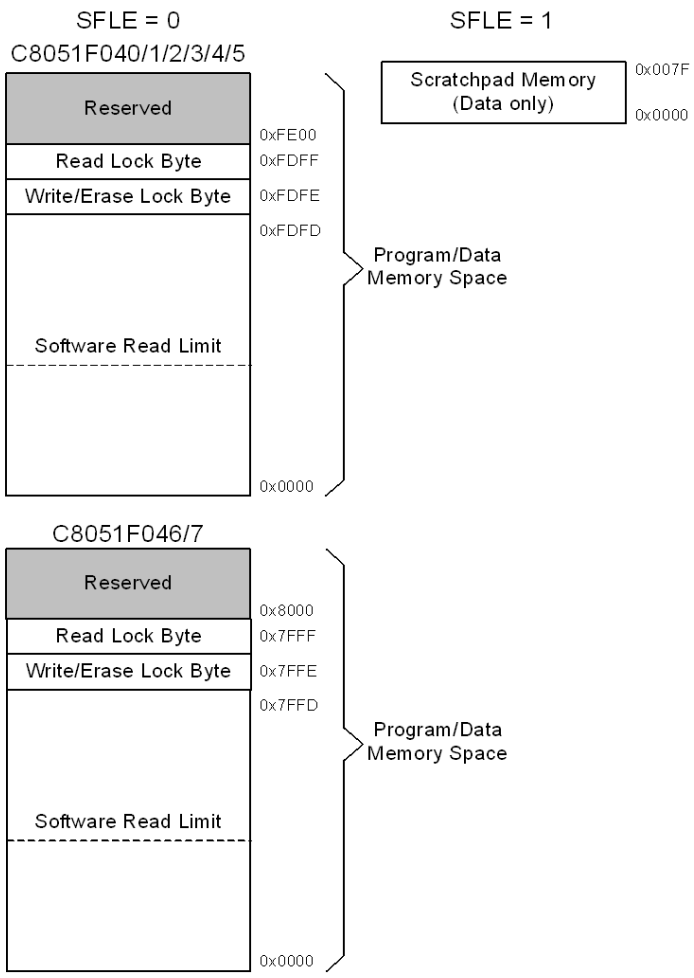
14.1. Programmable Internal Oscillator

All C8051F04x devices include a programmable internal oscillator that defaults as the system clock after a system reset. The internal oscillator period can be programmed via the OSCICL register as defined by SFR Definition 14.1. OSCICL is factory calibrated to obtain a 24.5 MHz frequency.

Electrical specifications for the precision internal oscillator are given in Table 14.1 on page 175. The programmed internal oscillator frequency must not exceed 25 MHz. The system clock may be derived from the programmed internal oscillator divided by 1, 2, 4, or 8, as defined by the IFCN bits in register OSCICN.

Read and Write/Erase Security Bits.
(Bit 7 is MSB.)

Bit	Memory Block	
	C8051F040/1/2/3/4/5	C8051F046/7
7	0xE000 - 0xFDFD	No effect
6	0xC000 - 0xDFFF	No effect
5	0xA000 - 0xBFFF	No effect
4	0x8000 - 0x9FFF	No effect
3	0x6000 - 0x7FFF	0x6000 - 0x7FFD
2	0x4000 - 0x5FFF	0x4000 - 0x5FFF
1	0x2000 - 0x3FFF	0x2000 - 0x3FFF
0	0x0000 - 0x1FFF	0x0000 - 0x1FFF



Flash Read Lock Byte

Bits7-0: Each bit locks a corresponding block of memory. (Bit7 is MSB).

0: Read operations are locked (disabled) for corresponding block across the JTAG interface.

1: Read operations are unlocked (enabled) for corresponding block across the JTAG interface.

Flash Write/Erase Lock Byte

Bits7-0: Each bit locks a corresponding block of memory.

0: Write/Erase operations are locked (disabled) for corresponding block across the JTAG interface.

1: Write/Erase operations are unlocked (enabled) for corresponding block across the JTAG interface.

NOTE: When the highest block is locked, the security bytes may be written but not erased.

Flash access Limit Register (FLACL)

The content of this register is used as the high byte of the 16-bit Software Read Limit address. This 16-bit read limit address value is calculated as 0xNN00 where NN is replaced by content of this register on reset. Software running at or above this address is prohibited from using the MOVX and MOVC instructions to read, write, or erase Flash locations below this address. Any attempts to read locations below this limit will return the value 0x00.

Figure 15.1. Flash Program Memory Map and Security Bytes

SFR Definition 16.3. EMI0TC: External Memory Timing Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EAS1	EAS0	ERW3	EWR2	EWR1	EWR0	EAH1	EAH0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA1
SFR Page: 0

Bits7-6: EAS1-0: EMIF Address Setup Time Bits.
00: Address setup time = 0 SYSCLK cycles.
01: Address setup time = 1 SYSCLK cycle.
10: Address setup time = 2 SYSCLK cycles.
11: Address setup time = 3 SYSCLK cycles.

Bits5-2: EWR3-0: EMIF /WR and /RD Pulse-Width Control Bits.
0000: /WR and /RD pulse width = 1 SYSCLK cycle.
0001: /WR and /RD pulse width = 2 SYSCLK cycles.
0010: /WR and /RD pulse width = 3 SYSCLK cycles.
0011: /WR and /RD pulse width = 4 SYSCLK cycles.
0100: /WR and /RD pulse width = 5 SYSCLK cycles.
0101: /WR and /RD pulse width = 6 SYSCLK cycles.
0110: /WR and /RD pulse width = 7 SYSCLK cycles.
0111: /WR and /RD pulse width = 8 SYSCLK cycles.
1000: /WR and /RD pulse width = 9 SYSCLK cycles.
1001: /WR and /RD pulse width = 10 SYSCLK cycles.
1010: /WR and /RD pulse width = 11 SYSCLK cycles.
1011: /WR and /RD pulse width = 12 SYSCLK cycles.
1100: /WR and /RD pulse width = 13 SYSCLK cycles.
1101: /WR and /RD pulse width = 14 SYSCLK cycles.
1110: /WR and /RD pulse width = 15 SYSCLK cycles.
1111: /WR and /RD pulse width = 16 SYSCLK cycles.

Bits1-0: EAH1-0: EMIF Address Hold Time Bits.
00: Address hold time = 0 SYSCLK cycles.
01: Address hold time = 1 SYSCLK cycle.
10: Address hold time = 2 SYSCLK cycles.
11: Address hold time = 3 SYSCLK cycles.

16.6.2.2.8-bit MOVX without Bank Select: EMI0CF[4:2] = ‘001’ or ‘011’.

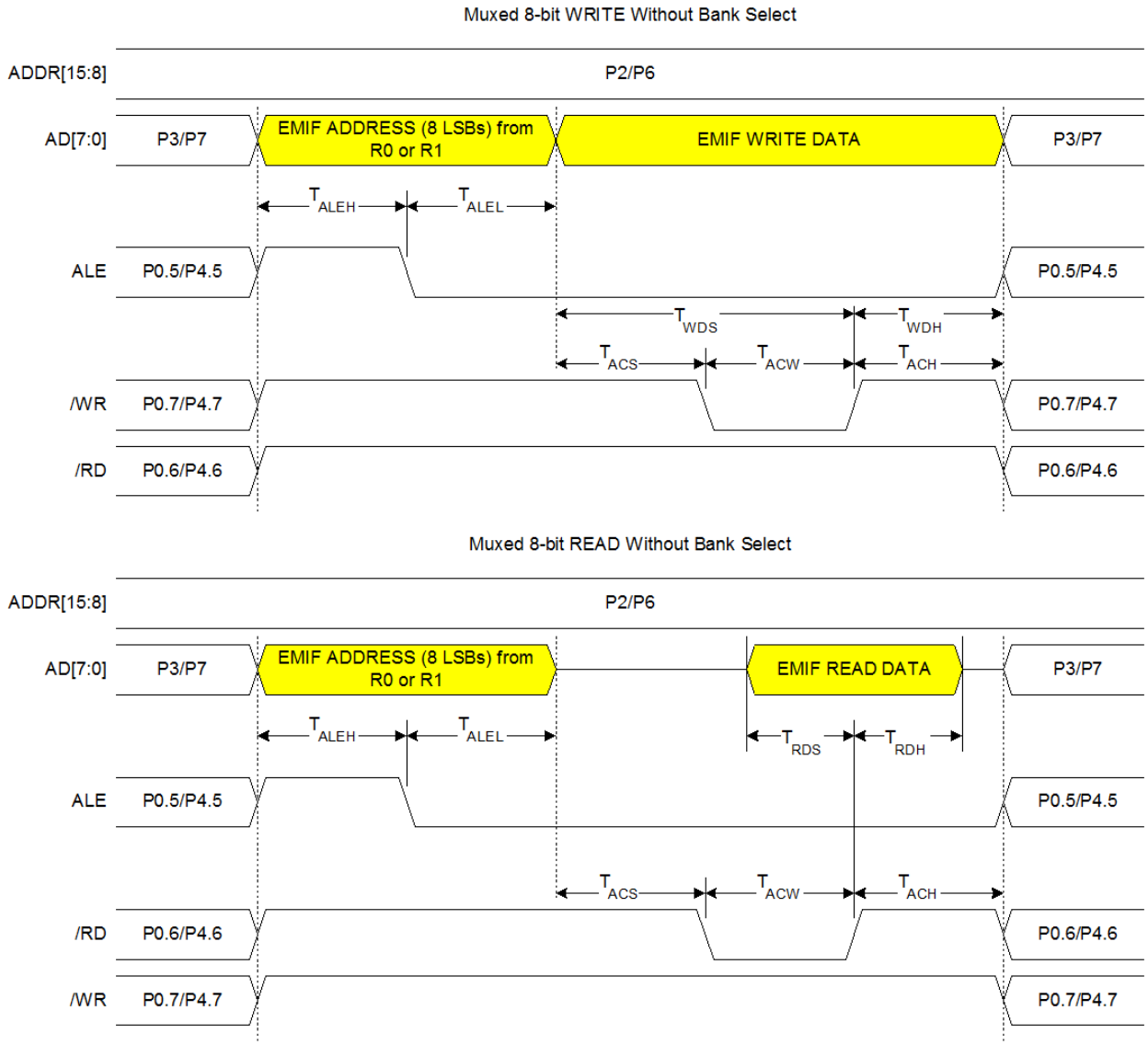


Figure 16.8. Multiplexed 8-bit MOVX without Bank Select Timing

a digital input by setting P3MDOUT.7 to a logic 0, which selects open-drain output mode, and P3.7 to a logic 1, which disables the low-side output driver.

If the Port pin has been assigned to a digital peripheral by the Crossbar and that pin functions as an input (for example RX0, the UART0 receive pin), then the output drivers on that pin are automatically disabled.

17.1.4. Weak Pullups

By default, each Port pin has an internal weak pullup device enabled which provides a resistive connection (about 100 kΩ) between the pin and V_{DD}. The weak pullup devices can be globally disabled by writing a logic 1 to the Weak Pullup Disable bit, (WEAKPUD, XBR2.7). The weak pullup is automatically deactivated on any pin that is driving a logic 0; that is, an output pin will not contend with its own pullup device. The weak pullup device can also be explicitly disabled on Ports 1, 2, and 3 pin by configuring the pin as an Analog Input, as described below.

17.1.5. Configuring Port 1, 2, and 3 Pins as Analog Inputs

The pins on Port 1 can serve as analog inputs to the ADC2 analog MUX (C8051F040/1/2/3 only), the pins on Port 2 can serve as analog inputs to the Comparators, and the pins on Port 3 can serve as inputs to ADC0. A Port pin is configured as an Analog Input by writing a logic 0 to the associated bit in the PnMDIN registers. All Port pins default to a Digital Input mode. Configuring a Port pin as an analog input:

1. Disables the digital input path from the pin. This prevents additional power supply current from being drawn when the voltage at the pin is near V_{DD} / 2. A read of the Port Data bit will return a logic 0 regardless of the voltage at the Port pin.
2. Disables the weak pullup device on the pin.
3. Causes the Crossbar to “skip over” the pin when allocating Port pins for digital peripherals, except for P2.0-P2.1.

Note that the output drivers on a pin configured as an Analog Input are not explicitly disabled. Therefore, the associated PnMDOUT bits of pins configured as Analog Inputs should explicitly be set to logic 0 (Open-Drain output mode), and the associated Port Data bits should be set to logic 1 (high-impedance). Also note that it is not required to configure a Port pin as an Analog Input in order to use it as an input to the ADC’s or Comparators; however, it is strongly recommended. See the analog peripheral’s corresponding section in this datasheet for further information.

SFR Definition 18.3. CAN0CN: CAN Control

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
*	*	*	CANIF	*	*	*	*	
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF8
SFR Page: 1

Bit 4: CANIF: CAN Interrupt Flag. Write = don't care.
0: CAN interrupt has not occurred.
1: CAN interrupt has occurred and is active.

CANIF is controlled by the CAN controller and is cleared by hardware once all interrupt conditions have been cleared in the CAN controller. See Section 3.4.1 in the *Bosch CAN User's Guide* (page 24) for more information concerning CAN controller interrupts.

***All CAN registers' functions/definitions are listed and described in the Bosch CAN User's Guide with the exception of the CANIF bit.**

This register may be accessed directly in the CIP-51 SFR register space, or through the indirect, index method (See Section "**18.2.5. Using CAN0ADR, CAN0DATH, and CANDATL to Access CAN Registers**" on page **232**).

SFR Definition 18.4. CAN0TST: CAN Test

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Please see the Bosch CAN User's Guide for a complete definition of this register								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xDB
SFR Page: 1

All CAN registers' functions/definitions are listed and described in the Bosch CAN User's Guide.
This register may be accessed directly in the CIP-51 SFR register space, or through the indirect, index method (See Section "**18.2.5. Using CAN0ADR, CAN0DATH, and CANDATL to Access CAN Registers**" on page **232**).

21.1.4. Mode 3: 9-Bit UART, Variable Baud Rate

Mode 3 uses the Mode 2 transmission protocol with the Mode 1 baud rate generation. Mode 3 operation transmits 11 bits: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The baud rate is derived from Timer 1 or Timer 2, 3, or 4 overflows, as defined by Equation 21.1 and Equation 21.3. Multiprocessor communications and hardware address recognition are supported, as described in **Section 21.2**.

21.2. Multiprocessor Communications

Modes 2 and 3 support multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit and the built-in UART0 address recognition hardware. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0. UART0 will recognize as “valid” (i.e., capable of causing an interrupt) **two** types of addresses: (1) a *masked* address and (2) a *broadcast* address **at any given time**. Both are described below.

23.2.3. Auto-Reload Mode

In Auto-Reload Mode, the counter/timer can be configured to count up or down and cause an interrupt/flag to occur upon an overflow/underflow event. When counting up, the counter/timer will set its overflow/underflow flag (TFn) and cause an interrupt (if enabled) upon overflow/underflow, the values in the Reload/Capture Registers (RCAPnH and RCAPnL) are loaded into the timer, and the timer is restarted. When the Timer External Enable Bit (EXENn) bit is set to '1' and the Decrement Enable Bit (DCEN) is '0', a '1'-to-'0' transition on the TnEX pin (configured as an input in the digital crossbar) will cause a timer reload (in addition to timer overflows causing auto-reloads). When DCEN is set to '1', the state of the TnEX pin controls whether the counter/timer counts *up* (increments) or *down* (decrements), and will not cause an auto-reload or interrupt event. See **Section 23.2.1** for information concerning configuration of a timer to count down.

When counting down, the counter/timer will set its overflow/underflow flag (TFn) and cause an interrupt (if enabled) when the value in the timer (TMRnH and TMRnL registers) matches the 16-bit value in the Reload/Capture Registers (RCAPnH and RCAPnL). This is considered an underflow event, and will cause the timer to load the value 0xFFFF. The timer is automatically restarted when an underflow occurs.

Counter/Timer with Auto-Reload mode is selected by clearing the CP/RLn bit. Setting TRn to logic 1 enables and starts the timer.

In Auto-Reload Mode, the External Flag (EXFn) toggles upon every overflow or underflow and does not cause an interrupt. The EXFn flag can be thought of as the most significant bit (MSB) of a 17-bit counter.

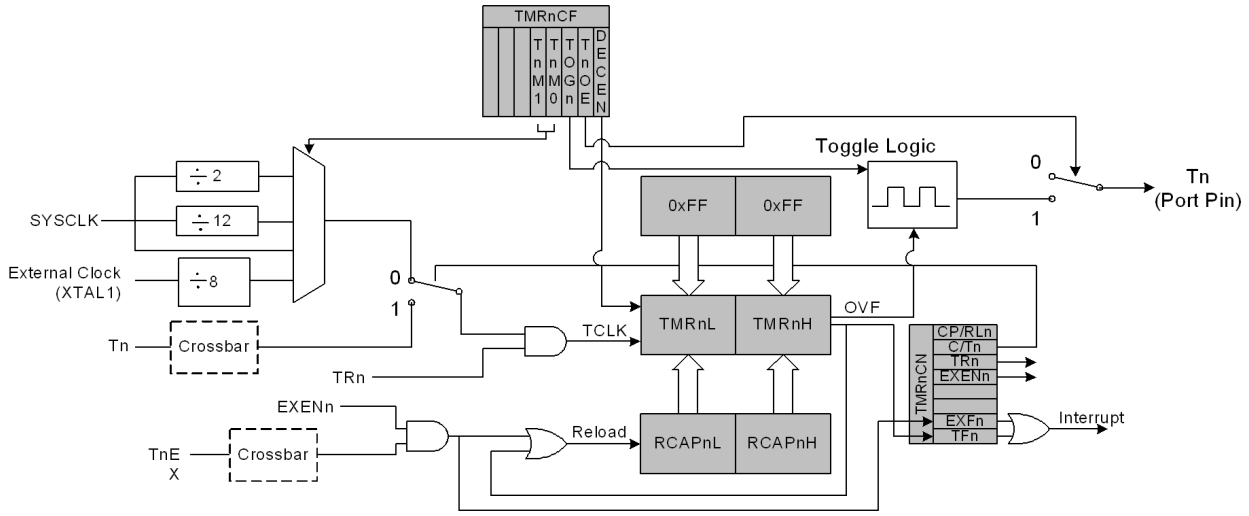


Figure 23.5. Tn Auto-reload Mode and Toggle Mode Block Diagram

JTAG Register Definition 25.3. FLASHCON: JTAG Flash Control Register

								Reset Value
SFLE	WRMD2	WRMD1	WRMD0	RDMD3	RDMD2	RDMD1	RDMD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

This register determines how the Flash interface logic will respond to reads and writes to the FLASHDAT Register.

Bit 7: SFLE: Scratchpad Flash Memory Access Enable
When this bit is set, Flash reads and writes from user software are directed to the 128-byte scratchpad Flash sector. When accessing the scratchpad, Flash accesses out of the address range 0x00-0x7F should not be attempted. Reads/Writes outside of this range will yield undefined results.
0: Flash access is directed to the Program/Data Flash sector.
1: Flash access is directed to the 128-byte scratchpad sector.

Bits6-4: WRMD2-0: Write Mode Select Bits.
The Write Mode Select Bits control how the interface logic responds to writes to the FLASHDAT Register per the following values:
000: A FLASHDAT write replaces the data in the FLASHDAT register, but is otherwise ignored.
001: A FLASHDAT write initiates a write of FLASHDAT into the memory address by the FLASHADR register. FLASHADR is incremented by one when complete.
010: A FLASHDAT write initiates an erasure (sets all bytes to 0xFF) of the Flash page containing the address in FLASHADR. The data written must be 0xA5 for the erase to occur. FLASHADR is not affected. If FLASHADR targets the Read Lock Byte or the Write/Erase Lock Byte, the entire user space will be erased (i.e. entire Flash memory except for the Reserved area (See **Section "15. Flash Memory" on page 179**).
(All other values for WRMD2-0 are reserved.)

Bits3-0: RDMD3-0: Read Mode Select Bits.
The Read Mode Select Bits control how the interface logic responds to reads to the FLASHDAT Register per the following values:
0000: A FLASHDAT read provides the data in the FLASHDAT register, but is otherwise ignored.
0001: A FLASHDAT read initiates a read of the byte addressed by the FLASHADR register if no operation is currently active. This mode is used for block reads.
0010: A FLASHDAT read initiates a read of the byte addressed by FLASHADR only if no operation is active and any data from a previous read has already been read from FLASHDAT. This mode allows single bytes to be read (or the last byte of a block) without initiating an extra read.
(All other values for RDMD3-0 are reserved.)