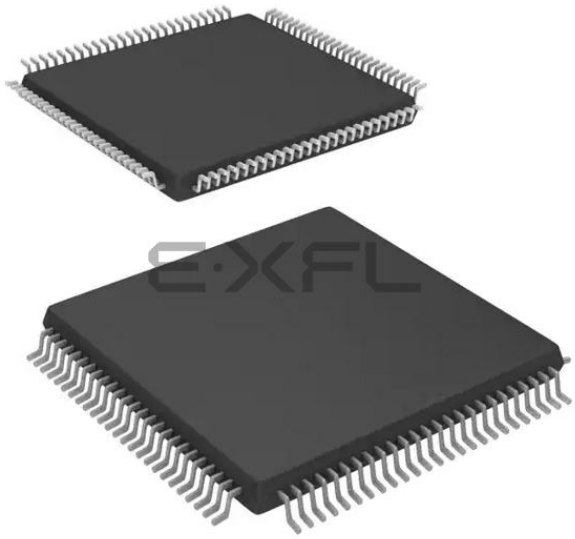

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 8x8b, 13x10b; D/A 2x10b, 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f042

Table of Contents

1.4. Programmable Digital I/O and Crossbar

The standard 8051 Ports (0, 1, 2, and 3) are available on the MCUs. The C8051F040/2/4/6 have 4 additional 8-bit ports (4, 5, 6, and 7) for a total of 64 general-purpose I/O Ports. The Ports behave like the standard 8051 with a few enhancements.

Each port pin can be configured as either a push-pull or open-drain output. Also, the "weak pullups" which are normally fixed on an 8051 can be globally disabled, providing additional power saving capabilities for low-power applications.

Perhaps the most unique enhancement is the Digital Crossbar. This is essentially a large digital switching network that allows mapping of internal digital system resources to Port I/O pins on P0, P1, P2, and P3 (See Figure 1.9). Unlike microcontrollers with standard multiplexed digital I/O ports, all combinations of functions are supported with all package options offered.

The on-chip counter/timers, serial buses, HW interrupts, ADC Start of Conversion input, comparator outputs, and other digital signals in the controller can be configured to appear on the Port I/O pins specified in the Crossbar Control registers. This allows the user to select the exact mix of general purpose Port I/O and digital resources needed for the particular application.

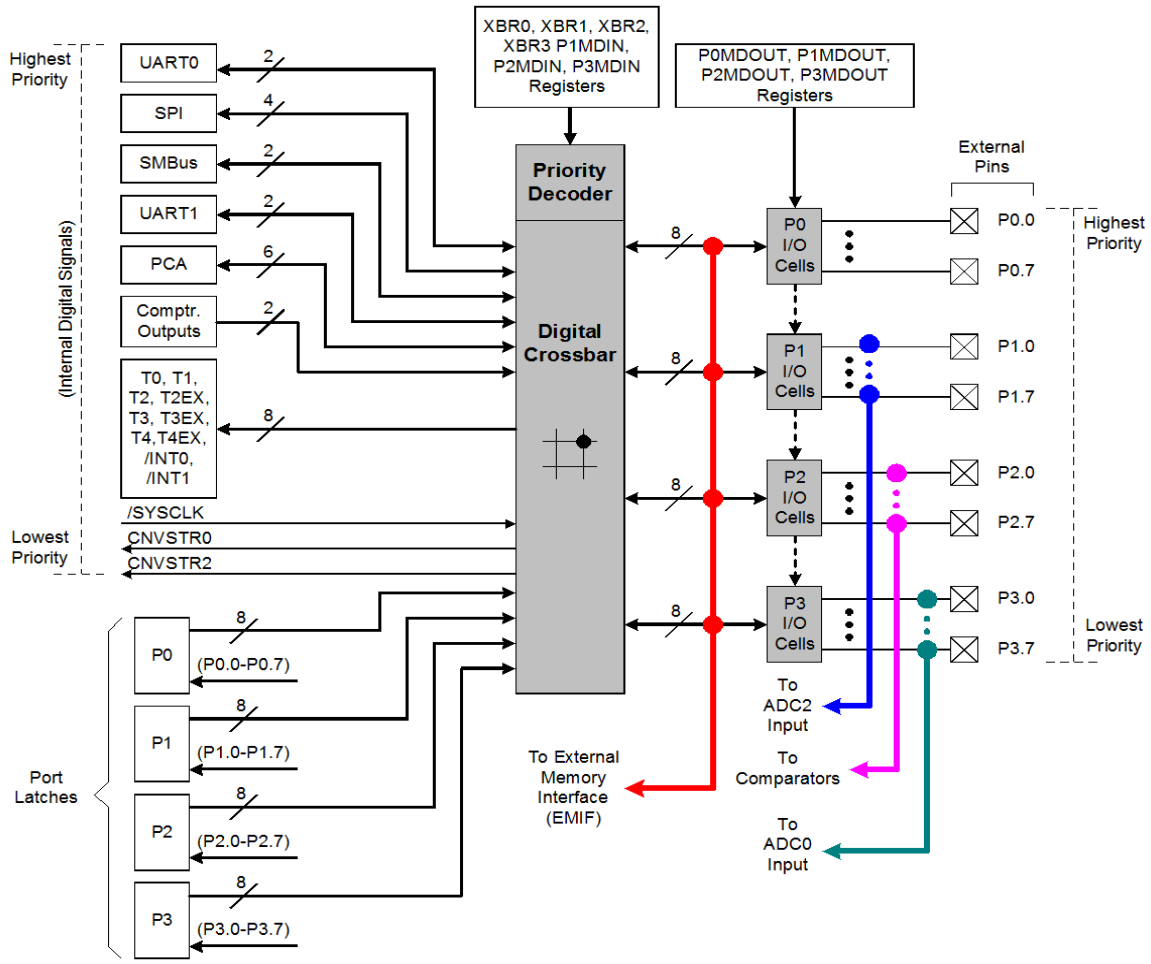

Figure 1.9. Digital Crossbar Diagram

SFR Definition 5.1. AMX0CF: AMUX0 Configuration

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	PORT3IC	HVDA2C	AIN23IC	AIN01IC	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	SFR Address:

SFR Address: 0xBA
SFR Page: 0

Bits7-4: UNUSED. Read = 0000b; Write = don't care
Bit3: PORT3IC: Port 3 even/odd Pin Input Pair Configuration Bit
0: Port 3 even and odd input channels are independent single-ended inputs
1: Port 3 even and odd input channels are (respectively) +, - difference input pair
Bit2: HVDA2C: HVDA 2's Compliment Bit
0: HVDA output measured as an independent single-ended input
1: HVDA result for 2's compliment value
Bit1: AIN23IC: AIN0.2, AIN0.3 Input Pair Configuration Bit
0: AIN0.2 and AIN0.3 are independent single-ended inputs
1: AIN0.2, AIN0.3 are (respectively) +, - difference input pair
Bit0: AIN01IC: AIN0.0, AIN0.1 Input Pair Configuration Bit
0: AIN0.0 and AIN0.1 are independent single-ended inputs
1: AIN0.0, AIN0.1 are (respectively) +, - difference input pair

NOTE: The ADC0 Data Word is in 2's complement format for channels configured as difference.

SFR Definition 5.2. AMX0SL: AMUX0 Channel Select

R	R	R	R	R/W	R/W	R/W	R/W	Reset Value
-	-	-	-	AMX0AD3	AMX0AD2	AMX0AD1	AMX0AD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBB
SFR Page: 0

Bits7-4: UNUSED. Read = 0000b; Write = don't care
Bits3-0: AMX0AD3-0: AMX0 Address Bits
0000-1111b: ADC Inputs selected per Table 5.1.

SFR Definition 5.3. AMX0PRT: Port 3 Pin Selection

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
PAIN7EN	PAIN6EN	PAIN5EN	PAIN4EN	PAIN3EN	PAIN2EN	PAIN1EN	PAIN0EN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xBD
SFR Page: 0

Bit7: PAIN7EN: Pin 7 Analog Input Enable Bit
0: P3.7 is not selected as an analog input to the AMUX.
1: P3.7 is selected as an analog input to the AMUX.

Bit6: PAIN6EN: Pin 6 Analog Input Enable Bit
0: P3.6 is not selected as an analog input to the AMUX.
1: P3.6 is selected as an analog input to the AMUX.

Bit5: PAIN5EN: Pin 5 Analog Input Enable Bit
0: P3.5 is not selected as an analog input to the AMUX.
1: P3.5 is selected as an analog input to the AMUX.

Bit4: PAIN4EN: Pin 4 Analog Input Enable Bit
0: P3.4 is not selected as an analog input to the AMUX.
1: P3.4 is selected as an analog input to the AMUX.

Bit3: PAIN3EN: Pin 3 Analog Input Enable Bit
0: P3.3 is not selected as an analog input to the AMUX.
1: P3.3 is enabled as an analog input to the AMUX.

Bit2: PAIN2EN: Pin 2 Analog Input Enable Bit
0: P3.2 is not selected as an analog input to the AMUX.
1: P3.2 is enabled as an analog input to the AMUX.

Bit1: PAIN1EN: Pin 1 Analog Input Enable Bit
0: P3.1 is not selected as an analog input to the AMUX.
1: P3.1 is enabled as an analog input to the AMUX.

Bit0: PAIN0EN: Pin 0 Analog Input Enable Bit
0: P3.0 is not selected as an analog input to the AMUX.
1: P3.0 is enabled as an analog input to the AMUX.

Note: Any number of Port 3 pins may be selected simultaneously inputs to the AMUX. Odd numbered and even numbered pins that are selected simultaneously are shorted together as “wired-OR”.

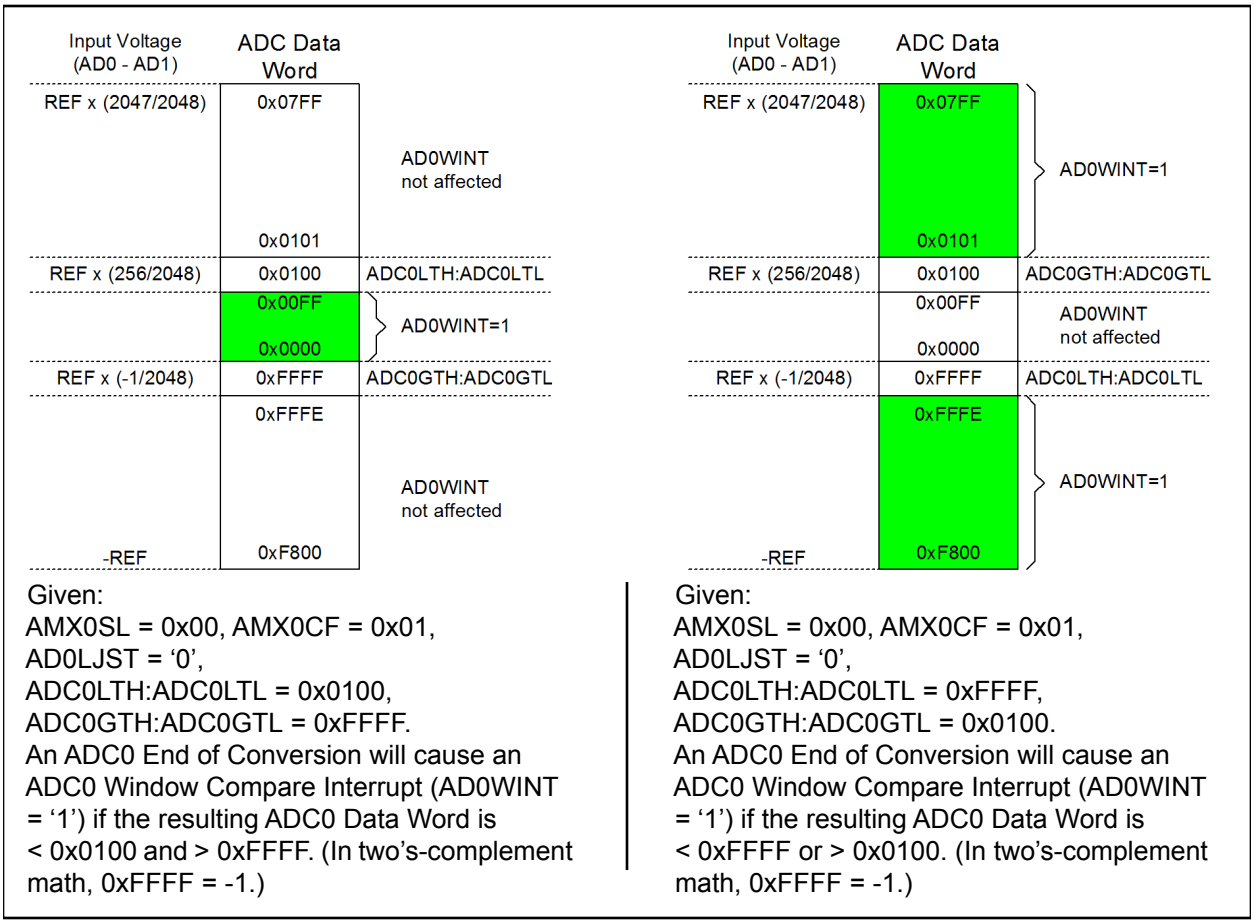

Figure 5.9. 12-Bit ADC0 Window Interrupt Example: Right Justified Differential Data

Table 6.1. AMUX Selection Chart (AMX0AD3-0 and AMX0CF3-0 bits)

		AMX0AD3-0								
		0000	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1xxx**
AMX0CF Bits 3-0	**0000**	AIN0.0	AIN0.1	AIN0.2	AIN0.3	HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0001	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0010	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0011	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	0101	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	0110	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	0111	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	1000	AIN0.0	AIN0.1	AIN0.2	AIN0.3	HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1001	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1010	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1011	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(HVDA) -(HVREF)		+P3EVEN -P3ODD)		TEMP SENSOR
	1101	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	+(HVDA) -(HVREF)		+P3EVEN -P3ODD		TEMP SENSOR
	1110	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		+P3EVEN -P3ODD		TEMP SENSOR
	1111	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		+P3EVEN -P3ODD		TEMP SENSOR

Note: “P3EVEN” denotes even numbered and “P3ODD” odd numbered Port 3 pins selected in the AMX0PRT register.

6.3.3. Settling Time Requirements

A minimum tracking time is required before an accurate conversion can be performed. This tracking time is determined by the ADC0 MUX resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion. Figure 6.5 shows the equivalent ADC0 input circuits for both Differential and Single-ended modes. Notice that the equivalent time constant for both input circuits is the same. The required settling time for a given settling accuracy (*SA*) may be approximated by Equation 6.2. When measuring the Temperature Sensor output, R_{TOTAL} reduces to R_{MUX}. Note that in low-power tracking mode, three SAR clocks are used for tracking at the start of every conversion. For most applications, these three SAR clocks will meet the tracking requirements. See Table 6.2 for absolute minimum settling/tracking time requirements.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

Equation 6.2. ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the ADC0 MUX resistance and any external source resistance.
n is the ADC resolution in bits (10).

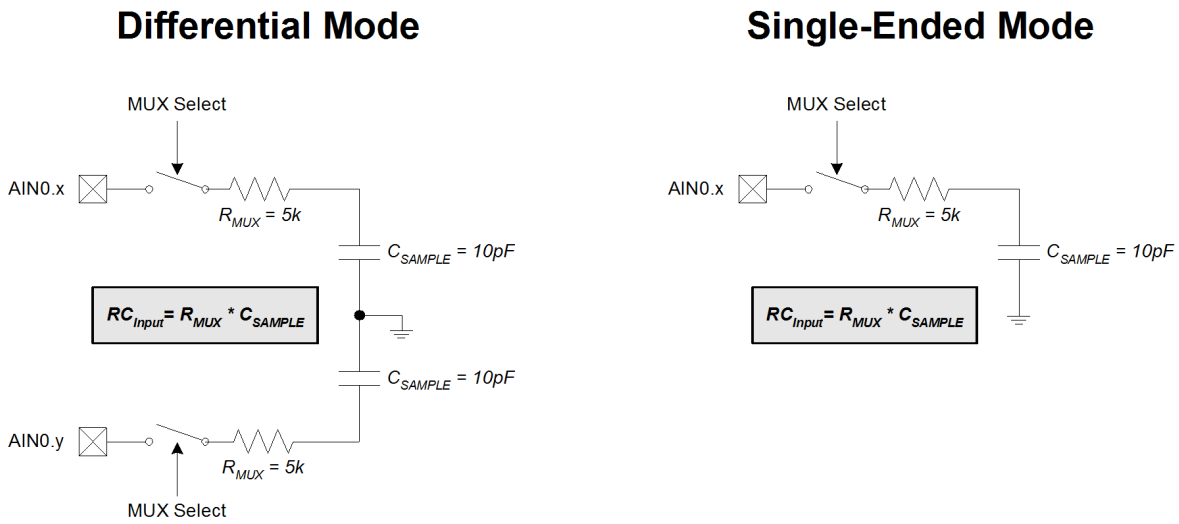

Figure 6.5. ADC0 Equivalent Input Circuits

Table 6.3. High-Voltage Difference Amplifier Electrical Characteristics

V_{DD} = 3.0 V, AV+ = 3.0 V, V_{REF} = 3.0 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Inputs					
Differential range	peak-to-peak	—	—	60	V
Common Mode Range	(HVAIN+) – (HVAIN–) = 0 V	–60	—	+60	V
Analog Output					
Output Voltage Range		0.1	—	2.9	V
DC Performance					
Common Mode Rejection Ratio	Vcm= –10 V to +10 V, Rs=0	44	52	—	dB
Offset Voltage		—	±3	—	mV
Noise	HVCAP floating	—	500	—	nV/rtHz
Nonlinearity	G = 1	—	72	—	dB
Dynamic Performance					
Small Signal Bandwidth	G = 0.05	—	3	—	MHz
Small Signal Bandwidth	G = 1	—	150	—	kHz
Slew Rate		—	2	—	V/µs
Settling Time	0.01%, G = 0.05, 10 V step	—	10	—	µs
Input/Output Impedance					
Differential (HVAIN+) input		—	105	—	kΩ
Differential (HVAIN–) input		—	98	—	kΩ
Common Mode input		—	51	—	kΩ
HVCAP		—	5	—	kΩ
Power Specification					
Quiescent Current		—	450	1000	µA

Table 12.2. Special Function Register (SFR) Memory Map (Continued)

ADDRESS	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	SFR PAGE
B0	P3 **(ALL PAGES)**							FLSCL FLACL	0 1 2 3 F
A8	IE **(ALL PAGES)**	SADDR0				P1MDIN	P2MDIN	P3MDIN	0 1 2 3 F
A0	P2 **(ALL PAGES)**	EMI0TC	EMI0CN	EMI0CF	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT	0 1 2 3 F
98	SCON0 SCON1	SBUF0 SBUF1	SPI0CFG	SPI0DAT	P4MDOUT	SPI0CKR P5MDOUT	P6MDOUT	P7MDOUT	0 1 2 3 F
90	P1 **(ALL PAGES)**	SSTA0					SFRPGCN	CLKSEL	0 1 2 3 F
88	TCON CPT0CN CPT1CN CPT2CN	TMOD CPT0MD CPT1MD CPT2MD	TL0 OSCICN	TL1 OSCICL	TH0 OSCXCN	TH1	CKCON	PSCTL	0 1 2 3 F
80	P0 **(ALL PAGES)**	SP **(ALL PAGES)**	DPL **(ALL PAGES)**	DPH **(ALL PAGES)**	SFRPAGE **(ALL PAGES)**	SFRNEXT **(ALL PAGES)**	SFRLAST **(ALL PAGES)**	PCON **(ALL PAGES)**	0 1 2 3 F
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	

13. Reset Sources

Reset circuitry allows the controller to be easily placed in a predefined default condition. On entry to this reset state, the following occur:

- CIP-51 halts program execution
- Special Function Registers (SFRs) are initialized to their defined reset values
- External port pins are forced to a known state
- Interrupts and timers are disabled.

All SFRs are reset to the predefined values noted in the SFR detailed descriptions. The contents of internal data memory are unaffected during a reset; any previously stored data is preserved. However, since the stack pointer SFR is reset, the stack is effectively lost even though the data on the stack are not altered.

The I/O port latches are reset to 0xFF (all logic 1s), activating internal weak pullups which take the external I/O pins to a high state. For V_{DD} Monitor resets, the /RST pin is driven low until the end of the V_{DD} reset timeout.

On exit from the reset state, the program counter (PC) is reset, and the system clock defaults to the internal oscillator running at its lowest frequency. Refer to Section "**14. Oscillators**" on page **173** for information on selecting and configuring the system clock source. The Watchdog Timer is enabled using its longest timeout interval (see Section "**13.7. Watchdog Timer Reset**" on page **167**). Once the system clock source is stable, program execution begins at location 0x0000.

There are seven sources for putting the MCU into the reset state: power-on, power-fail, external /RST pin, external CNVSTR0 signal, software command, Comparator0, Missing Clock Detector, and Watchdog Timer. Each reset source is described in the following sections.

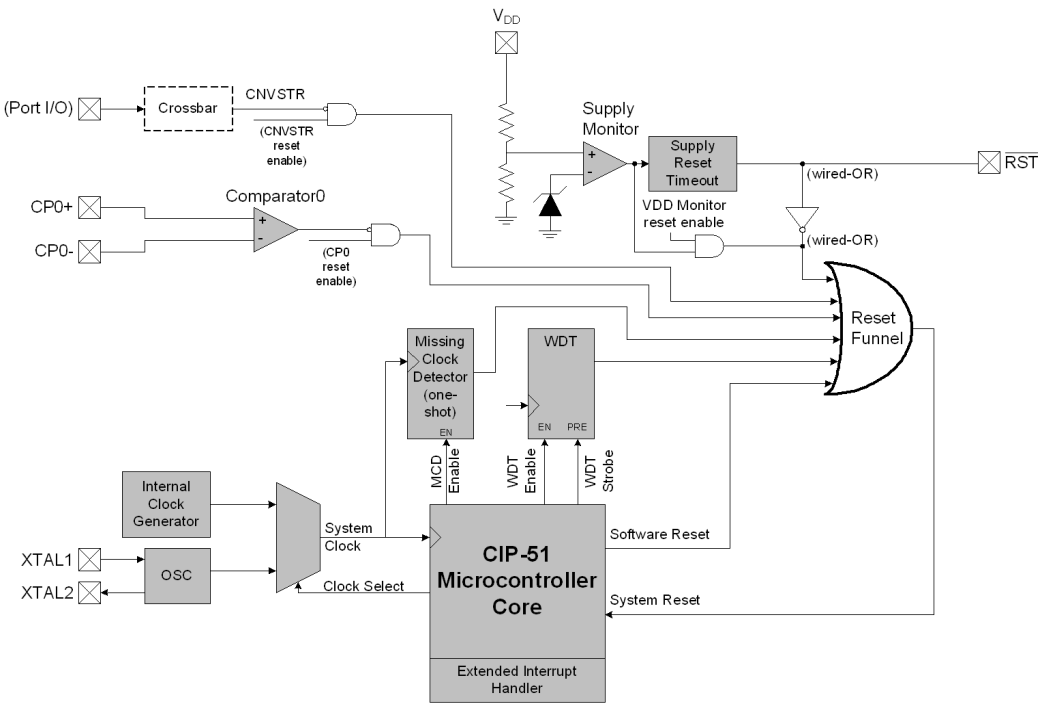

Figure 13.1. Reset Sources

13.1. Power-On Reset

The C8051F04x family incorporates a power supply monitor that holds the MCU in the reset state until V_{DD} rises above the V_{RST} level during power-up. See Figure 13.2 for timing diagram, and refer to Table 13.1 for the Electrical Characteristics of the power supply monitor circuit. The /RST pin is asserted low until the end of the 100 ms V_{DD} Monitor timeout in order to allow the V_{DD} supply to stabilize. The V_{DD} Monitor reset is enabled and disabled using the external V_{DD} monitor enable pin (MONEN).

On exit from a power-on reset, the PORSF flag (RSTSRC.1) is set by hardware to logic 1. All of the other reset flags in the RSTSRC register are indeterminate. PORSF is cleared by all other resets. Since all resets cause program execution to begin at the same location (0x0000), software can read the PORSF flag to determine if a power-up was the cause of reset. The contents of internal data memory should be assumed to be undefined after a power-on reset.

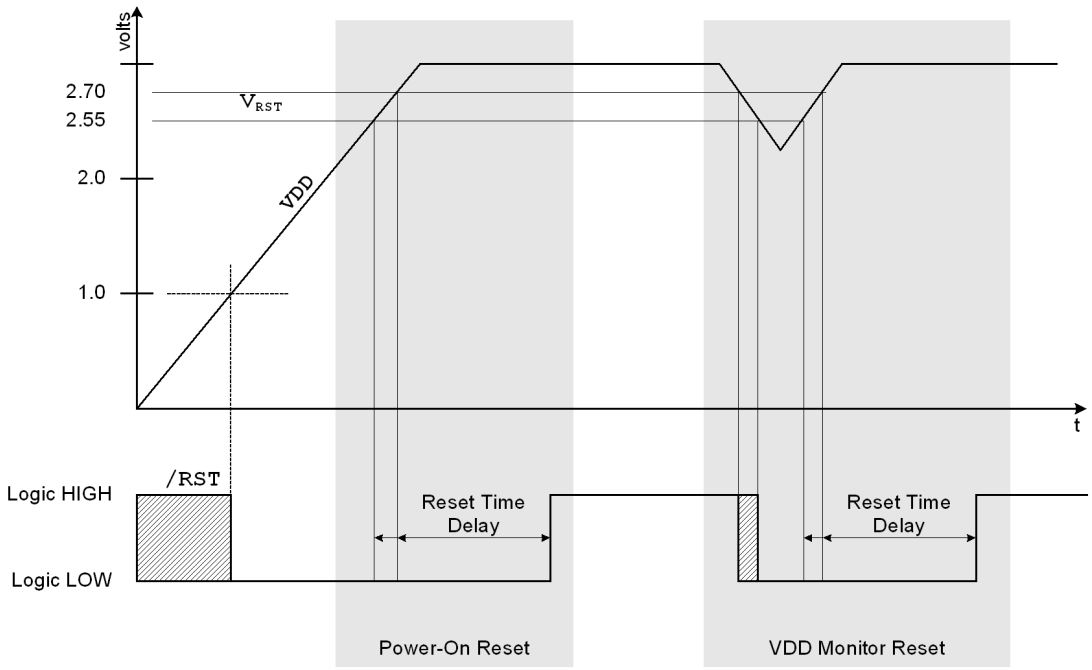

Figure 13.2. Reset Timing

13.2. Power-Fail Reset

When a power-down transition or power irregularity causes V_{DD} to drop below V_{RST}, the power supply monitor will drive the /RST pin low and return the CIP-51 to the reset state. When V_{DD} returns to a level above V_{RST}, the CIP-51 will leave the reset state in the same manner as that for the power-on reset (see Figure 13.2). Note that even though internal data memory contents are not altered by the power-fail reset, it is impossible to determine if V_{DD} dropped below the level required for data retention. If the PORSF flag is set to logic 1, the data may no longer be valid.

13.3. External Reset

The external /RST pin provides a means for external circuitry to force the MCU into a reset state. Asserting the /RST pin low will cause the MCU to enter the reset state. It may be desirable to provide an external pul-

15.3.1. Summary of Flash Security Options

There are three Flash access methods supported on the C8051F04x devices; 1) Accessing Flash through the JTAG debug interface, 2) Accessing Flash from firmware residing below the Flash Access Limit, and 3) Accessing Flash from firmware residing at or above the Flash Access Limit.

Accessing Flash through the JTAG debug interface:

1. The Read and Write/Erase Lock bytes (security bytes) provide security for Flash access through the JTAG interface.
2. Any unlocked page may be read from, written to, or erased.
3. Locked pages cannot be read from, written to, or erased.
4. Reading the security bytes is always permitted.
5. Locking additional pages by writing to the security bytes is always permitted.
6. If the page containing the security bytes is **unlocked**, it can be directly erased. **Doing so will reset the security bytes and unlock all pages of Flash.**
7. If the page containing the security bytes is **locked**, it cannot be directly erased. **To unlock the page containing the security bytes, a full JTAG device erase is required.** A full JTAG device erase will erase all Flash pages, including the page containing the security bytes and the security bytes themselves.
8. The Reserved Area cannot be read from, written to, or erased at any time.

Accessing Flash from firmware residing below the Flash Access Limit:

1. The Read and Write/Erase Lock bytes (security bytes) do not restrict Flash access from user firmware.
2. Any page of Flash except the page containing the security bytes may be read from, written to, or erased.
3. **The page containing the security bytes cannot be erased.** Unlocking pages of Flash can only be performed via the JTAG interface.
4. The page containing the security bytes may be read from or written to. Pages of Flash can be locked from JTAG access by writing to the security bytes.
5. The Reserved Area cannot be read from, written to, or erased at any time.

Accessing Flash from firmware residing at or above the Flash Access Limit:

1. The Read and Write/Erase Lock bytes (security bytes) do not restrict Flash access from user firmware.
2. Any page of Flash at or above the Flash Access Limit except the page containing the security bytes may be read from, written to, or erased.
3. Any page of Flash below the Flash Access Limit cannot be read from, written to, or erased.
4. Code branches to locations below the Flash Access Limit are permitted.
5. **The page containing the security bytes cannot be erased.** Unlocking pages of Flash can only be performed via the JTAG interface.
6. The page containing the security bytes may be read from or written to. Pages of Flash can be locked from JTAG access by writing to the security bytes.
7. The Reserved Area cannot be read from, written to, or erased at any time.

16.2. Configuring the External Memory Interface

Configuring the External Memory Interface consists of five steps:

1. Select EMIF on Low Ports (P3, P2, P1, and P0) or High Ports (P7, P6, P5, and P4).
2. Configure the Output Modes of the port pins as either push-pull or open-drain.
3. Select Multiplexed mode or Non-multiplexed mode.
4. Select the memory mode (on-chip only, split mode without bank select, split mode with bank select, or off-chip only).
5. Set up timing to interface with off-chip memory or peripherals.

Each of these five steps is explained in detail in the following sections. The Port selection, Multiplexed mode selection, and Mode bits are located in the EMI0CF register shown in SFR Definition 16.2.

16.3. Port Selection and Configuration

The External Memory Interface can appear on Ports 3, 2, 1, and 0 (C8051F04x devices) or on Ports 7, 6, 5, and 4 (C8051F040/2/4/6 devices only), depending on the state of the PRTSEL bit (EMI0CF.5). If the lower Ports are selected, the EMIFLE bit (XBR2.1) must be set to a '1' so that the Crossbar will skip over P0.7 (/WR), P0.6 (/RD), and, if multiplexed mode is selected, P0.5 (ALE). For more information about the configuring the Crossbar, see **Section "17.1. Ports 0 through 3 and the Priority Crossbar Decoder" on page 204**.

The External Memory Interface claims the associated Port pins for memory operations ONLY during the execution of an off-chip MOVX instruction. Once the MOVX instruction has completed, control of the Port pins reverts to the Port latches or to the Crossbar (on Ports 3, 2, 1, and 0). See **Section "17. Port Input/ Output" on page 203** for more information about the Crossbar and Port operation and configuration. **The Port latches should be explicitly configured as push-pull to 'park' the External Memory Interface pins in a dormant state, most commonly by setting them to a logic 1**.

During the execution of the MOVX instruction, the External Memory Interface will explicitly disable the drivers on all Port pins that are acting as Inputs (Data[7:0] during a READ operation, for example). The Output mode of the Port pins (whether the pin is configured as Open-Drain or Push-Pull) is unaffected by the External Memory Interface operation, and remains controlled by the PnMDOUT registers. In most cases, the output modes of all EMIF pins should be configured for push-pull mode. See **Section "17.1.2. Configuring the Output Modes of the Port Pins" on page 206**.

16.6.2.3.8-bit MOVX with Bank Select: EMI0CF[4:2] = '010'.

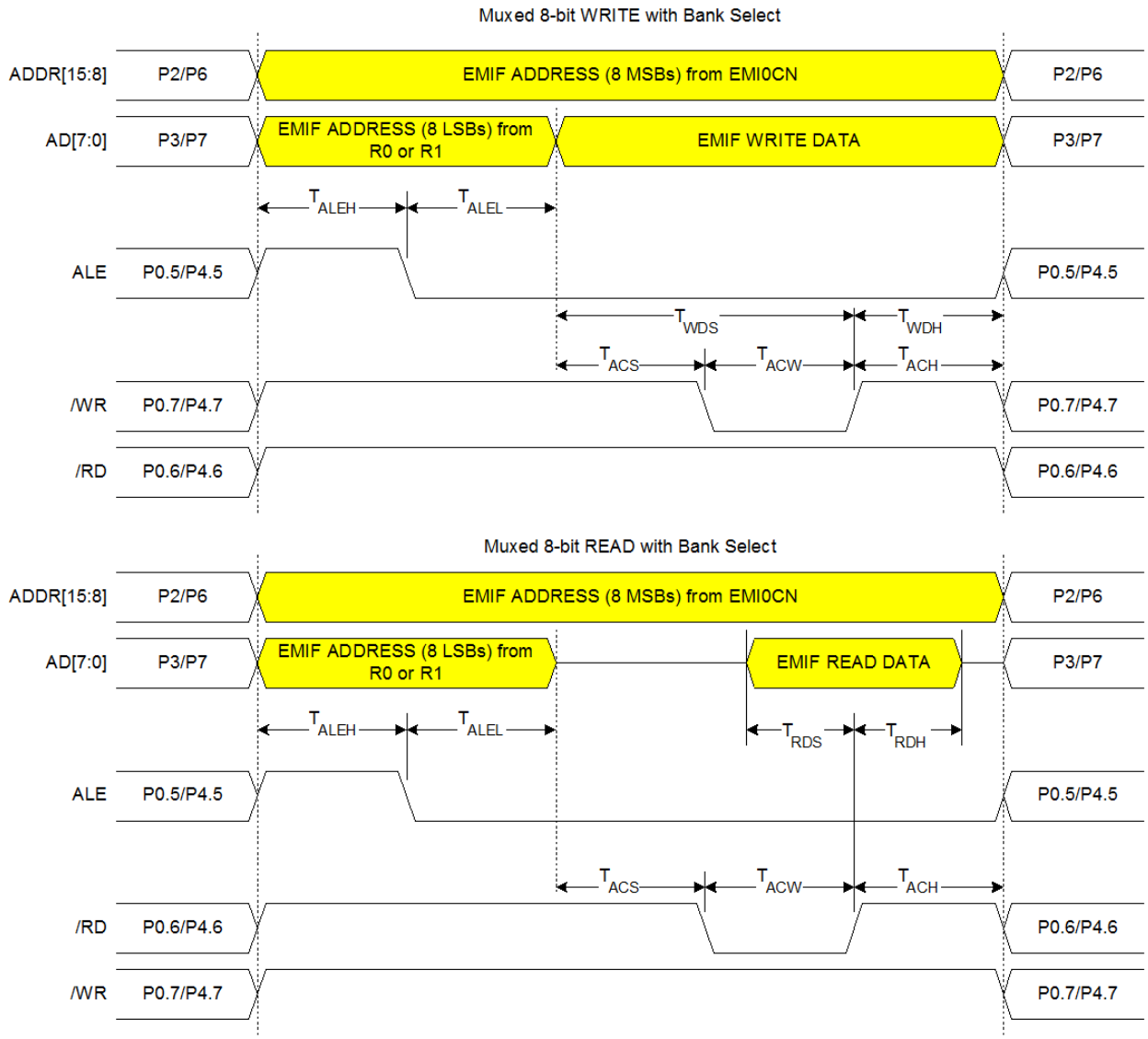

Figure 16.9. Multiplexed 8-bit MOVX with Bank Select Timing

SFR Definition 17.4. XBR3: Port I/O Crossbar Register 3

R/W	R	R	R	R/W	R/W	R/W	R/W	Reset Value
CTXOUT	—	—	—	CP2E	CNVST2E	T3EXE	T3E	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xE4
SFR Page: F

Bit7: CTXOUT: CAN Transmit Pin (CTX) Output Mode.
0: CTX pin output mode is configured as open-drain.
1: CTX pin output mode is configured as push-pull.
Bit6-4: Reserved
Bit3: CP2E: CP2 Output Enable Bit.
0: CP2 unavailable at Port pin.
1: CP2 routed to Port pin.
Bit2: CNVST2E: ADC2 External Convert Start Input Enable Bit (C8051F040/1/2/3 only).
0: CNVST2 for ADC2 unavailable at Port pin.
1: CNVST2 for ADC2 routed to Port pin.
Bit1: T3EXE: T3EX Input Enable Bit.
0: T3EX unavailable at Port pin.
1: T3EX routed to Port pin.
Bit0: T3E: T3 Input Enable Bit.
0: T3 unavailable at Port pin.
1: T3 routed to Port pin.

SFR Definition 17.5. P0: Port0 Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x80
SFR Page: All Pages

Bits7-0: P0.[7:0]: Port0 Output Latch Bits.
(Write - Output appears on I/O pins per XBR0, XBR1, XBR2, and XBR3 Registers)
0: Logic Low Output.
1: Logic High Output (open if corresponding P0MDOUT.n bit = 0).
(Read - Regardless of XBR0, XBR1, XBR2, and XBR3 Register settings).
0: P0.n pin is logic low.
1: P0.n pin is logic high.

Note: P0.7 (/WR), P0.6 (/RD), and P0.5 (ALE) can be driven by the External Data Memory Interface. See **Section "16. External Data Memory Interface and On-Chip XRAM" on page 187** for more information. See also SFR Definition 17.3 for information about configuring the Crossbar for External Memory accesses.

17.2.1. Configuring Ports Which are Not Pinned Out

Although P4, P5, P6, and P7 are not brought out to pins on the C8051F041/3/5/7 devices, the Port Data registers are still present and can be used by software. Because the digital input paths also remain active, it is recommended that these pins not be left in a ‘floating’ state in order to avoid unnecessary power dissipation arising from the inputs floating to non-valid logic levels. This condition can be prevented by any of the following:

1. Leave the weak pullup devices enabled by setting WEAKPUD (XBR2.7) to a logic 0.
2. Configure the output modes of P4, P5, P6, and P7 to “Push-Pull” by writing PnOUT = 0xFF.
3. Force the output states of P4, P5, P6, and P7 to logic 0 by writing zeros to the Port Data registers: P4 = 0x00, P5 = 0x00, P6= 0x00, and P7 = 0x00.

17.2.2. Configuring the Output Modes of the Port Pins

The output mode of each port pin can be configured to be either Open-Drain or Push-Pull. In the Push-Pull configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to be driven to V_{DD}. In the Open-Drain configuration, a logic 0 in the associated bit in the Port Data register will cause the Port pin to be driven to GND, and a logic 1 will cause the Port pin to assume a high-impedance state. The Open-Drain configuration is useful to prevent contention between devices in systems where the Port pin participates in a shared interconnection in which multiple outputs are connected to the same physical wire.

The output modes of the Port pins on Ports 4 through 7 are determined by the bits in their respective PnMDOUT Output Mode Registers. Each bit in PnMDOUT controls the output mode of its corresponding port pin (see SFR Definition 17.17, SFR Definition 17.19, SFR Definition 17.21, and SFR Definition 17.23). For example, to place Port pin 4.3 in push-pull mode (digital output), set P4MDOUT.3 to logic 1. All port pins default to open-drain mode upon device reset.

17.2.3. Configuring Port Pins as Digital Inputs

A Port pin is configured as a digital input by setting its output mode to "Open-Drain" in the PnMDOUT register and writing a logic 1 to the associated bit in the Port Data register. For example, P7.7 is configured as a digital input by setting P7MDOUT.7 to a logic 0, which selects open-drain output mode, and P3.7 to a logic 1, which disables the low-side output driver.

17.2.4. Weak Pullups

By default, each Port pin has an internal weak pullup device enabled which provides a resistive connection (about 100 kΩ) between the pin and V_{DD}. The weak pullup devices can be globally disabled by writing a logic 1 to the Weak Pullup Disable bit, (WEAKPUD, XBR2.7). The weak pullup is automatically deactivated on any pin that is driving a logic 0; that is, an output pin will not contend with its own pullup device.

17.2.5. External Memory Interface

If the External Memory Interface (EMIF) is enabled on the High ports (Ports 4 through 7), EMIFLE (XBR2.5) should be set to a logic 0.

If the External Memory Interface is enabled on the High ports and an off-chip MOVX operation occurs, the External Memory Interface will control the output states of the affected Port pins during the execution phase of the MOVX instruction, regardless of the settings of the Port Data registers. The output configuration of the Port pins is not affected by the EMIF operation, except that Read operations will explicitly disable the output drivers on the Data Bus during the MOVX execution. See **Section “16. External Data Memory Interface and On-Chip XRAM” on page 187** for more information about the External Memory Interface.

SFR Definition 18.3. CAN0CN: CAN Control

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
*	*	*	CANIF	*	*	*	*	
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xF8
SFR Page: 1

Bit 4: CANIF: CAN Interrupt Flag. Write = don't care.
0: CAN interrupt has not occurred.
1: CAN interrupt has occurred and is active.

CANIF is controlled by the CAN controller and is cleared by hardware once all interrupt conditions have been cleared in the CAN controller. See Section 3.4.1 in the *Bosch CAN User's Guide* (page 24) for more information concerning CAN controller interrupts.

***All CAN registers' functions/definitions are listed and described in the Bosch CAN User's Guide with the exception of the CANIF bit.**

This register may be accessed directly in the CIP-51 SFR register space, or through the indirect, index method (See Section "**18.2.5. Using CAN0ADR, CAN0DATH, and CANDATL to Access CAN Registers**" on page **232**).

SFR Definition 18.4. CAN0TST: CAN Test

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
Please see the Bosch CAN User's Guide for a complete definition of this register								
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xDB
SFR Page: 1

All CAN registers' functions/definitions are listed and described in the Bosch CAN User's Guide.
This register may be accessed directly in the CIP-51 SFR register space, or through the indirect, index method (See Section "**18.2.5. Using CAN0ADR, CAN0DATH, and CANDATL to Access CAN Registers**" on page **232**).

23.2. Timer 2, Timer 3, and Timer 4

Timers n are 16-bit counter/timers, each formed by two 8-bit SFRs: TMRnL (low byte) and TMRnH (high byte) where n = 2, 3, and 4 for timers 2, 3, and 4 respectively. These timers feature auto-reload, capture, and toggle output modes with the ability to count up or down. Capture Mode and Auto-reload mode are selected using bits in the Timer n Control registers (TMRnCN). Toggle output mode is selected using the Timer 2, 3, and 4 Configuration registers (TMRnCF). These timers may also be used to generate a square-wave at an external pin. As with Timers 0 and 1, Timers n can use either the system clock (divided by one, two, or twelve), external clock (divided by eight) or transitions on an external input pin as its clock source. The Counter/Timer Select bit C/Tn (TMRnCN.1) configures the peripheral as a counter or timer. Clearing C/Tn configures the Timer to be in a timer mode (i.e., the system clock or external clock as input for the timer). When C/Tn is set to 1, the timer is configured as a counter (i.e., high-to-low transitions at the Tn input pin increment (or decrement) the counter/timer register). Refer to **Section "17.1. Ports 0 through 3 and the Priority Crossbar Decoder" on page 204** for information on selecting and configuring external I/O pins for digital peripherals, such as the Tn pin. Timer 2 and 3 can be used to start an ADC Data Conversion and Timers 2, 3, and 4 can schedule DAC outputs. Only Timer 1 can be used to generate baud rates for UART 1, and Timers 1, 2, 3, or 4 may be used to generate baud rates for UART 0.

Timer n can use either SYSCLK, SYSCLK divided by 2, SYSCLK divided by 12, an external clock divided by 8, or high-to-low transitions on the Tn input pin as its clock source when operating in Counter/Timer with Capture mode. Clearing the C/Tn bit (TMRnCN.1) selects the system clock/external clock as the input for the timer. The Timer Clock Select bits TnM0 and TnM1 in TMRnCF can be used to select the system clock undivided, system clock divided by two, system clock divided by 12, or an external clock provided at the XTAL1/XTAL2 pins divided by 8 (see SFR Definition 23.9). When C/Tn is set to logic 1, a high-to-low transition at the Tn input pin increments the counter/timer register (i.e., configured as a counter).

23.2.1. Configuring Timer 2, 3, and 4 to Count Down

Timers 2, 3, and 4 have the ability to count down. When the timer's respective Decrement Enable Bit (DCEN) in the Timer Configuration Register (See SFR Definition 23.9) is set to '1', the timer can then count *up* or *down*. When DCEN = 1, the direction of the timer's count is controlled by the TnEX pin's logic level. When TnEX = 1, the counter/timer will count up; when TnEX = 0, the counter/timer will count down. To use this feature, TnEX must be enabled in the digital crossbar and configured as a digital input.

Note: When DCEN = 1, other functions of the TnEX input (i.e., capture and auto-reload) are not available. TnEX will only control the direction of the timer when DCEN = 1.

SFR Definition 23.9. TMRnCF: Timer n Configuration

			R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	TnM1	TnM0	TOGn	TnOE	DCEN	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: TMR2CF:0xC9;TMR3CF:0xC9;TMR4CF:0xC9
SFR Page TMR2CF: page 0;TMR3CF: page 1;TMR4CF: page 2

Bit7-5: Reserved.

Bit4-3: TnM1 and TnM0: Timer Clock Mode Select Bits.
Bits used to select the Timer clock source. The sources can be the System Clock (SYSCLK), SYSCLK divided by 2 or 12, or an external clock signal routed to Tn (port pin) divided by 8. Clock source is selected as follows:
00: SYSCLK/12
01: SYSCLK
10: EXTERNAL CLOCK/8
11: SYSCLK/2

Bit2: TOGn: Toggle output state bit.
When timer is used to toggle a port pin, this bit can be used to read the state of the output, or can be written to in order to force the state of the output.

Bit1: TnOE: Timer output enable bit.
This bit enables the timer to output a 50% duty cycle output to the timer's assigned external port pin.
NOTE: A timer is configured for Square Wave Output as follows:
CP/RLn = 0
C/Tn = 0
TnOE = 1
Load RCAPnH:RCAPnL (See **Section "Equation 23.1. Square Wave Frequency" on page 300***).*
Configure Port Pin for output (See **Section "17. Port Input/Output" on page 203***).*
0: Output of toggle mode not available at Timers' assigned port pin.
1: Output of toggle mode available at Timers' assigned port pin.

Bit0: DCEN: Decrement Enable Bit.
This bit enables the timer to count up or down as determined by the state of TnEX.
0: Timer will count up, regardless of the state of TnEX.
1: Timer will count up or down depending on the state of TnEX as follows:
if TnEX = 0, the timer counts DOWN
if TnEX = 1, the timer counts UP.

SFR Definition 23.13. TMRnH Timer n High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: TMR2H: 0xCD; TMR3H: 0xCD; TMR4H: 0xCD

SFR Page: TMR2H: page 0; TMR3H: page 1; TMR4H: page 2

Bits 7-0: TMRnH: Timer n High Byte.
The TMRnH register contains the high byte of the 16-bit Timer n