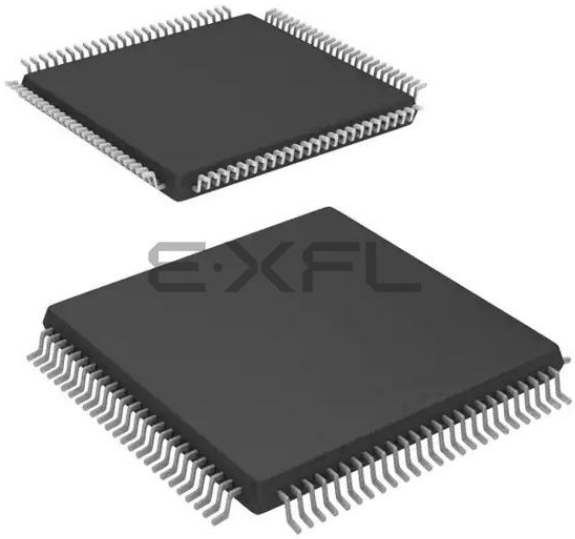

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f044-gq

List of Registers

Table 1.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory	RAM	External Memory Interface	SMBus/I^2C and SPI	CAN	UARTS	Timers (16-bit)	Programmable Counter Array	Digital Port I/O's	12-bit 100ksps ADC	10-bit 100ksps ADC	8-bit 500 ksps ADC Inputs	High Voltage Diff Amp	Voltage Reference	Temperature Sensor	DAC Resolution (bits)	DAC Outputs	Analog Comparators	Lead-free (RoHS Compliant)	Package
C8051F040	25	64 kB	4352	✓	✓	✓	2	5	✓	64	✓	-	8	✓	✓	✓	12	2	3	-	100TQFP
C8051F040-GQ	25	64 kB	4352	✓	✓	✓	2	5	✓	64	✓	-	8	✓	✓	✓	12	2	3	✓	100TQFP
C8051F041	25	64 kB	4352	✓	✓	✓	2	5	✓	32	✓	-	8	✓	✓	✓	12	2	3	-	64TQFP
C8051F041-GQ	25	64 kB	4352	✓	✓	✓	2	5	✓	32	✓	-	8	✓	✓	✓	12	2	3	✓	64TQFP
C8051F042	25	64 kB	4352	✓	✓	✓	2	5	✓	64	-	✓	8	✓	✓	✓	12	2	3	-	100TQFP
C8051F042-GQ	25	64 kB	4352	✓	✓	✓	2	5	✓	64	-	✓	8	✓	✓	✓	12	2	3	✓	100TQFP
C8051F043	25	64 kB	4352	✓	✓	✓	2	5	✓	32	-	✓	8	✓	✓	✓	12	2	3	-	64TQFP
C8051F043-GQ	25	64 kB	4352	✓	✓	✓	2	5	✓	32	-	✓	8	✓	✓	✓	12	2	3	✓	64TQFP
C8051F044	25	64 kB	4352	✓	✓	✓	2	5	✓	64	-	✓		✓	✓	✓			3	-	100TQFP
C8051F044-GQ	25	64 kB	4352	✓	✓	✓	2	5	✓	64	-	✓		✓	✓	✓			3	✓	100TQFP
C8051F045	25	64 kB	4352	✓	✓	✓	2	5	✓	32	-	✓		✓	✓	✓			3	-	64TQFP
C8051F045-GQ	25	64 kB	4352	✓	✓	✓	2	5	✓	32	-	✓		✓	✓	✓			3	✓	64TQFP
C8051F046	25	32 kB	4352	✓	✓	✓	2	5	✓	64	-	✓		✓	✓	✓			3	-	100TQFP
C8051F046-GQ	25	32 kB	4352	✓	✓	✓	2	5	✓	64	-	✓		✓	✓	✓			3	✓	100TQFP
C8051F047	25	32 kB	4352	✓	✓	✓	2	5	✓	32	-	✓		✓	✓	✓			3	-	64TQFP
C8051F047-GQ	25	32 kB	4352	✓	✓	✓	2	5	✓	32	-	✓		✓	✓	✓			3	✓	64TQFP

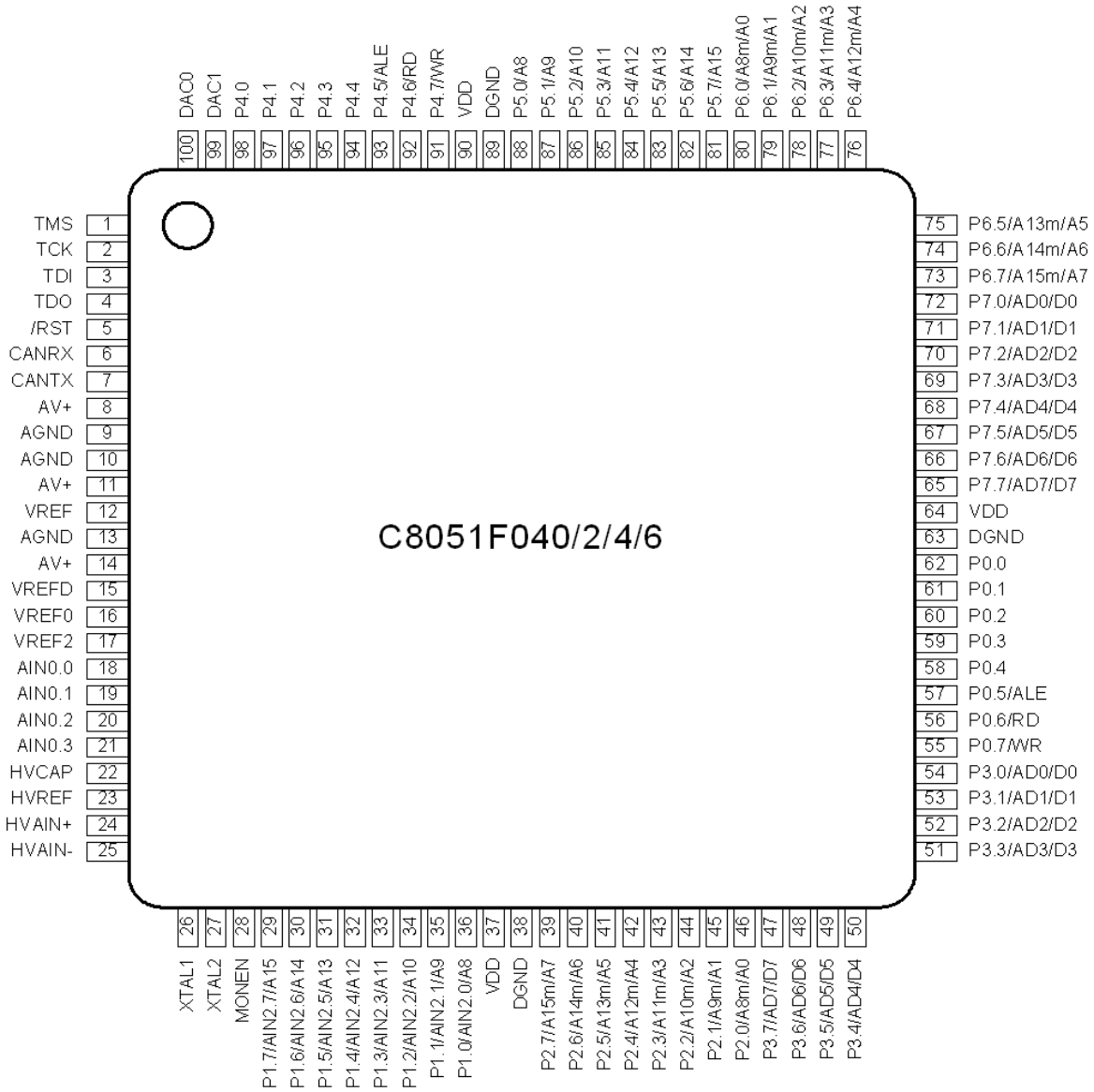
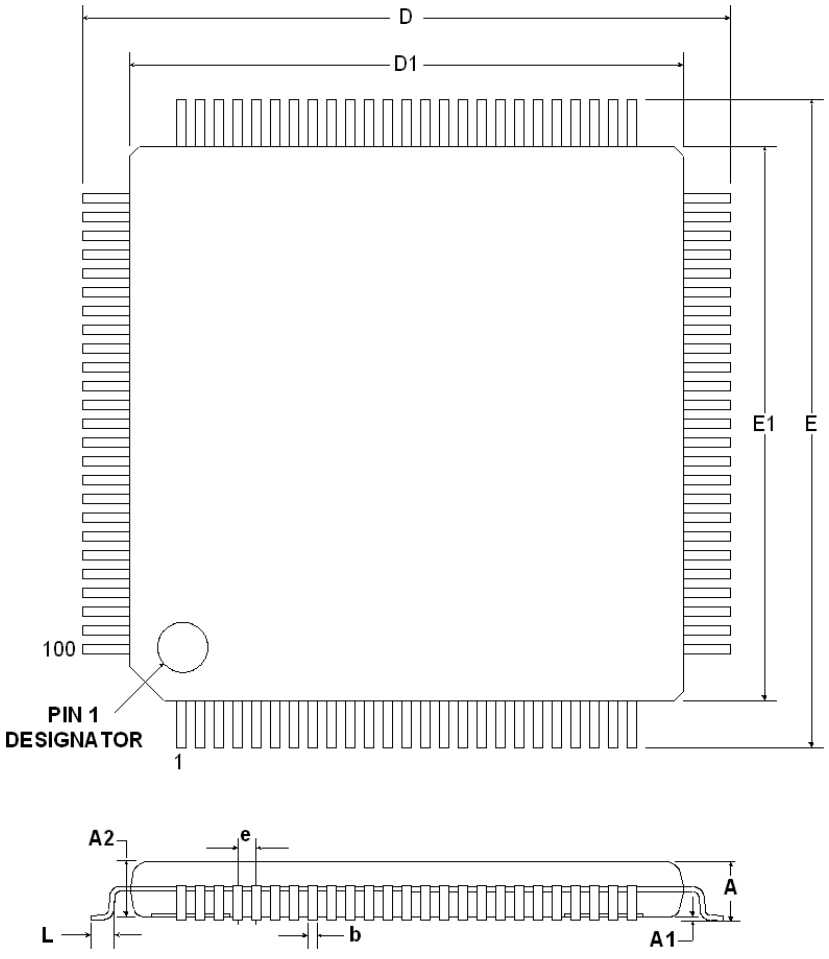


Figure 4.1. TQFP-100 Pinout Diagram



	MIN (mm)	NOM (mm)	MAX (mm)
A	-	-	1.20
A1	0.05	-	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
D	-	16.00	-
D1	-	14.00	-
e	-	0.50	-
E	-	16.00	-
E1	-	14.00	-
L	0.45	0.60	0.75

Figure 4.2. TQFP-100 Package Drawing

7.3.2. Window Detector in Differential Mode

Figure 7.6 shows two example window comparisons for differential mode, with ADC2LT = 0x10 (+16d) and ADC2GT = 0xFF (–1d). Notice that in Differential mode, the codes vary from –VREF to VREF x (127/128) and are represented as 8-bit 2s complement signed integers. In the left example, an AD2WINT interrupt will be generated if the ADC2 conversion word (ADC2L) is within the range defined by ADC2GT and ADC2LT (if 0xFF (–1d) < ADC2 < 0x0F (16d)). In the right example, an AD2WINT interrupt will be generated if ADC2 is outside of the range defined by ADC2GT and ADC2LT (if ADC2 < 0xFF (–1d) or ADC2 > 0x10 (+16d)).

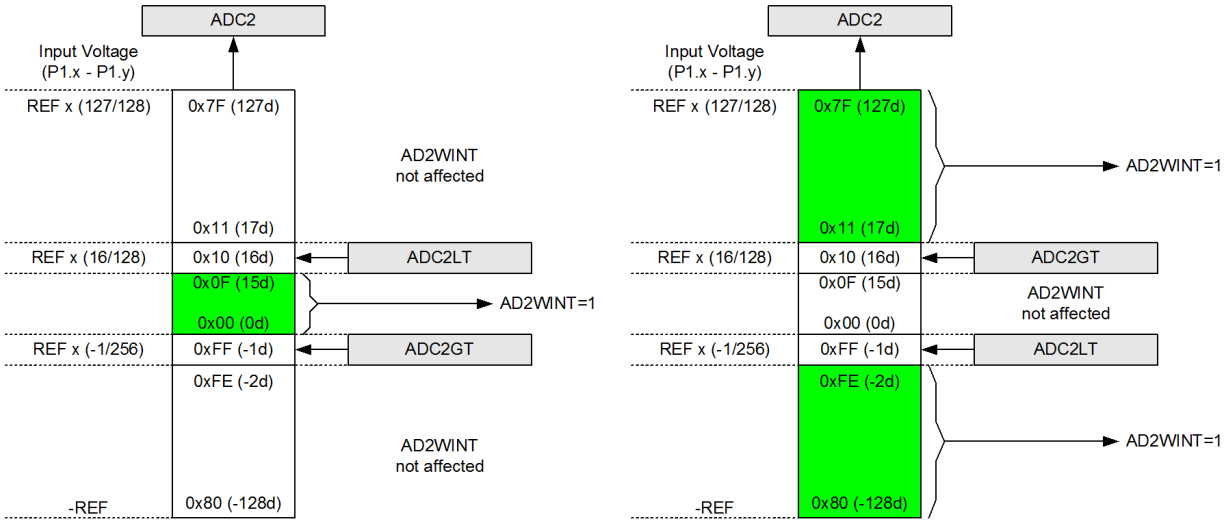


Figure 7.6. ADC Window Compare Examples, Differential Mode

12.2.7. Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should not be set to logic 1. Future product versions may use these bits to implement new features, in which case the reset value of the bit will be logic 0, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the data sheet associated with their corresponding system function.

SFR Definition 12.5. SP: Stack Pointer

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x81
SFR Page: All Pages

Bits7-0: SP: Stack Pointer.
The Stack Pointer holds the location of the top of the stack. The stack pointer is incremented before every PUSH operation. The SP register defaults to 0x07 after reset.

SFR Definition 12.6. DPL: Data Pointer Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x82
SFR Page: All Pages

Bits7-0: DPL: Data Pointer Low.
The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and Flash memory.

SFR Definition 12.7. DPH: Data Pointer High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x83
SFR Page: All Pages

Bits7-0: DPH: Data Pointer High.
The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed XRAM and Flash memory.

SFR Definition 12.9. ACC: Accumulator

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xE0
SFR Page: All Pages

Bits7-0: ACC: Accumulator.
This register is the accumulator for arithmetic operations.

SFR Definition 12.10. B: B Register

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xF0
SFR Page: All Pages

Bits7-0: B: B Register.
This register serves as a second accumulator for certain arithmetic operations.

Table 12.4. Interrupt Summary (Continued)

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit addressable?	Cleared by HW?	SFRPAGE (SFRPGEN = 1)	Enable Flag	Priority Control
Comparator 1	0x005B	11	CP1FIF/CP1RIF (CPT1CN.4/.5)			2	CP1IE (EIE1.5)	PCP1 (EIP1.5)
Comparator 2	0x0063	12	CP2FIF/CP2RIF (CPT2CN.4/.5)			3	CP2IE (EIE1.6)	PCP2 (EIP1.6)
Timer 3	0x0073	14	TF3 (TMR3CN.7)			1	ET3 (EIE2.0)	PT3 (EIP2.0)
ADC0 End of Conversion	0x007B	15	ADC0INT (ADC0CN.5)	Y		0	EADC0 (EIE2.1)	PADC0 (EIP2.1)
Timer 4	0x0083	16	TF4 (TMR4CN.7)			2	ET4 (EIE2.2)	PT4 (EIP2.2)
ADC2 Window Comparator	0x0093	17	AD2WINT (ADC2CN.0)			2	EWADC2 (EIE2.3)	PWADC2 (EIP2.3)
ADC2 End of Conversion	0x008B	18	ADC2INT (ADC1CN.5)			2	EADC1 (EIE2.4)	PADC1 (EIP2.4)
CAN Interrupt	0x009B	19	CAN0CN.7		Y	1	ECAN0 (EIE2.5)	PCAN0 (EIP2.5)
UART1	0x00A3	20	RI1 (SCON1.0) TI1 (SCON1.1)			1	ES1 (EIE2.6)	PS1 (EIP2.6)

SFR Definition 12.11. IE: Interrupt Enable

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EA	IEGF0	ET2	ES0	ET1	EX1	ET0	EX0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xA8
SFR Page: All Pages

Bit7: EA: Enable All Interrupts.
This bit globally enables/disables all interrupts. It overrides the individual interrupt mask settings.
0: Disable all interrupt sources.
1: Enable each interrupt according to its individual mask setting.

Bit6: IEGF0: General Purpose Flag 0.
This is a general purpose flag for use under software control.

Bit5: ET2: Enabler Timer 2 Interrupt.
This bit sets the masking of the Timer 2 interrupt.
0: Disable Timer 2 interrupt.
1: Enable interrupt requests generated by the TF2 flag.

Bit4: ES0: Enable UART0 Interrupt.
This bit sets the masking of the UART0 interrupt.
0: Disable UART0 interrupt.
1: Enable UART0 interrupt.

Bit3: ET1: Enable Timer 1 Interrupt.
This bit sets the masking of the Timer 1 interrupt.
0: Disable all Timer 1 interrupt.
1: Enable interrupt requests generated by the TF1 flag.

Bit2: EX1: Enable External Interrupt 1.
This bit sets the masking of external interrupt 1.
0: Disable external interrupt 1.
1: Enable interrupt requests generated by the /INT1 pin.

Bit1: ET0: Enable Timer 0 Interrupt.
This bit sets the masking of the Timer 0 interrupt.
0: Disable all Timer 0 interrupt.
1: Enable interrupt requests generated by the TF0 flag.

Bit0: EX0: Enable External Interrupt 0.
This bit sets the masking of external interrupt 0.
0: Disable external interrupt 0.
1: Enable interrupt requests generated by the /INT0 pin.

SFR Definition 13.1. WDTCN: Watchdog Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								xxxxx111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xFF
SFR Page: All Pages

Bits7-0: WDT Control
Writing 0xA5 both enables and reloads the WDT.
Writing 0xDE followed within 4 system clocks by 0xAD disables the WDT.
Writing 0xFF locks out the disable feature.

Bit4: Watchdog Status Bit (when Read)
Reading the WDTCN.[4] bit indicates the Watchdog Timer Status.
0: WDT is inactive
1: WDT is active

Bits2-0: Watchdog Timeout Interval Bits
The WDTCN.[2:0] bits set the Watchdog Timeout Interval. When writing these bits, WDTCN.7 must be set to 0.

16.4. Multiplexed and Non-multiplexed Selection

The External Memory Interface is capable of acting in a Multiplexed mode or a Non-multiplexed mode, depending on the state of the EMD2 (EMI0CF.4) bit.

16.4.1. Multiplexed Configuration

In Multiplexed mode, the Data Bus and the lower 8-bits of the Address Bus share the same Port pins: AD[7:0]. In this mode, an external latch (74HC373 or equivalent logic gate) is used to hold the lower 8-bits of the RAM address. The external latch is controlled by the ALE (Address Latch Enable) signal, which is driven by the External Memory Interface logic. An example of a Multiplexed Configuration is shown in Figure 16.1.

In Multiplexed mode, the external MOVX operation can be broken into two phases delineated by the state of the ALE signal. During the first phase, ALE is high and the lower 8-bits of the Address Bus are presented to AD[7:0]. During this phase, the address latch is configured such that the 'Q' outputs reflect the states of the 'D' inputs. When ALE falls, signaling the beginning of the second phase, the address latch outputs remain fixed and are no longer dependent on the latch inputs. Later in the second phase, the Data Bus controls the state of the AD[7:0] port at the time /RD or /WR is asserted.

See **Section "16.6.2. Multiplexed Mode" on page 199** for more information.

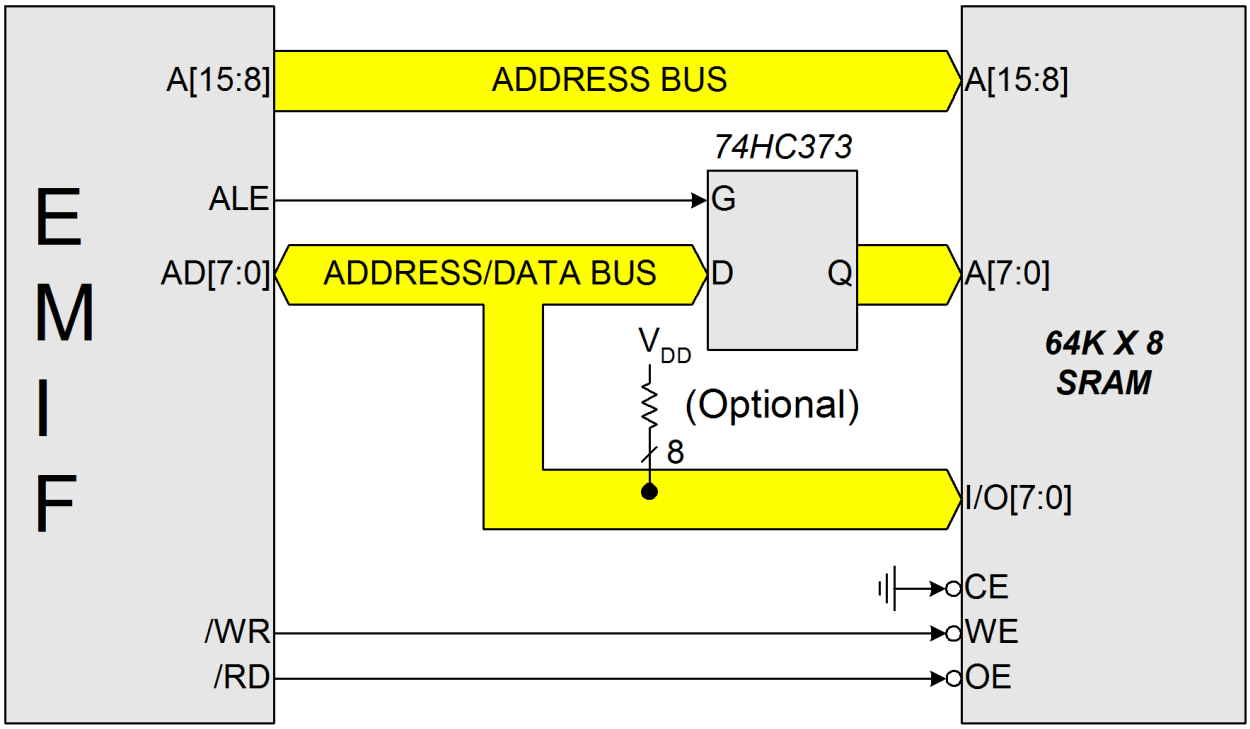


Figure 16.1. Multiplexed Configuration Example

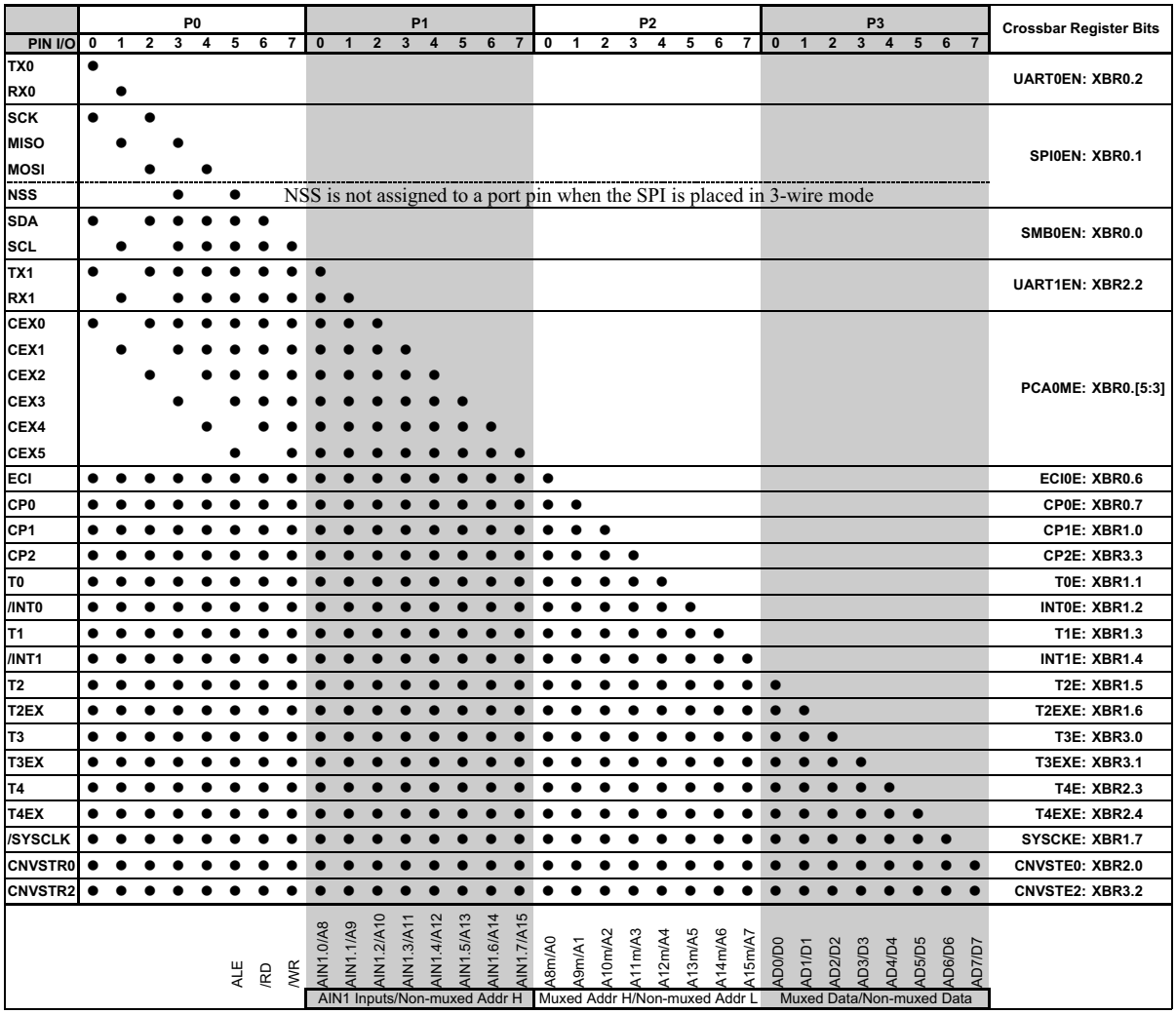


Figure 17.3. Priority Crossbar Decode Table

(EMIFLE = 0; P1MDIN = 0xFF)

17.1.1. Crossbar Pin Assignment and Allocation

The Crossbar assigns Port pins to a peripheral if the corresponding enable bits of the peripheral are set to a logic 1 in the Crossbar configuration registers XBR0, XBR1, XBR2, and XBR3, shown in SFR Definition 17.1, SFR Definition 17.2, SFR Definition 17.3, and SFR Definition 17.4. For example, if the UART0EN bit (XBR0.2) is set to a logic 1, the TX0 and RX0 pins will be mapped to P0.0 and P0.1 respectively. Because UART0 has the highest priority, its pins will always be mapped to P0.0 and P0.1 when UART0EN is set to a logic 1. If a digital peripheral's enable bits are not set to a logic 1, then its ports are not accessible at the Port pins of the device. Also note that the Crossbar assigns pins to all associated functions when a serial communication peripheral is selected (i.e. SMBus, SPI, UART). It would be impossible, for example, to assign TX0 to a Port pin without assigning RX0 as well. Each combination of enabled peripherals results in a unique device pinout.

All Port pins on Ports 0 through 3 that are not allocated by the Crossbar can be accessed as General-Purpose I/O (GPIO) pins by reading and writing the associated Port Data registers (See SFR Definition 17.5,

Table 18.2. CAN Register Index and Reset Values

CAN Register Index	Register Name	Reset Value	Notes
0x00	CAN Control Register	0x0001	Accessible in CIP-51 SFR Map
0x01	Status Register	0x0000	Accessible in CIP-51 SFR Map
0x02	Error Register	0x0000	Read Only
0x03	Bit Timing Register	0x2301	Write Enabled by CCE Bit in CAN0CN
0x04	Interrupt Register	0x0000	Read Only
0x05	Test Register	0x0000	Bit 7 (RX) is determined by CAN bus
0x06	BRP Extension Register	0x0000	Write Enabled by TEST bit in CAN0CN
0x08	IF1 Command Request	0x0001	CAN0ADR autoincrements in IF1 index space (0x08 - 0x12) upon write to CAN0DATL
0x09	IF1 Command Mask	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x0A	IF1 Mask 1	0xFFFF	CAN0ADR autoincrement upon write to CAN0DATL
0x0B	IF1 Mask 2	0xFFFF	CAN0ADR autoincrement upon write to CAN0DATL
0x0C	IF1 Arbitration 1	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x0D	IF1 Arbitration 2	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x0E	IF1 Message Control	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x0F	IF1 Data A1	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x10	IF1 Data A2	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x11	IF1 Data B1	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x12	IF1 Data B2	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x20	IF2 Command Request	0x0001	CAN0ADR autoincrements in IF2 index space (0x20 - 0x2A) upon write to CAN0DATL
0x21	IF2 Command Mask	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x22	IF2 Mask 1	0xFFFF	CAN0ADR autoincrement upon write to CAN0DATL
0x23	IF2 Mask 2	0xFFFF	CAN0ADR autoincrement upon write to CAN0DATL
0x24	IF2 Arbitration 1	0x0000	CAN0ADR autoincrement upon write to CAN0DATL
0x25	IF2 Arbitration 2	0x0000	CAN0ADR autoincrement upon write to CAN0DATL

20. Enhanced Serial Peripheral Interface (SPI0)

The Enhanced Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

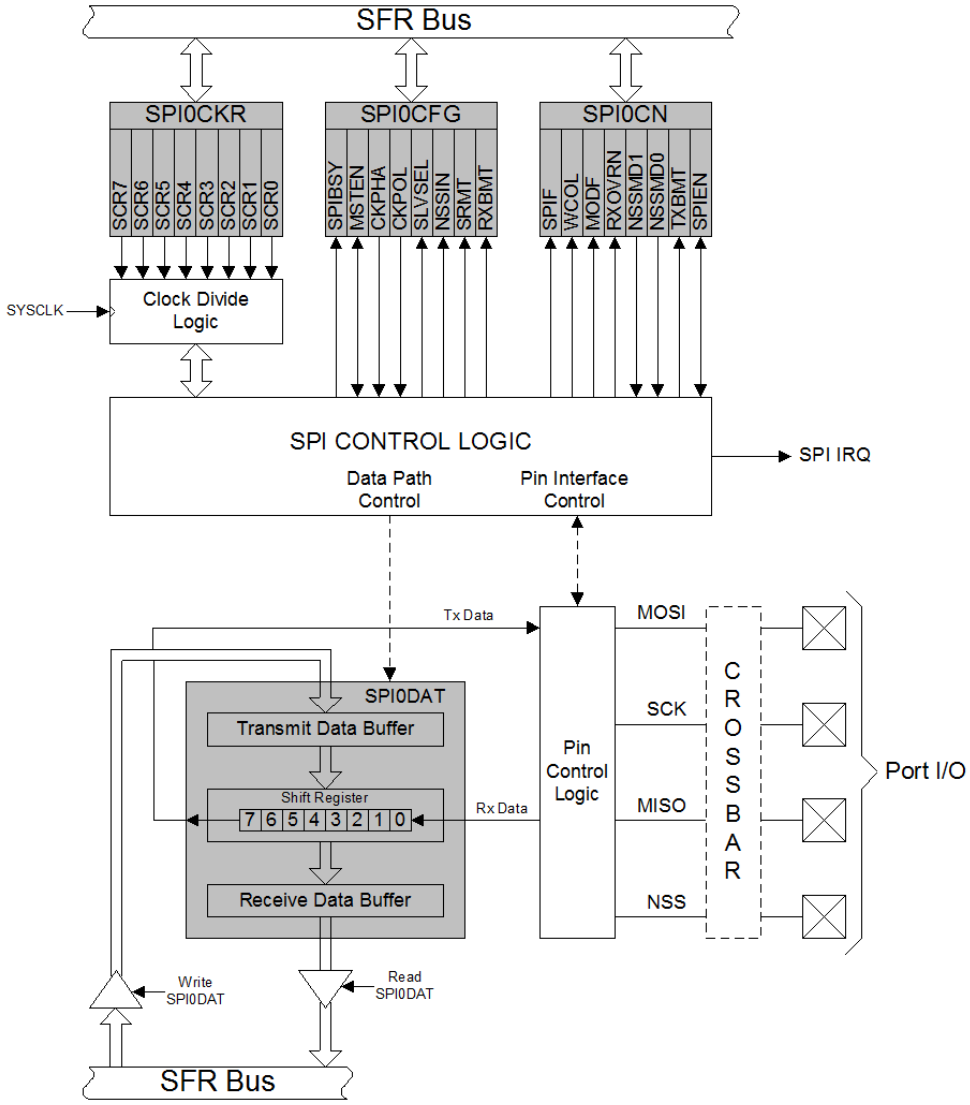


Figure 20.1. SPI Block Diagram

SFR Definition 21.1. SCON0: UART0 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
SM00	SM10	SM20	REN0	TB80	RB80	TI0	RI0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x98
SFR Page: 0

Bits7-6: SM00-SM10: Serial Port Operation Mode:
Write:
When written, these bits select the Serial Port Operation Mode as follows:

SM00	SM10	Mode
0	0	Mode 0: Synchronous Mode
0	1	Mode 1: 8-Bit UART, Variable Baud Rate
1	0	Mode 2: 9-Bit UART, Fixed Baud Rate
1	1	Mode 3: 9-Bit UART, Variable Baud Rate

Reading these bits returns the current UART0 mode as defined above.

Bit5: SM20: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port Operation Mode.
Mode 0: No effect
Mode 1: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI0 will only be activated if stop bit is logic level 1.
Mode 2 and 3: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI0 is set and an interrupt is generated only when the ninth bit is logic 1 and the received address matches the UART0 address or the broadcast address.

Bit4: REN0: Receive Enable.
This bit enables/disables the UART0 receiver.
0: UART0 reception disabled.
1: UART0 reception enabled.

Bit3: TB80: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in Modes 2 and 3. It is not used in Modes 0 and 1. Set or cleared by software as required.

Bit2: RB80: Ninth Receive Bit.
The bit is assigned the logic level of the ninth bit received in Modes 2 and 3. In Mode 1, if SM20 is logic 0, RB80 is assigned the logic level of the received stop bit. RB8 is not used in Mode 0.

Bit1: TI0: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART0 (after the 8th bit in Mode 0, or at the beginning of the stop bit in other modes). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

Bit0: RI0: Receive Interrupt Flag.
Set by hardware when a byte of data has been received by UART0 (as selected by the SM20 bit). When the UART0 interrupt is enabled, setting this bit causes the CPU to vector to the UART0 interrupt service routine. This bit must be cleared manually by software.

SFR Definition 22.1. SCON1: Serial Port 1 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
S1MODE	-	MCE1	REN1	TB81	RB81	TI1	RI1	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x98
SFR Page: 1

Bit7: S1MODE: Serial Port 1 Operation Mode.
This bit selects the UART1 Operation Mode.
0: Mode 0: 8-bit UART with Variable Baud Rate
1: Mode 1: 9-bit UART with Variable Baud Rate

Bit6: UNUSED. Read = 1b. Write = don't care.

Bit5: MCE1: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port 0 Operation Mode.
Mode 0: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI1 will only be activated if stop bit is logic level 1.
Mode 1: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI1 is set and an interrupt is generated only when the ninth bit is logic 1.

Bit4: REN1: Receive Enable.
This bit enables/disables the UART receiver.
0: UART1 reception disabled.
1: UART1 reception enabled.

Bit3: TB81: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in 9-bit UART Mode. It is not used in 8-bit UART Mode. Set or cleared by software as required.

Bit2: RB81: Ninth Receive Bit.
RB81 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.

Bit1: TI1: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART1 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART1 interrupt is enabled, setting this bit causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software.

Bit0: RI1: Receive Interrupt Flag.
Set to '1' by hardware when a byte of data has been received by UART1 (set at the STOP bit sampling time). When the UART1 interrupt is enabled, setting this bit to '1' causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software.

SFR Definition 23.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x88
SFR Page: 0

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 signal.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 interrupt will be falling-edge sensitive or active-low.
0: /INT1 is level triggered, active-low.
1: /INT1 is edge triggered, falling-edge.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 signal.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 interrupt will be falling-edge sensitive or active-low.
0: /INT0 is level triggered, active logic-low.
1: /INT0 is edge triggered, falling-edge.

JTAG Register Definition 25.3. FLASHCON: JTAG Flash Control Register

								Reset Value
SFLE	WRMD2	WRMD1	WRMD0	RDMD3	RDMD2	RDMD1	RDMD0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

This register determines how the Flash interface logic will respond to reads and writes to the FLASHDAT Register.

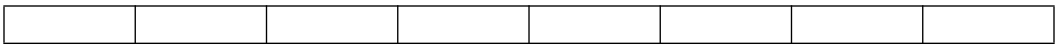
Bit 7: SFLE: Scratchpad Flash Memory Access Enable
When this bit is set, Flash reads and writes from user software are directed to the 128-byte scratchpad Flash sector. When accessing the scratchpad, Flash accesses out of the address range 0x00-0x7F should not be attempted. Reads/Writes outside of this range will yield undefined results.
0: Flash access is directed to the Program/Data Flash sector.
1: Flash access is directed to the 128-byte scratchpad sector.

Bits6-4: WRMD2-0: Write Mode Select Bits.
The Write Mode Select Bits control how the interface logic responds to writes to the FLASHDAT Register per the following values:
000: A FLASHDAT write replaces the data in the FLASHDAT register, but is otherwise ignored.
001: A FLASHDAT write initiates a write of FLASHDAT into the memory address by the FLASHADR register. FLASHADR is incremented by one when complete.
010: A FLASHDAT write initiates an erasure (sets all bytes to 0xFF) of the Flash page containing the address in FLASHADR. The data written must be 0xA5 for the erase to occur. FLASHADR is not affected. If FLASHADR targets the Read Lock Byte or the Write/Erase Lock Byte, the entire user space will be erased (i.e. entire Flash memory except for the Reserved area (See **Section "15. Flash Memory" on page 179**).
(All other values for WRMD2-0 are reserved.)

Bits3-0: RDMD3-0: Read Mode Select Bits.
The Read Mode Select Bits control how the interface logic responds to reads to the FLASHDAT Register per the following values:
0000: A FLASHDAT read provides the data in the FLASHDAT register, but is otherwise ignored.
0001: A FLASHDAT read initiates a read of the byte addressed by the FLASHADR register if no operation is currently active. This mode is used for block reads.
0010: A FLASHDAT read initiates a read of the byte addressed by FLASHADR only if no operation is active and any data from a previous read has already been read from FLASHDAT. This mode allows single bytes to be read (or the last byte of a block) without initiating an extra read.
(All other values for RDMD3-0 are reserved.)

JTAG Register Definition 25.4. FLASHDAT: JTAG Flash Data

Reset Value: 0000000000

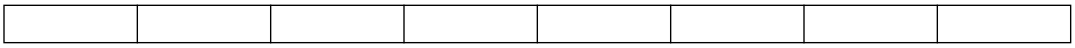


This register is used to read or write data to the Flash memory across the JTAG interface.

Bits9-2: DATA7-0: Flash Data Byte.
Bit1: FAIL: Flash Fail Bit.
0: Previous Flash memory operation was successful.
1: Previous Flash memory operation failed. Usually indicates the associated memory location was locked.
Bit0: BUSY: Flash Busy Bit.
0: Flash interface logic is not busy.
1: Flash interface logic is processing a request. Reads or writes while BUSY = 1 will not initiate another operation.

JTAG Register Definition 25.5. FLASHADR: JTAG Flash Address

Reset Value: 0x0000



This register holds the address for all JTAG Flash read, write, and erase operations. This register auto-increments after each read or write, regardless of whether the operation succeeded or failed.

Bits15-0: Flash Operation 16-bit Address.