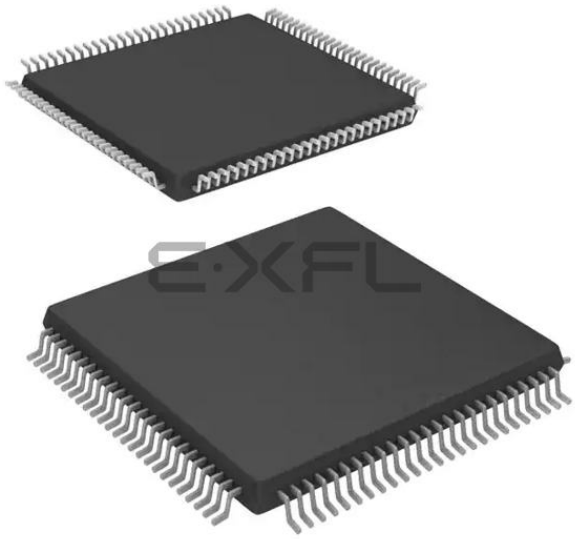

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Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	64
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f046-gqr

1. System Overview

The C8051F04x family of devices are fully integrated mixed-signal System-on-a-Chip MCUs with 64 digital I/O pins (C8051F040/2/4/6) or 32 digital I/O pins (C8051F041/3/5/7), and an integrated CAN 2.0B controller. Highlighted features are listed below; refer to Table 1.1 for specific product feature selection.

- High-Speed pipelined 8051-compatible CIP-51 microcontroller core (up to 25 MIPS)
- Controller Area Network (CAN 2.0B) Controller with 32 message objects, each with its own indentifier mask.
- In-system, full-speed, non-intrusive debug interface (on-chip)
- True 12-bit (C8051F040/1) or 10-bit (C8051F042/3/4/5/6/7) 100 ksps 8-channel ADC with PGA and analog multiplexer
- High Voltage Difference Amplifier input to the 12/10-bit ADC (60 V Peak-to-Peak) with programmable gain.
- True 8-bit 500 ksps 8-channel ADC with PGA and analog multiplexer (C8051F040/1/2/3)
- Two 12-bit DACs with programmable update scheduling (C8051F040/1/2/3)
- 64 kB (C8051F040/1/2/3/4/5) or 32 kB (C8051F046/7) of in-system programmable Flash memory
- 4352 (4096 + 256) bytes of on-chip RAM
- External Data Memory Interface with 64 kB address space
- SPI, SMBus/I^2C, and (2) UART serial interfaces implemented in hardware
- Five general purpose 16-bit Timers
- Programmable Counter/Timer Array with six capture/compare modules
- On-chip Watchdog Timer, V_{DD} Monitor, and Temperature Sensor

With on-chip V_{DD} monitor, Watchdog Timer, and clock oscillator, the C8051F04x family of devices are truly stand-alone System-on-a-Chip solutions. All analog and digital peripherals are enabled/disabled and configured by user firmware. The Flash memory can be reprogrammed even in-circuit, providing non-volatile data storage, and also allowing field upgrades of the 8051 firmware.

On-board JTAG debug circuitry allows non-intrusive (uses no on-chip resources), full speed, in-circuit programming and debugging using the production MCU installed in the final application. This debug system supports inspection and modification of memory and registers, setting breakpoints, watchpoints, single stepping, Run, and Halt commands. All analog and digital peripherals are fully functional while debugging using JTAG.

Each MCU is specified for 2.7 V to 3.6 V operation over the industrial temperature range (–45 to +85 °C). The Port I/Os, /RST, and JTAG pins are tolerant for input signals up to 5 V. The C8051F040/2/4/6 are available in a 100-pin TQFP and the C8051F041/3/5/7 are available in a 64-pin TQFP.

4. Pinout and Package Definitions

Table 4.1. Pin Definitions

Name	Pin Numbers		Type	Description
	F040/2/4/6	F041/3/5/7		
V_{DD}	37, 64, 90	24, 41, 57		Digital Supply Voltage. Must be tied to +2.7 to +3.6 V.
DGND	38, 63, 89	25, 40, 56		Digital Ground. Must be tied to Ground.
AV+	8, 11, 14	3, 6		Analog Supply Voltage. Must be tied to +2.7 to +3.6 V.
AGND	9, 10, 13	4, 5		Analog Ground. Must be tied to Ground.
TMS	1	58	D In	JTAG Test Mode Select with internal pullup.
TCK	2	59	D In	JTAG Test Clock with internal pullup.
TDI	3	60	D In	JTAG Test Data Input with internal pullup. TDI is latched on the rising edge of TCK.
TDO	4	61	D Out	JTAG Test Data Output with internal pullup. Data is shifted out on TDO on the falling edge of TCK. TDO output is a tri-state driver.
/RST	5	62	D I/O	Device Reset. Open-drain output of internal V_{DD} monitor. Is driven low when V_{DD} is < 2.7 V and MONEN is high. An external source can initiate a system reset by driving this pin low.
XTAL1	26	17	A In	Crystal Input. This pin is the return for the internal oscillator circuit for a crystal or ceramic resonator. For a precision internal clock, connect a crystal or ceramic resonator from XTAL1 to XTAL2. If overdriven by an external CMOS clock, this becomes the system clock.
XTAL2	27	18	A Out	Crystal Output. This pin is the excitation driver for a crystal or ceramic resonator.
MONEN	28	19	D In	V_{DD} Monitor Enable. When tied high, this pin enables the internal V_{DD} monitor, which forces a system reset when V_{DD} is < 2.7 V. When tied low, the internal V_{DD} monitor is disabled. **In most applications, MONEN should be connected directly to V_{DD}.**
VREF	12	7	A I/O	Bandgap Voltage Reference Output (all devices). DAC Voltage Reference Input (C8051F041/3 only).
VREFA		8	A In	ADC0 (C8051F041/3/5/7) and ADC2 (C8051F041/3 only) Voltage Reference Input.
VREF0	16		A In	ADC0 Voltage Reference Input.
VREF2	17		A In	ADC2 Voltage Reference Input (C8051F040/2 only).
VREF	15		A In	DAC Voltage Reference Input (C8051F040/2 only).
AIN0.0	18	9	A In	ADC0 Input Channel 0 (See ADC0 Specification for complete description).

Table 4.1. Pin Definitions (Continued)

Name	Pin Numbers		Type	Description
	F040/2/4/6	F041/3/5/7		
P4.4	94		D I/O	Port 4.4. See Port Input/Output section for complete description.
P4.5/ALE	93		D I/O	ALE Strobe for External Memory Address bus (multiplexed mode) Port 4.5 See Port Input/Output section for complete description.
P4.6/RD	92		D I/O	/RD Strobe for External Memory Address bus Port 4.6 See Port Input/Output section for complete description.
P4.7/WR	91		D I/O	/WR Strobe for External Memory Address bus Port 4.7 See Port Input/Output section for complete description.
P5.0/A8	88		D I/O	Bit 8 External Memory Address bus (Non-multiplexed mode) Port 5.0 See Port Input/Output section for complete description.
P5.1/A9	87		D I/O	Port 5.1. See Port Input/Output section for complete description.
P5.2/A10	86		D I/O	Port 5.2. See Port Input/Output section for complete description.
P5.3/A11	85		D I/O	Port 5.3. See Port Input/Output section for complete description.
P5.4/A12	84		D I/O	Port 5.4. See Port Input/Output section for complete description.
P5.5/A13	83		D I/O	Port 5.5. See Port Input/Output section for complete description.
P5.6/A14	82		D I/O	Port 5.6. See Port Input/Output section for complete description.
P5.7/A15	81		D I/O	Port 5.7. See Port Input/Output section for complete description.
P6.0/A8m/A0	80		D I/O	Bit 8 External Memory Address bus (Multiplexed mode) Bit 0 External Memory Address bus (Non-multiplexed mode) Port 6.0 See Port Input/Output section for complete description.
P6.1/A9m/A1	79		D I/O	Port 6.1. See Port Input/Output section for complete description.
P6.2/A10m/A2	78		D I/O	Port 6.2. See Port Input/Output section for complete description.
P6.3/A11m/A3	77		D I/O	Port 6.3. See Port Input/Output section for complete description.

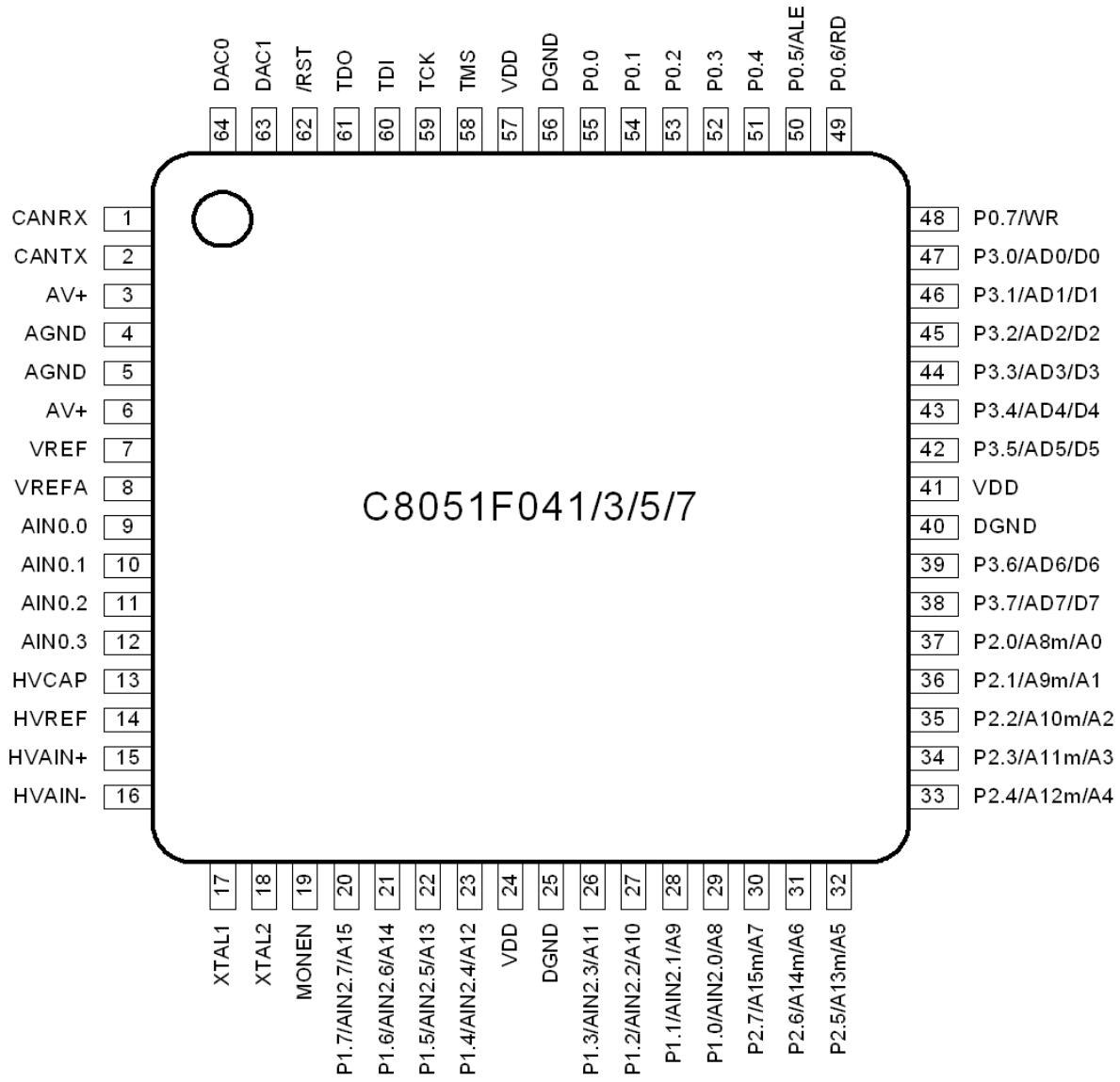

Figure 4.3. TQFP-64 Pinout Diagram

SFR Definition 5.6. ADC0CN: ADC0 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0CM1	AD0CM0	AD0WINT	AD0LJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xE8
SFR Page: 0

Bit7: AD0EN: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: AD0TM: ADC Track Mode Bit
0: When the ADC is enabled, tracking is continuous unless a conversion is in process
1: Tracking Defined by AD0CM1-0 bits

Bit5: AD0INT: ADC0 Conversion Complete Interrupt Flag.
This flag must be cleared by software.
0: ADC0 has not completed a data conversion since the last time this flag was cleared.
1: ADC0 has completed a data conversion.

Bit4: AD0BUSY: ADC0 Busy Bit.
Read:
0: ADC0 Conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 Conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1-0 = 00b

Bit3-2: AD0CM1-0: ADC0 Start of Conversion Mode Select.
If AD0TM = 0:
00: ADC0 conversion initiated on every write of ‘1’ to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 3.
10: ADC0 conversion initiated on rising edge of external CNVSTR0.
11: ADC0 conversion initiated on overflow of Timer 2.
If AD0TM = 1:
00: Tracking starts with the write of ‘1’ to AD0BUSY and lasts for 3 SAR clocks, followed by conversion.
01: Tracking started by the overflow of Timer 3 and last for 3 SAR clocks, followed by conversion.
10: ADC0 tracks only when CNVSTR0 input is logic low; conversion starts on rising CNVSTR0 edge.
11: Tracking started by the overflow of Timer 2 and last for 3 SAR clocks, followed by conversion.

Bit1: AD0WINT: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit0: AD0LJST: ADC0 Left Justify Select.
0: Data in ADC0H:ADC0L registers are right-justified.
1: Data in ADC0H:ADC0L registers are left-justified.

Table 6.1. AMUX Selection Chart (AMX0AD3-0 and AMX0CF3-0 bits)

		AMX0AD3-0								
		0000	**0001**	**0010**	**0011**	**0100**	**0101**	**0110**	**0111**	**1xxx**
AMX0CF Bits 3-0	**0000**	AIN0.0	AIN0.1	AIN0.2	AIN0.3	HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0001	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0010	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0011	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		HVDA	AGND	P3EVEN	P3ODD	TEMP SENSOR
	0100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	0101	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	0110	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	0111	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		P3EVEN	P3ODD	TEMP SENSOR
	1000	AIN0.0	AIN0.1	AIN0.2	AIN0.3	HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1001	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1010	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1011	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		HVDA	AGND	+P3EVEN -P3ODD		TEMP SENSOR
	1100	AIN0.0	AIN0.1	AIN0.2	AIN0.3	+(HVDA) -(HVREF)		+P3EVEN -P3ODD)		TEMP SENSOR
	1101	+(AIN0.0) -(AIN0.1)		AIN0.2	AIN0.3	+(HVDA) -(HVREF)		+P3EVEN -P3ODD		TEMP SENSOR
	1110	AIN0.0	AIN0.1	+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		+P3EVEN -P3ODD		TEMP SENSOR
	1111	+(AIN0.0) -(AIN0.1)		+(AIN0.2) -(AIN0.3)		+(HVDA) -(HVREF)		+P3EVEN -P3ODD		TEMP SENSOR

Note: “P3EVEN” denotes even numbered and “P3ODD” odd numbered Port 3 pins selected in the AMX0PRT register.

SFR Definition 10.1. REF0CN: Reference Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	AD0VRS	AD1VRS	TEMPE	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD1
SFR Page: 0

Bits7-5: UNUSED. Read = 000b; Write = don't care.
Bit4: AD0VRS: ADC0 Voltage Reference Select
0: ADC0 voltage reference from VREFA pin.
1: ADC0 voltage reference from DAC0 output (C8051F041/3 only).
Bit3: AD2VRS: ADC2 Voltage Reference Select (C8051F041/3 only).
0: ADC2 voltage reference from VREFA pin.
1: ADC2 voltage reference from AV+.
Bit2: TEMPE: Temperature Sensor Enable Bit.
0: Internal Temperature Sensor Off.
1: Internal Temperature Sensor On.
Bit1: BIASE: ADC/DAC Bias Generator Enable Bit. (Must be '1' if using ADC or DAC).
0: Internal Bias Generator Off.
1: Internal Bias Generator On.
Bit0: REFBE: Internal Reference Buffer Enable Bit.
0: Internal Reference Buffer Off.
1: Internal Reference Buffer On. Internal voltage reference is driven on the VREF pin.

Table 12.2. Special Function Register (SFR) Memory Map (Continued)

ADDRESS	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	SFR PAGE
B0	P3 **(ALL PAGES)**							FLSCL FLACL	0 1 2 3 F
A8	IE **(ALL PAGES)**	SADDR0				P1MDIN	P2MDIN	P3MDIN	0 1 2 3 F
A0	P2 **(ALL PAGES)**	EMI0TC	EMI0CN	EMI0CF	P0MDOUT	P1MDOUT	P2MDOUT	P3MDOUT	0 1 2 3 F
98	SCON0 SCON1	SBUF0 SBUF1	SPI0CFG	SPI0DAT	P4MDOUT	SPI0CKR P5MDOUT	P6MDOUT	P7MDOUT	0 1 2 3 F
90	P1 **(ALL PAGES)**	SSTA0					SFRPGCN	CLKSEL	0 1 2 3 F
88	TCON CPT0CN CPT1CN CPT2CN	TMOD CPT0MD CPT1MD CPT2MD	TL0 OSCICN	TL1 OSCICL	TH0 OSCXCN	TH1	CKCON	PSCTL	0 1 2 3 F
80	P0 **(ALL PAGES)**	SP **(ALL PAGES)**	DPL **(ALL PAGES)**	DPH **(ALL PAGES)**	SFRPAGE **(ALL PAGES)**	SFRNEXT **(ALL PAGES)**	SFRLAST **(ALL PAGES)**	PCON **(ALL PAGES)**	0 1 2 3 F
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	

13.7.1. Enable/Reset WDT

The watchdog timer is both enabled and reset by writing 0xA5 to the WDTCN register. The user's application software should include periodic writes of 0xA5 to WDTCN as needed to prevent a watchdog timer overflow. The WDT is enabled and reset as a result of any system reset.

13.7.2. Disable WDT

Writing 0xDE followed by 0xAD to the WDTCN register disables the WDT. The following code segment illustrates disabling the WDT:

```
CLR    EA            ; disable all interrupts
MOV    WDTCN,#0DEh   ; disable software watchdog timer
MOV    WDTCN,#0ADh
SETB   EA            ; re-enable interrupts
```

The writes of 0xDE and 0xAD must occur within 4 clock cycles of each other, or the disable operation is ignored. Interrupts should be disabled during this procedure to avoid delay between the two writes.

13.7.3. Disable WDT Lockout

Writing 0xFF to WDTCN locks out the disable feature. Once locked out, the disable operation is ignored until the next system reset. Writing 0xFF does not enable or reset the watchdog timer. Applications always intending to use the watchdog should write 0xFF to WDTCN in the initialization code.

13.7.4. Setting WDT Interval

WDTCN.[2:0] control the watchdog timeout interval. The interval is given by the following equation:

$4^{3 + WDTCN[2-0]} \times T_{sysclk}$; where T_{sysclk} is the system clock period.

For a 3 MHz system clock, this provides an interval range of 0.021 ms to 349.5 ms. WDTCN.7 must be logic 0 when setting this interval. Reading WDTCN returns the programmed interval. WDTCN.[2:0] reads 111b after a system reset.

SFR Definition 14.1. OSCICL: Internal Oscillator Calibration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8B
SFR Page: F

Bits 7-0: OSCICL: Internal Oscillator Calibration Register
This register calibrates the internal oscillator period. The reset value for OSCICL defines the internal oscillator base frequency. The reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

SFR Definition 14.2. OSCICN: Internal Oscillator Control

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
IOSCEN	IFRDY	-	-	-	-	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8A
SFR Page: F

Bit7: IOSCEN: Internal Oscillator Enable Bit.
0: Internal Oscillator Disabled
1: Internal Oscillator Enabled
Bit6: IFRDY: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.
Bits5-2: Reserved.
Bits1-0: IFCN1-0: Internal Oscillator Frequency Control Bits.
00: SYSCLK derived from Internal Oscillator divided by 8.
01: SYSCLK derived from Internal Oscillator divided by 4.
10: SYSCLK derived from Internal Oscillator divided by 2.
11: SYSCLK derived from Internal Oscillator divided by 1.

14.5. External RC Example

If an RC network is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 14.1, Option 2. The capacitor should be no greater than 100 pF; however, for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. If the frequency desired is 100 kHz, let R = 246 kΩ and C = 50 pF:

f = 1.23(10^3) / RC = 1.23 (10^3) / [246 x 50] = 0.1 MHz = 100 kHz

Referring to the table in SFR Definition 14.4, the required XFCN setting is 010b.

14.6. External Capacitor Example

If a capacitor is used as an external oscillator for the MCU, the circuit should be configured as shown in Figure 14.1, Option 3. The capacitor should be no greater than 100 pF; however, for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the desired frequency of oscillation and find the capacitor to be used from the equations below. Assume V_{DD} = 3.0 V and f = 50 kHz:

f = KF / (C x V_{DD}) = KF / (C x 3) = 0.050 MHz

If a frequency of roughly 50 kHz is desired, select the K Factor from the table in SFR Definition 14.4 as KF = 7.7:

0.050 MHz = 7.7 / (C x 3)

C x 3 = 7.7 / 0.050 = 154, so C = 154 / 3 pF = 51.3 pF

Therefore, the XFCN value to use in this example is 010b.

15.3.1. Summary of Flash Security Options

There are three Flash access methods supported on the C8051F04x devices; 1) Accessing Flash through the JTAG debug interface, 2) Accessing Flash from firmware residing below the Flash Access Limit, and 3) Accessing Flash from firmware residing at or above the Flash Access Limit.

Accessing Flash through the JTAG debug interface:

1. The Read and Write/Erase Lock bytes (security bytes) provide security for Flash access through the JTAG interface.
2. Any unlocked page may be read from, written to, or erased.
3. Locked pages cannot be read from, written to, or erased.
4. Reading the security bytes is always permitted.
5. Locking additional pages by writing to the security bytes is always permitted.
6. If the page containing the security bytes is **unlocked**, it can be directly erased. **Doing so will reset the security bytes and unlock all pages of Flash.**
7. If the page containing the security bytes is **locked**, it cannot be directly erased. **To unlock the page containing the security bytes, a full JTAG device erase is required.** A full JTAG device erase will erase all Flash pages, including the page containing the security bytes and the security bytes themselves.
8. The Reserved Area cannot be read from, written to, or erased at any time.

Accessing Flash from firmware residing below the Flash Access Limit:

1. The Read and Write/Erase Lock bytes (security bytes) do not restrict Flash access from user firmware.
2. Any page of Flash except the page containing the security bytes may be read from, written to, or erased.
3. **The page containing the security bytes cannot be erased.** Unlocking pages of Flash can only be performed via the JTAG interface.
4. The page containing the security bytes may be read from or written to. Pages of Flash can be locked from JTAG access by writing to the security bytes.
5. The Reserved Area cannot be read from, written to, or erased at any time.

Accessing Flash from firmware residing at or above the Flash Access Limit:

1. The Read and Write/Erase Lock bytes (security bytes) do not restrict Flash access from user firmware.
2. Any page of Flash at or above the Flash Access Limit except the page containing the security bytes may be read from, written to, or erased.
3. Any page of Flash below the Flash Access Limit cannot be read from, written to, or erased.
4. Code branches to locations below the Flash Access Limit are permitted.
5. **The page containing the security bytes cannot be erased.** Unlocking pages of Flash can only be performed via the JTAG interface.
6. The page containing the security bytes may be read from or written to. Pages of Flash can be locked from JTAG access by writing to the security bytes.
7. The Reserved Area cannot be read from, written to, or erased at any time.

16.2. Configuring the External Memory Interface

Configuring the External Memory Interface consists of five steps:

1. Select EMIF on Low Ports (P3, P2, P1, and P0) or High Ports (P7, P6, P5, and P4).
2. Configure the Output Modes of the port pins as either push-pull or open-drain.
3. Select Multiplexed mode or Non-multiplexed mode.
4. Select the memory mode (on-chip only, split mode without bank select, split mode with bank select, or off-chip only).
5. Set up timing to interface with off-chip memory or peripherals.

Each of these five steps is explained in detail in the following sections. The Port selection, Multiplexed mode selection, and Mode bits are located in the EMI0CF register shown in SFR Definition 16.2.

16.3. Port Selection and Configuration

The External Memory Interface can appear on Ports 3, 2, 1, and 0 (C8051F04x devices) or on Ports 7, 6, 5, and 4 (C8051F040/2/4/6 devices only), depending on the state of the PRTSEL bit (EMI0CF.5). If the lower Ports are selected, the EMIFLE bit (XBR2.1) must be set to a '1' so that the Crossbar will skip over P0.7 (/WR), P0.6 (/RD), and, if multiplexed mode is selected, P0.5 (ALE). For more information about the configuring the Crossbar, see **Section "17.1. Ports 0 through 3 and the Priority Crossbar Decoder" on page 204**.

The External Memory Interface claims the associated Port pins for memory operations ONLY during the execution of an off-chip MOVX instruction. Once the MOVX instruction has completed, control of the Port pins reverts to the Port latches or to the Crossbar (on Ports 3, 2, 1, and 0). See **Section "17. Port Input/ Output" on page 203** for more information about the Crossbar and Port operation and configuration. **The Port latches should be explicitly configured as push-pull to 'park' the External Memory Interface pins in a dormant state, most commonly by setting them to a logic 1**.

During the execution of the MOVX instruction, the External Memory Interface will explicitly disable the drivers on all Port pins that are acting as Inputs (Data[7:0] during a READ operation, for example). The Output mode of the Port pins (whether the pin is configured as Open-Drain or Push-Pull) is unaffected by the External Memory Interface operation, and remains controlled by the PnMDOUT registers. In most cases, the output modes of all EMIF pins should be configured for push-pull mode. See **Section "17.1.2. Configuring the Output Modes of the Port Pins" on page 206**.

SFR Definition 16.3. EMI0TC: External Memory Timing Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
EAS1	EAS0	ERW3	EWR2	EWR1	EWR0	EAH1	EAH0	11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xA1
SFR Page: 0

Bits7-6: EAS1-0: EMIF Address Setup Time Bits.
00: Address setup time = 0 SYSCLK cycles.
01: Address setup time = 1 SYSCLK cycle.
10: Address setup time = 2 SYSCLK cycles.
11: Address setup time = 3 SYSCLK cycles.

Bits5-2: EWR3-0: EMIF /WR and /RD Pulse-Width Control Bits.
0000: /WR and /RD pulse width = 1 SYSCLK cycle.
0001: /WR and /RD pulse width = 2 SYSCLK cycles.
0010: /WR and /RD pulse width = 3 SYSCLK cycles.
0011: /WR and /RD pulse width = 4 SYSCLK cycles.
0100: /WR and /RD pulse width = 5 SYSCLK cycles.
0101: /WR and /RD pulse width = 6 SYSCLK cycles.
0110: /WR and /RD pulse width = 7 SYSCLK cycles.
0111: /WR and /RD pulse width = 8 SYSCLK cycles.
1000: /WR and /RD pulse width = 9 SYSCLK cycles.
1001: /WR and /RD pulse width = 10 SYSCLK cycles.
1010: /WR and /RD pulse width = 11 SYSCLK cycles.
1011: /WR and /RD pulse width = 12 SYSCLK cycles.
1100: /WR and /RD pulse width = 13 SYSCLK cycles.
1101: /WR and /RD pulse width = 14 SYSCLK cycles.
1110: /WR and /RD pulse width = 15 SYSCLK cycles.
1111: /WR and /RD pulse width = 16 SYSCLK cycles.

Bits1-0: EAH1-0: EMIF Address Hold Time Bits.
00: Address hold time = 0 SYSCLK cycles.
01: Address hold time = 1 SYSCLK cycle.
10: Address hold time = 2 SYSCLK cycles.
11: Address hold time = 3 SYSCLK cycles.

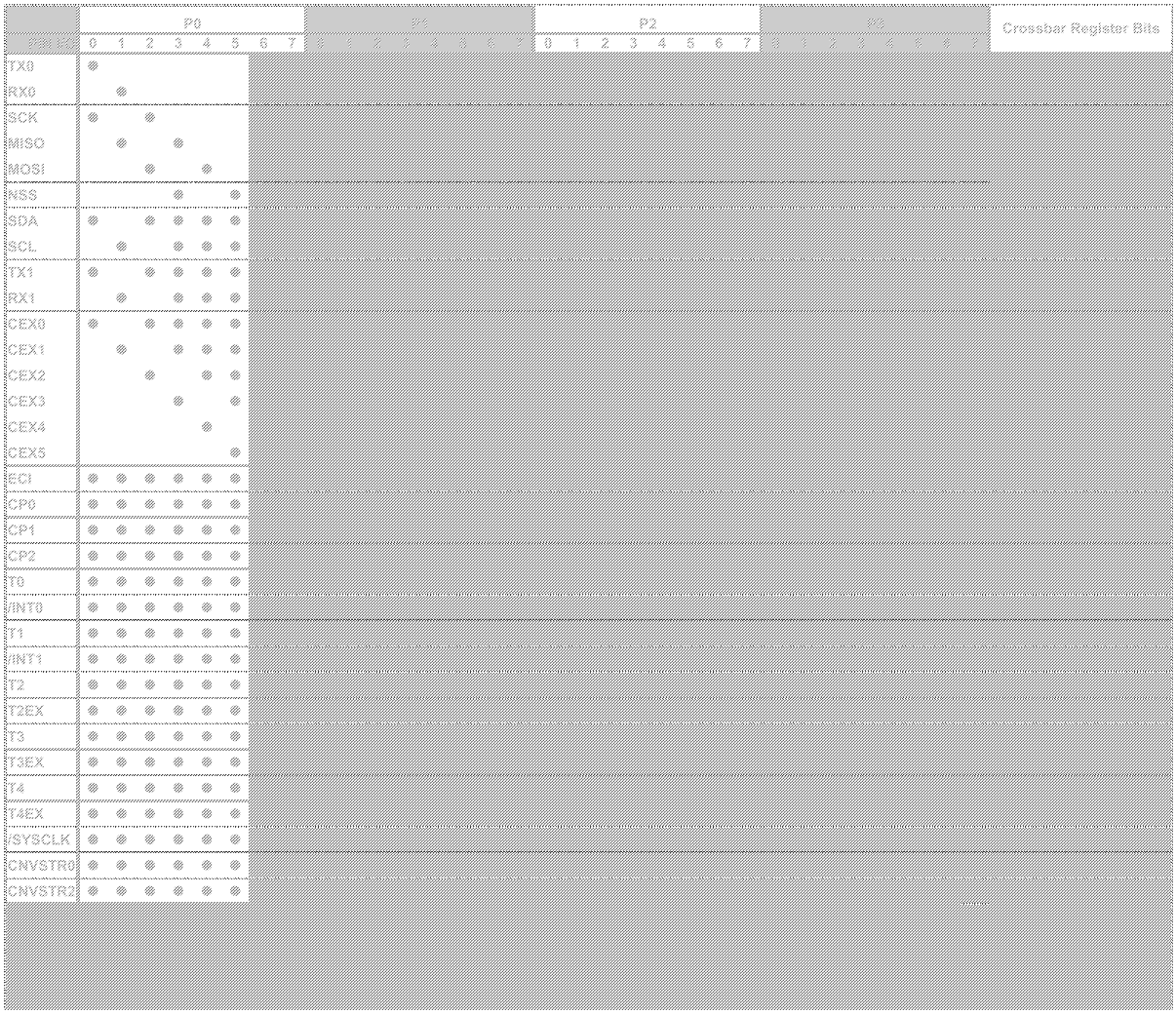

Figure 17.5. Priority Crossbar Decode Table
(EMIFLE = 1; EMIF in Non-multiplexed Mode; P1MDIN = 0xFF)

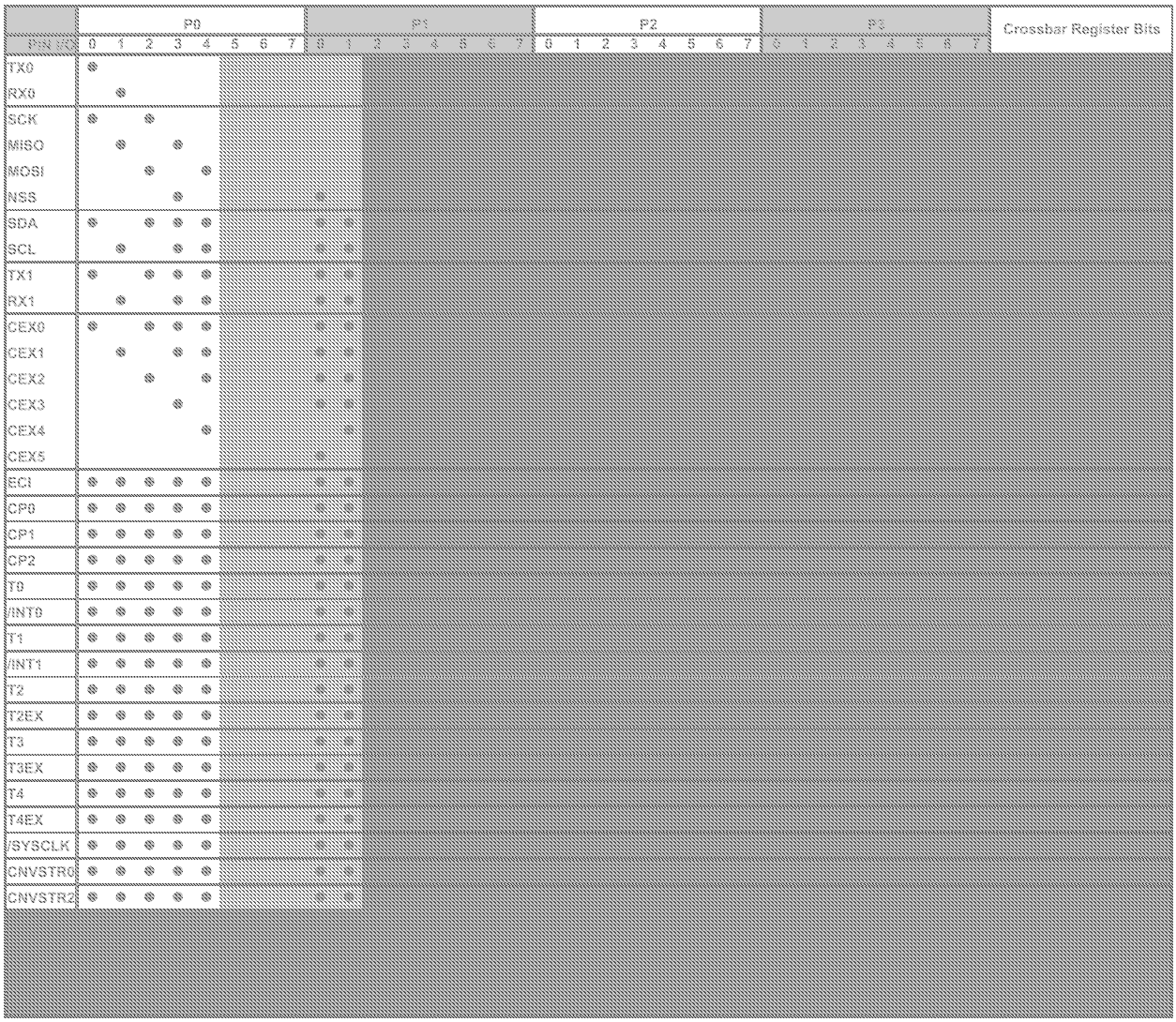

Figure 17.6. Crossbar Example:

(EMIFLE = 1; EMIF in Multiplexed Mode; P1MDIN = 0xE3;
XBR0 = 0x05; XBR1 = 0x14; XBR2 = 0x42)

We will adjust the length of the 4 bit segments so that their sum is as close as possible to the desired bit time. Since each segment must be an integer multiple of the time quantum (t_q), the closest achievable bit time is 22 t_q (994.642 ns), yielding a bit rate of 1.00539 Mbit/sec. The Sync_Seg is a constant 1 t_q. The Prop_Seg must be greater than or equal to the propagation delay of 400 ns; we choose 9 t_q (406.899 ns).

The remaining time quanta (t_q) in the bit time are divided between Phase_Seg1 and Phase_Seg2 as shown in Figure 18.1. We select Phase_Seg1 = 6 t_q and Phase_Seg2 = 6 t_q.

$$\text{Phase\_Seg1} + \text{Phase\_Seg2} = \text{Bit Time} - (\text{Sync\_Seg} + \text{Prop\_Seg})$$

Note 1: If Phase_Seg1 + Phase_Seg2 is even, then Phase_Seg2 = Phase_Seg1.

Note 2: Phase_Seg2 should be at least 2 t_q.

Equation 18.1. Assigning the Phase Segments

The Synchronization Jump Width (SJW) timing parameter is defined by Figure 18.2. It is used for determining the value written to the Bit Timing Register and for determining the required oscillator tolerance. Since we are using a quartz crystal as the system clock source, an oscillator tolerance calculation is not needed.

$$\text{SJW} = \min (4, \text{Phase\_Seg1})$$

Equation 18.2. Synchronization Jump Width (SJW)

The value written to the Bit Timing Register can be calculated using Equation 18.3. The BRP Extension register is left at its reset value of 0x0000.

BRPE = BRP - 1 = BRP Extension Register = 0x0000

SJWp = SJW - 1 = min (4, 6) – 1 = 3

TSEG1 = (Prop_Seg + Phase_Seg1 - 1) = 9 + 6 - 1 = 14

TSEG2 = (Phase_Seg2 - 1) = 5

Bit Timing Register = (TSEG2 * 0x1000) + (TSEG1 * 0x0100) + (SJWp * 0x0040) + BRPE = 0x5EC0

Equation 18.3. Calculating the Bit Timing Register Value

The following steps are performed to initialize the CAN timing registers:

Step 1. Set the SFRPAGE register to CAN0_PAGE.
Step 2. Set the INIT the CCE bits to ‘1’ in the CAN Control Register accessible through the CAN0CN SFR.
Step 3. Set the CAN0ADR to 0x03 to point to the Bit Timing Register.

19.4. SMBus Special Function Registers

The SMBus0 serial interface is accessed and controlled through five SFRs: SMB0CN Control Register, SMB0CR Clock Rate Register, SMB0ADR Address Register, SMB0DAT Data Register and SMB0STA Status Register. The five special function registers related to the operation of the SMBus0 interface are described in the following sections.

19.4.1. Control Register

The SMBus0 Control register SMB0CN is used to configure and control the SMBus0 interface. All of the bits in the register can be read or written by software. Two of the control bits are also affected by the SMBus0 hardware. The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by the hardware when a valid serial interrupt condition occurs. It can only be cleared by software. The Stop flag (STO, SMB0CN.4) is set to logic 1 by software. It is cleared to logic 0 by hardware when a STOP condition is detected on the bus.

Setting the ENSMB flag to logic 1 enables the SMBus0 interface. Clearing the ENSMB flag to logic 0 disables the SMBus0 interface and removes it from the bus. Momentarily clearing the ENSMB flag and then resetting it to logic 1 will reset SMBus0 communication. However, ENSMB should not be used to temporarily remove a device from the bus since the bus state information will be lost. Instead, the Assert Acknowledge (AA) flag should be used to temporarily remove the device from the bus (see description of AA flag below).

Setting the Start flag (STA, SMB0CN.5) to logic 1 will put SMBus0 in a master mode. If the bus is free, SMBus0 will generate a START condition. If the bus is not free, SMBus0 waits for a STOP condition to free the bus and then generates a START condition after a 5 µs delay per the SMB0CR value (In accordance with the SMBus protocol, the SMBus0 interface also considers the bus free if the bus is idle for 50 µs and no STOP condition was recognized). If STA is set to logic 1 while SMBus0 is in master mode and one or more bytes have been transferred, a repeated START condition will be generated.

When the Stop flag (STO, SMB0CN.4) is set to logic 1 while the SMBus0 interface is in master mode, the interface generates a STOP condition. In a slave mode, the STO flag may be used to recover from an error condition. In this case, a STOP condition is not generated on the bus, but the SMBus hardware behaves as if a STOP condition has been received and enters the "not addressed" slave receiver mode. Note that this simulated STOP will not cause the bus to appear free to SMBus0. The bus will remain occupied until a STOP appears on the bus or a Bus Free Timeout occurs. Hardware automatically clears the STO flag to logic 0 when a STOP condition is detected on the bus.

The Serial Interrupt flag (SI, SMB0CN.3) is set to logic 1 by hardware when the SMBus0 interface enters any one of the 28 possible states except the Idle state. If interrupts are enabled for the SMBus0 interface, an interrupt request is generated when the SI flag is set. The SI flag must be cleared by software.

Important Note: If SI is set to logic 1 while the SCL line is low, the clock-low period of the serial clock will be stretched and the serial transfer is suspended until SI is cleared to logic 0. A high level on SCL is not affected by the setting of the SI flag.

The Assert Acknowledge flag (AA, SMB0CN.2) is used to set the level of the SDA line during the acknowledge clock cycle on the SCL line. Setting the AA flag to logic 1 will cause an ACK (low level on SDA) to be sent during the acknowledge cycle if the device has been addressed. Setting the AA flag to logic 0 will cause a NACK (high level on SDA) to be sent during acknowledge cycle. After the transmission of a byte in slave mode, the slave can be temporarily removed from the bus by clearing the AA flag. The slave's own address and general call address will be ignored. To resume operation on the bus, the AA flag must be reset to logic 1 to allow the slave's address to be recognized.

Setting the SMBus0 Free Timer Enable bit (FTE, SMB0CN.1) to logic 1 enables the timer in SMB0CR. When SCL goes high, the timer in SMB0CR counts up. A timer overflow indicates a free bus timeout: if SMBus0 is waiting to generate a START, it will do so after this timeout. The bus free period should be less than 50 µs (see SFR Definition 19.2, SMBus0 Clock Rate Register).

When the TOE bit in SMB0CN is set to logic 1, Timer 4 is used to detect SCL low timeouts. If Timer 4 is enabled (see **Section “23.2. Timer 2, Timer 3, and Timer 4” on page 297**), Timer 4 is forced to reload when SCL is high, and forced to count when SCL is low. With Timer 4 enabled and configured to overflow after 25 ms (and TOE set), a Timer 4 overflow indicates a SCL low timeout; the Timer 4 interrupt service routine can then be used to reset SMBus0 communication in the event of an SCL low timeout.