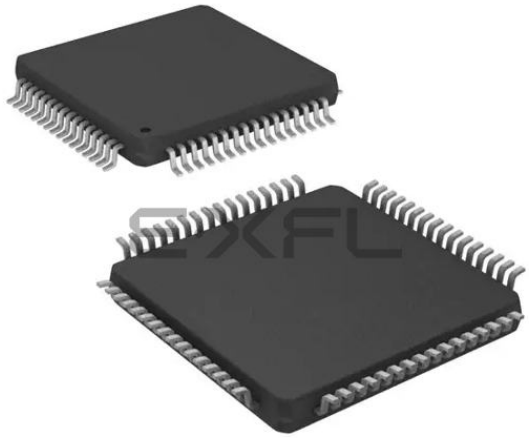

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Details	
Product Status	Not For New Designs
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	CANbus, EBI/EMI, SMBus (2-Wire/I²C), SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, Temp Sensor, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f047-gqr

2. Absolute Maximum Ratings

Table 2.1. Absolute Maximum Ratings*

Parameter	Conditions	Min	Typ	Max	Units
Ambient temperature under bias		–55	—	125	°C
Storage Temperature		–65	—	150	°C
Voltage on any Pin (except V_{DD}, Port I/O, and JTAG pins) with respect to DGND		–0.3	—	V_{DD} + 0.3	V
Voltage on any Port I/O Pin, /RST, and JTAG pins with respect to DGND		–0.3	—	5.8	V
Voltage on V_{DD} with respect to DGND		–0.3	—	4.2	V
Maximum Total current through V_{DD}, AV+, DGND, and AGND		—	—	800	mA
Maximum output current sunk by any Port pin		—	—	100	mA
Maximum output current sunk by any other I/O pin		—	—	50	mA
Maximum output current sourced by any Port pin		—	—	100	mA
Maximum output current sourced by any other I/O pin		—	—	50	mA

***Note:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Due to special I/O design requirements of the High Voltage Difference Amplifier, undue electrical over-voltage stress (i.e., ESD) experienced by these pads may result in impedance degradation of these inputs (HVAIN+ and HVAIN–). For this reason, care should be taken to ensure proper handling and use as typically required to prevent ESD damage to electrostatically sensitive CMOS devices (e.g., static-free workstations, use of grounding straps, over-voltage protection in end-applications, etc.)

SFR Definition 5.6. ADC0CN: ADC0 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
AD0EN	AD0TM	AD0INT	AD0BUSY	AD0CM1	AD0CM0	AD0WINT	AD0LJST	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0xE8
SFR Page: 0

Bit7: AD0EN: ADC0 Enable Bit.
0: ADC0 Disabled. ADC0 is in low-power shutdown.
1: ADC0 Enabled. ADC0 is active and ready for data conversions.

Bit6: AD0TM: ADC Track Mode Bit
0: When the ADC is enabled, tracking is continuous unless a conversion is in process
1: Tracking Defined by AD0CM1-0 bits

Bit5: AD0INT: ADC0 Conversion Complete Interrupt Flag.
This flag must be cleared by software.
0: ADC0 has not completed a data conversion since the last time this flag was cleared.
1: ADC0 has completed a data conversion.

Bit4: AD0BUSY: ADC0 Busy Bit.
Read:
0: ADC0 Conversion is complete or a conversion is not currently in progress. AD0INT is set to logic 1 on the falling edge of AD0BUSY.
1: ADC0 Conversion is in progress.
Write:
0: No Effect.
1: Initiates ADC0 Conversion if AD0CM1-0 = 00b

Bit3-2: AD0CM1-0: ADC0 Start of Conversion Mode Select.
If AD0TM = 0:
00: ADC0 conversion initiated on every write of ‘1’ to AD0BUSY.
01: ADC0 conversion initiated on overflow of Timer 3.
10: ADC0 conversion initiated on rising edge of external CNVSTR0.
11: ADC0 conversion initiated on overflow of Timer 2.
If AD0TM = 1:
00: Tracking starts with the write of ‘1’ to AD0BUSY and lasts for 3 SAR clocks, followed by conversion.
01: Tracking started by the overflow of Timer 3 and last for 3 SAR clocks, followed by conversion.
10: ADC0 tracks only when CNVSTR0 input is logic low; conversion starts on rising CNVSTR0 edge.
11: Tracking started by the overflow of Timer 2 and last for 3 SAR clocks, followed by conversion.

Bit1: AD0WINT: ADC0 Window Compare Interrupt Flag.
This bit must be cleared by software.
0: ADC0 Window Comparison Data match has not occurred since this flag was last cleared.
1: ADC0 Window Comparison Data match has occurred.

Bit0: AD0LJST: ADC0 Left Justify Select.
0: Data in ADC0H:ADC0L registers are right-justified.
1: Data in ADC0H:ADC0L registers are left-justified.

5.4. ADC0 Programmable Window Detector

The ADC0 Programmable Window Detector continuously compares the ADC0 output to user-programmed limits, and notifies the system when an out-of-bound condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD0WINT in ADC0CN) can also be used in polled mode. The high and low bytes of the reference words are loaded into the ADC0 Greater-Than and ADC0 Less-Than registers (ADC0GTH, ADC0GTL, ADC0LTH, and ADC0LTL). Reference comparisons are shown starting on page 63. Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC0GTx and ADC0LTx registers.

SFR Definition 5.9. ADC0GTH: ADC0 Greater-Than Data High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC5
SFR Page: 0

Bits7-0: High byte of ADC0 Greater-Than Data Word.

SFR Definition 5.10. ADC0GTL: ADC0 Greater-Than Data Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC4
SFR Page: 0

Bits7-0: Low byte of ADC0 Greater-Than Data Word.

SFR Definition 5.11. ADC0LTH: ADC0 Less-Than Data High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC7
SFR Page: 0

Bits7-0: High byte of ADC0 Less-Than Data Word.

Table 5.2. 12-Bit ADC0 Electrical Characteristics

V_{DD} = 3.0 V, AV+ = 3.0 V, VREF = 2.40 V (REFBE = 0), PGA Gain = 1, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			12		bits
Integral Nonlinearity		—	—	±1	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	—	±1	LSB
Offset Error	Note 1	—	0.5±3	—	LSB
Full Scale Error	Differential mode; See Note 1	—	0.4±3	—	LSB
Offset Temperature Coefficient		—	±0.25	—	ppm/°C
Dynamic Performance (10 kHz sine-wave input, 0 to 1 dB below Full Scale, 100 ksps)					
Signal-to-Noise Plus Distortion		66	—	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	–75	—	dB
Spurious-Free Dynamic Range		—	80	—	dB
Conversion Rate					
Maximum SAR Clock Frequency		—	—	2.5	MHz
Conversion Time in SAR Clocks		16	—	—	clocks
Track/Hold Acquisition Time		1.5	—	—	µs
Throughput Rate		—	—	100	ksps
Analog Inputs					
Input Voltage Range	Single-ended operation	0	—	VREF	V
Common-mode Voltage Range	Differential operation	AGND	—	AV+	V
Input Capacitance		—	10	—	pF
Temperature Sensor					
Nonlinearity	Notes 1, 2	—	±1	—	°C
Absolute Accuracy	Notes 1, 2	—	±3	—	°C
Gain	Notes 1, 2	—	2.86 ±0.034	—	mV/°C
Offset	Notes 1, 2 (Temp = 0 °C)	—	0.776 ±0.009	—	V
Power Specifications					
Power Supply Current (AV+ supplied to ADC)	Operating Mode, 100 ksps	—	450	900	µA
Power Supply Rejection		—	±0.3	—	mV/V

Notes:
1. Represents one standard deviation from the mean.
2. Includes ADC offset, gain, and linearity variations.

Table 5.3. High-Voltage Difference Amplifier Electrical Characteristics

V_{DD} = 3.0 V, AV+ = 3.0 V, V_{REF} = 3.0 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Analog Inputs					
Differential range	peak-to-peak	—	—	60	V
Common Mode Range	(HVAIN+) – (HVAIN–) = 0 V	–60	—	+60	V
Analog Output					
Output Voltage Range		0.1	—	2.9	V
DC Performance					
Common Mode Rejection Ratio	Vcm= –10 V to +10 V, Rs=0	44	52	—	dB
Offset Voltage		—	±3	—	mV
Noise	HVCAP floating	—	500	—	nV/rtHz
Nonlinearity	G = 1	—	72	—	dB
Dynamic Performance					
Small Signal Bandwidth	G = 0.05	—	3	—	MHz
Small Signal Bandwidth	G = 1	—	150	—	kHz
Slew Rate		—	2	—	V/µs
Settling Time	0.01%, G = 0.05, 10 V step	—	10	—	µs
Input/Output Impedance					
Differential (HVAIN+) input		—	105	—	kΩ
Differential (HVAIN-) input		—	98	—	kΩ
Common Mode input		—	51	—	kΩ
HVCAP		—	5	—	kΩ
Power Specification					
Quiescent Current		—	450	1000	µA

Table 7.1. AMUX Selection Chart (AMX2AD2-0 and AMX2CF3-0 bits)

		AMX2AD2-0							
		000	**001**	**010**	**011**	**100**	**101**	**110**	**111**
AMX2CF Bits 3-0	**0000**	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
	0001	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
	0010	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	P1.6	P1.7
	0011	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	P1.6	P1.7
	0100	P1.0	P1.1	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	0101	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	0110	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	0111	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	P1.6	P1.7
	1000	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1001	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1010	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1011	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	P1.4	P1.5	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1100	P1.0	P1.1	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1101	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	P1.2	P1.3	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1110	P1.0	P1.1	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)
	1111	+(P1.0) -(P1.1)	-(P1.0) +(P1.1)	+(P1.2) -(P1.3)	-(P1.2) +(P1.3)	+(P1.4) -(P1.5)	-(P1.4) +(P1.5)	+(P1.6) -(P1.7)	-(P1.6) +(P1.7)

7.3. ADC2 Programmable Window Detector

The ADC2 Programmable Window Detector continuously compares the ADC2 output to user-programmed limits, and notifies the system when an out-of-bound condition is detected. This is especially effective in an interrupt-driven system, saving code space and CPU bandwidth while delivering faster system response times. The window detector interrupt flag (AD2WINT in ADC2CN) can also be used in polled mode. The reference words are loaded into the ADC2 Greater-Than and ADC2 Less-Than registers (ADC2GT and ADC2LT). Notice that the window detector flag can be asserted when the measured data is inside or outside the user-programmed limits, depending on the programming of the ADC2GT and ADC2LT registers.

SFR Definition 7.6. ADC2GT: ADC2 Greater-Than Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								11111111
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC4
SFR Page: 2

Bits7-0: High byte of ADC2 Greater-Than Data Word.

SFR Definition 7.7. ADC2LT: ADC2 Less-Than Data

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xC6
SFR Page: 2

Bits7-0: Low byte of ADC2 Greater-Than Data Word.

7.3.1. Window Detector in Single-Ended Mode

Figure 7.5 shows two example window comparisons for Single-ended mode, with ADC2LT = 0x20 and ADC2GT = 0x10. In Single-ended mode, the codes vary from 0 to VREF x (255/256) and are represented as 8-bit unsigned integers. In the left example, an AD2WINT interrupt will be generated if the ADC2 conversion word (ADC2) is within the range defined by ADC2GT and ADC2LT (if 0x10 < ADC2 < 0x20). In the right example, and AD2WINT interrupt will be generated if ADC2 is outside of the range defined by ADC2GT and ADC2LT (if ADC2 < 0x10 or ADC2 > 0x20).

SFR Definition 9.1. REF0CN: Reference Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	AD0VRS	AD2VRS	TEMPE	BIASE	REFBE	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0xD1
SFR Page: 0

Bits7-5: UNUSED. Read = 000b; Write = don't care.
Bit4: AD0VRS: ADC0 Voltage Reference Select
0: ADC0 voltage reference from VREF0 pin.
1: ADC0 voltage reference from DAC0 output (C8051F040/2 only).
Bit3: AD2VRS: ADC2 Voltage Reference Select (C8051F040/2 only).
0: ADC2 voltage reference from VREF2 pin.
1: ADC2 voltage reference from AV+.
Bit2: TEMPE: Temperature Sensor Enable Bit.
0: Internal Temperature Sensor Off.
1: Internal Temperature Sensor On.
Bit1: BIASE: ADC/DAC Bias Generator Enable Bit. (Must be '1' if using ADC or DAC).
0: Internal Bias Generator Off.
1: Internal Bias Generator On.
Bit0: REFBE: Internal Reference Buffer Enable Bit.
0: Internal Reference Buffer Off.
1: Internal Reference Buffer On. Internal voltage reference is driven on the VREF pin.

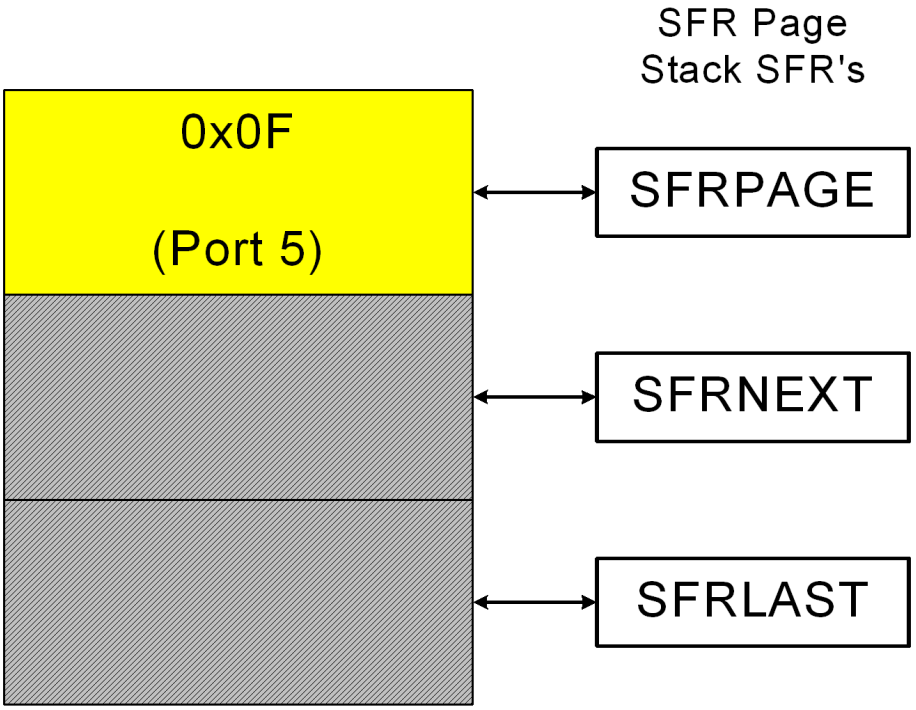

Figure 12.4. SFR Page Stack While Using SFR Page 0x0F To Access Port 5

While CIP-51 executes in-line code (writing values to Port 5 in this example), an ADC2 Window Comparator Interrupt occurs. The CIP-51 vectors to the ADC2 Window Comparator ISR and pushes the current SFR Page value (SFR Page 0x0F) into SFRNEXT in the SFR Page Stack. The SFR page needed to access ADC2's SFR's is then automatically placed in the SFRPAGE register (SFR Page 0x02). SFRPAGE is considered the "top" of the SFR Page Stack. Software can now access the ADC2 SFR's. Software may switch to any SFR Page by writing a new value to the SFRPAGE register at any time during the ADC2 ISR to access SFR's that are not on SFR Page 0x02. See Figure 12.5.

Table 12.2. Special Function Register (SFR) Memory Map

ADDRESS	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	SFR PAGE
F8	SPI0CN CAN0CN P7	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL1	PCA0CPH1	WDTCN **(ALL PAGES)**	0 1 2 3 F
F0	B **(ALL PAGES)**						EIP1 **(ALL PAGES)**	EIP2 **(ALL PAGES)**	0 1 2 3 F
E8	ADC0CN ADC2CN P6	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	PCA0CPL4	PCA0CPH4	RSTSRC	0 1 2 3 F
E0	ACC **(ALL PAGES)**	PCA0CPL5 XBR0	PCA0CPH5 XBR1	XBR2	XBR3		EIE1 **(ALL PAGES)**	EIE2 **(ALL PAGES)**	0 1 2 3 F
D8	PCA0CN CAN0DATL P5	PCA0MD CAN0DATH	PCA0CPM0 CAN0ADR	PCA0CPM1 CAN0TST	PCA0CPM2	PCA0CPM3	PCA0CPM4	PCA0CPM5	0 1 2 3 F
D0	PSW **(ALL PAGES)**	REF0CN	DAC0L DAC1L	DAC0H DAC1H	DAC0CN DAC1CN		HVA0CN		0 1 2 3 F
C8	TMR2CN TMR3CN TMR4CN P4	TMR2CF TMR3CF TMR4CF	RCAP2L RCAP3L RCAP4L	RCAP2H RCAP3H RCAP4H	TMR2L TMR3L TMR4L	TMR2H TMR3H TMR4H		SMB0CR	0 1 2 3 F
C0	SMB0CN CAN0STA	SMB0STA	SMB0DAT	SMB0ADR	ADC0GTL ADC2GT	ADC0GTH	ADC0LTL ADC2LT	ADC0LTH	0 1 2 3 F
B8	IP **(ALL PAGES)**	SADEN0	AMX0CF AMX2CF	AMX0SL AMX2SL	ADC0CF ADC2CF	AMX0PRT	ADC0L ADC2	ADC0H	0 1 2 3 F
	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)	

12.17. Power Management Modes

The CIP-51 core has two software programmable power management modes: Idle and Stop. Idle mode halts the CPU while leaving the external peripherals and internal clocks active. In Stop mode, the CPU is halted, all interrupts and timers (except the Missing Clock Detector) are inactive, and the internal oscillator is stopped. Since clocks are running in Idle mode, power consumption is dependent upon the system clock frequency and the number of peripherals left in active mode before entering Idle. Stop mode consumes the least power. SFR Definition 12.18 describes the Power Control Register (PCON) used to control the CIP-51's power management modes.

Although the CIP-51 has Idle and Stop modes built in (as with any standard 8051 architecture), power management of the entire MCU is better accomplished by enabling/disabling individual peripherals as needed. Each analog peripheral can be disabled when not in use and put into low power mode. Digital peripherals, such as timers or serial buses, draw little power whenever they are not in use. Turning off the oscillator saves even more power, but requires a reset to restart the MCU.

12.17.1.Idle Mode

Setting the Idle Mode Select bit (PCON.0) causes the CIP-51 to halt the CPU and enter Idle mode as soon as the instruction that sets the bit completes. All internal registers and memory maintain their original data. All analog and digital peripherals can remain active during Idle mode.

Idle mode is terminated when an enabled interrupt or /RST is asserted. The assertion of an enabled interrupt will cause the Idle Mode Selection bit (PCON.0) to be cleared and the CPU to resume operation. The pending interrupt will be serviced and the next instruction to be executed after the return from interrupt (RETI) will be the instruction immediately following the one that set the Idle Mode Select bit. If Idle mode is terminated by an internal or external reset, the CIP-51 performs a normal reset sequence and begins program execution at address 0x0000.

If enabled, the WDT will eventually cause an internal watchdog reset and thereby terminate the Idle mode. This feature protects the system from an unintended permanent shutdown in the event of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the Idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to **Section 13.7** for more information on the use and configuration of the WDT.

Note: Any instruction that sets the IDLE bit should be immediately followed by an instruction that has 2 or more opcode bytes. For example:

```
// in 'C':
PCON |= 0x01;         // set IDLE bit
PCON  = PCON;         // ... followed by a 3-cycle dummy instruction

; in assembly:
ORL PCON, #01h        ; set IDLE bit
MOV PCON, PCON        ; ... followed by a 3-cycle dummy instruction
```

If the instruction following the write of the IDLE bit is a single-byte instruction and an interrupt occurs during the execution phase of the instruction that sets the IDLE bit, the CPU may not wake from IDLE mode when a future interrupt occurs.

SFR Definition 14.1. OSCICL: Internal Oscillator Calibration

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								Variable
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8B
SFR Page: F

Bits 7-0: OSCICL: Internal Oscillator Calibration Register
This register calibrates the internal oscillator period. The reset value for OSCICL defines the internal oscillator base frequency. The reset value is factory calibrated to generate an internal oscillator frequency of 24.5 MHz.

SFR Definition 14.2. OSCICN: Internal Oscillator Control

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	Reset Value
IOSCEN	IFRDY	-	-	-	-	IFCN1	IFCN0	11000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8A
SFR Page: F

Bit7: IOSCEN: Internal Oscillator Enable Bit.
0: Internal Oscillator Disabled
1: Internal Oscillator Enabled
Bit6: IFRDY: Internal Oscillator Frequency Ready Flag.
0: Internal Oscillator is not running at programmed frequency.
1: Internal Oscillator is running at programmed frequency.
Bits5-2: Reserved.
Bits1-0: IFCN1-0: Internal Oscillator Frequency Control Bits.
00: SYSCLK derived from Internal Oscillator divided by 8.
01: SYSCLK derived from Internal Oscillator divided by 4.
10: SYSCLK derived from Internal Oscillator divided by 2.
11: SYSCLK derived from Internal Oscillator divided by 1.

16.2. Configuring the External Memory Interface

Configuring the External Memory Interface consists of five steps:

1. Select EMIF on Low Ports (P3, P2, P1, and P0) or High Ports (P7, P6, P5, and P4).
2. Configure the Output Modes of the port pins as either push-pull or open-drain.
3. Select Multiplexed mode or Non-multiplexed mode.
4. Select the memory mode (on-chip only, split mode without bank select, split mode with bank select, or off-chip only).
5. Set up timing to interface with off-chip memory or peripherals.

Each of these five steps is explained in detail in the following sections. The Port selection, Multiplexed mode selection, and Mode bits are located in the EMI0CF register shown in SFR Definition 16.2.

16.3. Port Selection and Configuration

The External Memory Interface can appear on Ports 3, 2, 1, and 0 (C8051F04x devices) or on Ports 7, 6, 5, and 4 (C8051F040/2/4/6 devices only), depending on the state of the PRTSEL bit (EMI0CF.5). If the lower Ports are selected, the EMIFLE bit (XBR2.1) must be set to a '1' so that the Crossbar will skip over P0.7 (/WR), P0.6 (/RD), and, if multiplexed mode is selected, P0.5 (ALE). For more information about the configuring the Crossbar, see **Section "17.1. Ports 0 through 3 and the Priority Crossbar Decoder" on page 204**.

The External Memory Interface claims the associated Port pins for memory operations ONLY during the execution of an off-chip MOVX instruction. Once the MOVX instruction has completed, control of the Port pins reverts to the Port latches or to the Crossbar (on Ports 3, 2, 1, and 0). See **Section "17. Port Input/ Output" on page 203** for more information about the Crossbar and Port operation and configuration. **The Port latches should be explicitly configured as push-pull to 'park' the External Memory Interface pins in a dormant state, most commonly by setting them to a logic 1**.

During the execution of the MOVX instruction, the External Memory Interface will explicitly disable the drivers on all Port pins that are acting as Inputs (Data[7:0] during a READ operation, for example). The Output mode of the Port pins (whether the pin is configured as Open-Drain or Push-Pull) is unaffected by the External Memory Interface operation, and remains controlled by the PnMDOUT registers. In most cases, the output modes of all EMIF pins should be configured for push-pull mode. See **Section "17.1.2. Configuring the Output Modes of the Port Pins" on page 206**.

16.4.2. Non-multiplexed Configuration

In Non-multiplexed mode, the Data Bus and the Address Bus pins are not shared. An example of a Non-multiplexed Configuration is shown in Figure 16.2. See **Section "16.6.1. Non-multiplexed Mode" on page 196** for more information about Non-multiplexed operation.

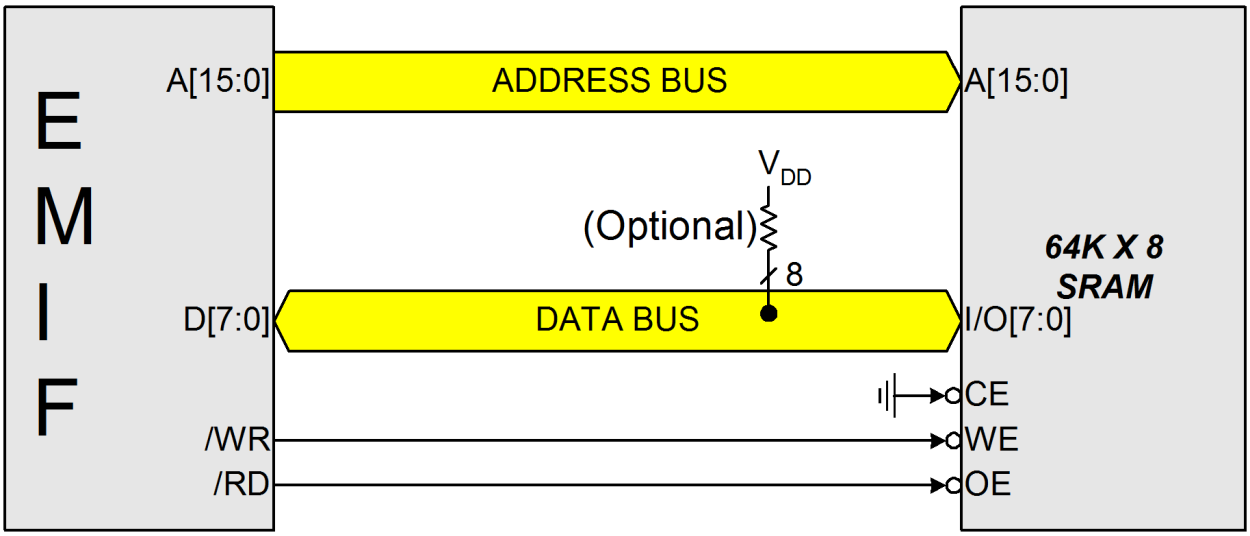

Figure 16.2. Non-multiplexed Configuration Example

16.5.3. Split Mode with Bank Select

When EMI0CF.[3:2] are set to ‘10’, the XRAM memory map is split into two areas, on-chip space and off-chip space.

- Effective addresses below the 4k boundary will access on-chip XRAM space.
- Effective addresses above the 4k boundary will access off-chip space.
- 8-bit MOVX operations use the contents of EMI0CN to determine whether the memory access is on-chip or off-chip. The upper 8-bits of the Address Bus A[15:8] are determined by EMI0CN, and the lower 8-bits of the Address Bus A[7:0] are determined by R0 or R1. All 16-bits of the Address Bus A[15:0] are driven in “Bank Select” mode.
- 16-bit MOVX operations use the contents of DPTR to determine whether the memory access is on-chip or off-chip, and the full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

16.5.4. External Only

When EMI0CF[3:2] are set to ‘11’, all MOVX operations are directed to off-chip space. On-chip XRAM is not visible to the CPU. This mode is useful for accessing off-chip memory located between 0x0000 and the 4k boundary.

- 8-bit MOVX operations ignore the contents of EMI0CN. The upper Address bits A[15:8] are not driven (identical behavior to an off-chip access in “Split Mode without Bank Select” described above). This allows the user to manipulate the upper address bits at will by setting the Port state directly. The lower 8-bits of the effective address A[7:0] are determined by the contents of R0 or R1.
- 16-bit MOVX operations use the contents of DPTR to determine the effective address A[15:0]. The full 16-bits of the Address Bus A[15:0] are driven during the off-chip transaction.

16.6. Timing

The timing parameters of the External Memory Interface can be configured to enable connection to devices having different setup and hold time requirements. The Address Setup time, Address Hold time, /RD and
/WR strobe widths, and in multiplexed mode, the width of the ALE pulse are all programmable in units of SYSCLK periods through EMI0TC, shown in SFR Definition 16.3, and EMI0CF[1:0].

The timing for an off-chip MOVX instruction can be calculated by adding 4 SYSCLK cycles to the timing parameters defined by the EMI0TC register. Assuming non-multiplexed operation, the minimum execution time for an off-chip XRAM operation is 5 SYSCLK cycles (1 SYSCLK for /RD or /WR pulse + 4 SYSCLKs). For multiplexed operations, the Address Latch Enable signal will require a minimum of 2 additional SYSCLK cycles. Therefore, the minimum execution time of an off-chip XRAM operation in multiplexed mode is 7 SYSCLK cycles (2 SYSCLKs for /ALE, 1 for /RD or /WR + 4 SYSCLKs). The programmable setup and hold times default to the maximum delay settings after a reset.

Table 16.1 lists the AC parameters for the External Memory Interface, and Figure 16.4 through Figure 16.9 show the timing diagrams for the different External Memory Interface modes and MOVX operations.

16.6.1.2.8-bit MOVX without Bank Select: EMI0CF[4:2] = '101' or '111'.

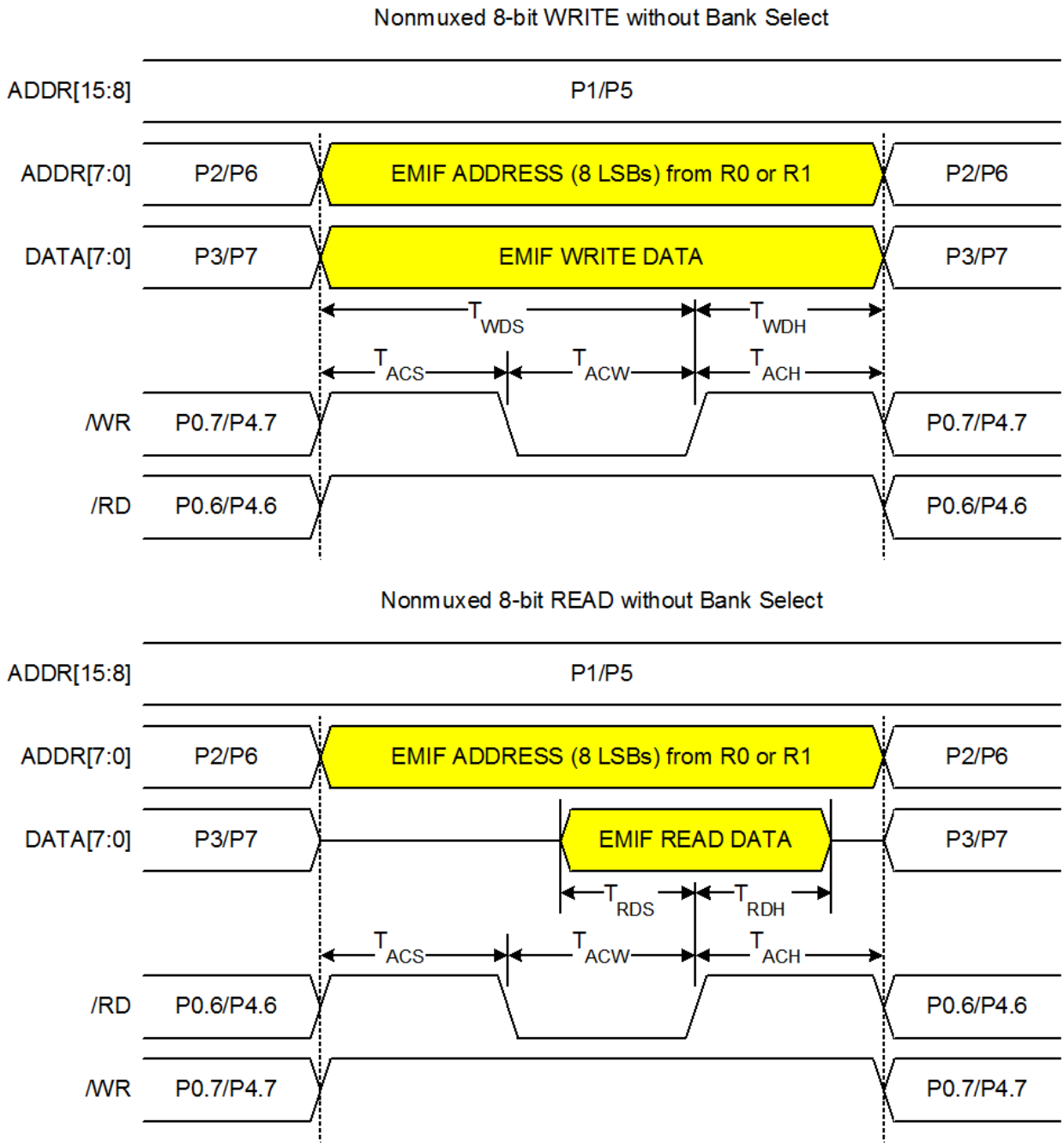

Figure 16.5. Non-multiplexed 8-bit MOVX without Bank Select Timing

20.3. SPI0 Slave Mode Operation

When SPI0 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI0 logic counts SCK edges. When 8 bits have been shifted through the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI0DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI0DAT. Writes to SPI0DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will wait until the byte is transferred before loading it with the transmit buffer's contents.

When configured as a slave, SPI0 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI0 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. Note that the NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 20.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

3-wire slave mode is active when NSSMD1 (SPI0CN.3) = 0 and NSSMD0 (SPI0CN.2) = 0. NSS is not used in this mode, and does not get mapped to an external port pin through the crossbar. Since there is no way of uniquely addressing the device in 3-wire slave mode, SPI0 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI0 with the SPIEN bit. Figure 20.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.

20.4. SPI0 Interrupt Sources

When SPI0 interrupts are enabled, the following four flags will generate an interrupt when they are set to logic 1:

Note: All of the following interrupt bits must be cleared by software.

1. The SPI Interrupt Flag, SPIF (SPI0CN.7) is set to logic 1 at the end of each byte transfer. This flag can occur in all SPI0 modes.
2. The Write Collision Flag, WCOL (SPI0CN.6) is set to logic 1 if a write to SPI0DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI0DAT will be ignored, and the transmit buffer will not be written.This flag can occur in all SPI0 modes.
3. The Mode Fault Flag MODF (SPI0CN.5) is set to logic 1 when SPI0 is configured as a master, and for multi-master mode and the NSS pin is pulled low. When a Mode Fault occurs, the MSTEN and SPIEN bits in SPI0CN are set to logic 0 to disable SPI0 and allow another master device to access the bus.
4. The Receive Overrun Flag RXOVRN (SPI0CN.4) is set to logic 1 when configured as a slave, and a transfer is completed and the receive buffer still holds an unread byte from a previous transfer. The new byte is not transferred to the receive buffer, allowing the previously received data byte to be read. The data byte which caused the overrun is lost.

21.1.4. Mode 3: 9-Bit UART, Variable Baud Rate

Mode 3 uses the Mode 2 transmission protocol with the Mode 1 baud rate generation. Mode 3 operation transmits 11 bits: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The baud rate is derived from Timer 1 or Timer 2, 3, or 4 overflows, as defined by Equation 21.1 and Equation 21.3. Multiprocessor communications and hardware address recognition are supported, as described in **Section 21.2**.

21.2. Multiprocessor Communications

Modes 2 and 3 support multiprocessor communication between a master processor and one or more slave processors by special use of the ninth data bit and the built-in UART0 address recognition hardware. When a master processor wants to transmit to one or more slaves, it first sends an address byte to select the target(s). An address byte differs from a data byte in that its ninth bit is logic 1; in a data byte, the ninth bit is always set to logic 0. UART0 will recognize as “valid” (i.e., capable of causing an interrupt) **two** types of addresses: (1) a *masked* address and (2) a *broadcast* address **at any given time**. Both are described below.

22.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB81 (SCON1.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB81 (SCON1.2) and the stop bit is ignored.

Data transmission begins when an instruction writes a data byte to the SBUF1 register. The TI1 Transmit Interrupt Flag (SCON1.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN1 Receive Enable bit (SCON1.4) is set to '1'. After the stop bit is received, the data byte will be loaded into the SBUF1 receive register if the following conditions are met: (1) RI1 must be logic 0, and (2) if MCE1 is logic 1, the 9th bit must be logic 1 (when MCE1 is logic 0, the state of the ninth data bit is unimportant). If these conditions are met, the eight bits of data are stored in SBUF1, the ninth bit is stored in RB81, and the RI1 flag is set to '1'. If the above conditions are not met, SBUF1 and RB81 will not be loaded and the RI1 flag will not be set to '1'. A UART1 interrupt will occur if enabled when either TI1 or RI1 is set to '1'.

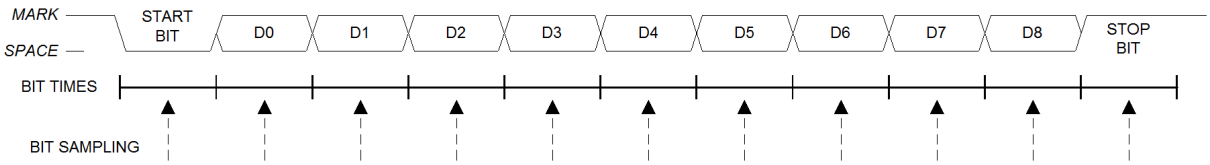

Figure 22.5. 9-Bit UART Timing Diagram

SFR Definition 22.1. SCON1: Serial Port 1 Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
S1MODE	-	MCE1	REN1	TB81	RB81	TI1	RI1	01000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x98
SFR Page: 1

Bit7: S1MODE: Serial Port 1 Operation Mode.
This bit selects the UART1 Operation Mode.
0: Mode 0: 8-bit UART with Variable Baud Rate
1: Mode 1: 9-bit UART with Variable Baud Rate

Bit6: UNUSED. Read = 1b. Write = don't care.

Bit5: MCE1: Multiprocessor Communication Enable.
The function of this bit is dependent on the Serial Port 0 Operation Mode.
Mode 0: Checks for valid stop bit.
0: Logic level of stop bit is ignored.
1: RI1 will only be activated if stop bit is logic level 1.
Mode 1: Multiprocessor Communications Enable.
0: Logic level of ninth bit is ignored.
1: RI1 is set and an interrupt is generated only when the ninth bit is logic 1.

Bit4: REN1: Receive Enable.
This bit enables/disables the UART receiver.
0: UART1 reception disabled.
1: UART1 reception enabled.

Bit3: TB81: Ninth Transmission Bit.
The logic level of this bit will be assigned to the ninth transmission bit in 9-bit UART Mode. It is not used in 8-bit UART Mode. Set or cleared by software as required.

Bit2: RB81: Ninth Receive Bit.
RB81 is assigned the value of the STOP bit in Mode 0; it is assigned the value of the 9th data bit in Mode 1.

Bit1: TI1: Transmit Interrupt Flag.
Set by hardware when a byte of data has been transmitted by UART1 (after the 8th bit in 8-bit UART Mode, or at the beginning of the STOP bit in 9-bit UART Mode). When the UART1 interrupt is enabled, setting this bit causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software.

Bit0: RI1: Receive Interrupt Flag.
Set to '1' by hardware when a byte of data has been received by UART1 (set at the STOP bit sampling time). When the UART1 interrupt is enabled, setting this bit to '1' causes the CPU to vector to the UART1 interrupt service routine. This bit must be cleared manually by software.