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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Last Time Buy
Core Processor	SH-2A
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, SCI, Serial Sound
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/ds72611rp100fpv

The clock pulse generator blocks function as follows:

(1) PLL Circuit 1

PLL circuit 1 multiplies the input clock frequency from the CKIO pin by 1, 2, 3, 4, 6, or 8. The multiplication rate is set by the frequency control register. When this is done, the phase of the rising edge of the bus clock is controlled so that it will agree with the phase of the rising edge of the CKIO pin.

(2) PLL Circuit 2

PLL circuit 2 multiplies the input clock frequency from the crystal oscillator or EXTAL pin by 2 or 4. The multiplication rate is fixed according to the clock operating mode. The clock operating mode is specified by the MD_CLK1 and MD_CLK0 pins. For details on the clock operating mode, see table 4.2.

Note that the settings of these pins cannot be changed during operation. If changed, the operation of this LSI cannot be guaranteed.

(3) Crystal Oscillator

The crystal oscillator is an oscillation circuit in which a crystal resonator is connected to the XTAL pin or EXTAL pin. This can be used according to the clock operating mode.

(4) Divider

Divider generates a clock signal at the operating frequency used by the CPU or peripheral clock. The operating frequency can be 1, 1/2, 1/3, 1/4, 1/6, 1/8, or 1/12 times the output frequency of PLL circuit 1, as long as it stays at or above the clock frequency of the CKIO pin. The division ratio is set in the frequency control register (FRQCR).

(5) Clock Frequency Control Circuit

The clock frequency control circuit controls the clock frequency using the MD_CLK1 and MD_CLK0 pins and the frequency control register (FRQCR).

(6) Standby Control Circuit

The standby control circuit controls the states of the clock pulse generator and other modules during clock switching, or in sleep, software, and deep standby mode.

7.4.5 Usage Examples

(1) Break Condition Specified for C Bus Instruction Fetch Cycle

(Example 1-1)

- Register specifications

  BAR_0 = H'00000404, BAMR_0 = H'00000000, BBR_0 = H'0054, BAR_1 = H'00008010, BAMR_1 = H'00000006, BBR_1 = H'0054, BDR_1 = H'00000000, BDMR_1 = H'00000000, BRCR = H'00000020

  <Channel 0>

  Address: H'00000404, Address mask: H'00000000

  Bus cycle: C bus/instruction fetch (after instruction execution)/read (operand size is not included in the condition)

  <Channel 1>

  Address: H'00008010, Address mask: H'00000006

  Data: H'00000000, Data mask: H'00000000

  Bus cycle: C bus/instruction fetch (before instruction execution)/read (operand size is not included in the condition)

  A user break occurs after an instruction of address H'00000404 is executed or before instructions of addresses H'00008010 to H'00008016 are executed.

(Example 1-2)

- Register specifications

  BAR_0 = H'00027128, BAMR_0 = H'00000000, BBR_0 = H'005A, BAR_1= H'00031415, BAMR_1 = H'00000000, BBR_1 = H'0054, BDR_1 = H'00000000, BDMR_1 = H'00000000, BRCR = H'00000000

  <Channel 0>

  Address: H'00027128, Address mask: H'00000000

  Bus cycle: C bus/instruction fetch (before instruction execution)/write/word

  <Channel 1>

  Address: H'00031415, Address mask: H'00000000

  Data: H'00000000, Data mask: H'00000000

  Bus cycle: C bus/instruction fetch (before instruction execution)/read (operand size is not included in the condition)

  On channel 0, a user break does not occur since instruction fetch is not a write cycle. On channel 1, a user break does not occur since instruction fetch is performed for an even address.

11.5 Completion of DMA Transfer and Interrupts

11.5.1 Completion of DMA Transfer

When the value H'0000 0000 is transferred from the working byte count register to the DMA current byte count register (DMCBCTn) (all data has been transferred), the DMA transfer end condition is fulfilled and one DMA transfer is complete.

The operations following detection of the DMA transfer end condition are as follows.

- DMA transfer end condition

  The DMA transfer end condition detection bit (DEDET) for the corresponding channel in the DMA transfer end detection register (DMEDET) is set to "1".

- Interrupt request generation

  An interrupt request is generated for the interrupt controller according to the settings of the DMA interrupt control register (DMICNT) and the DMA common interrupt control register (DMICNTA).

- Output of DMA end signal

  The DMA end signal (DTENDm) is output according the setting of the DMA end signal output control bit (DTCM) in the DMA mode register (DMMODn) for the channel.

- Clearing the DMA transfer enable bit (DEN)

  If the DMA transfer enable clear bit (ECLR) in DMA control register B (DMCNTBn) is set to "1", the DEN bit in the DMA control register B (DMCNTBn) is cleared to "0", suspending any subsequent DMA transfer for the channel.

  If the DMA transfer enable clear bit (ECLR) is clear ("0"), the DEN bit is not cleared.

- Reloading the source address register

  If the DMA source address reload function enable bit (SRLOD) in the DMA control register A (DMCNTAn) is set to "1", the DMA current source address register (DMCSADRn) is reloaded with the value in the DMA reload source address register (DMRSADRn).

- Reloading the destination address register

  If the DMA destination address reload function enable bit (DRLOD) in DMA control register A (DMCNTAn) is set to "1", the DMA current destination address register (DMCDADRn) is reloaded with the value in the DMA reload destination address register (DMRDADRn).

Table 12.12 TIORH_0 (Channel 0)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_0 Function**	**TIOC0B Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	X		Input capture at both edges
	1	X	X		Capture input source is channel 1/count clock Input capture at TCNT_1 count-up/count-down

[Legend]

X: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

(3) Cascaded Operation Example (b)

Figure 12.22 illustrates the operation when TCNT_1 and TCNT_2 have been cascaded and the I2AE bit in TICCR has been set to 1 to include the TIOC2A pin in the TGRA_1 input capture conditions. In this example, the IOA0 to IOA3 bits in TIOR_1 have selected the TIOC1A rising edge for the input capture timing while the IOA0 to IOA3 bits in TIOR_2 have selected the TIOC2A rising edge for the input capture timing.

Under these conditions, the rising edge of both TIOC1A and TIOC2A is used for the TGRA_1 input capture condition. For the TGRA_2 input capture condition, the TIOC2A rising edge is used.

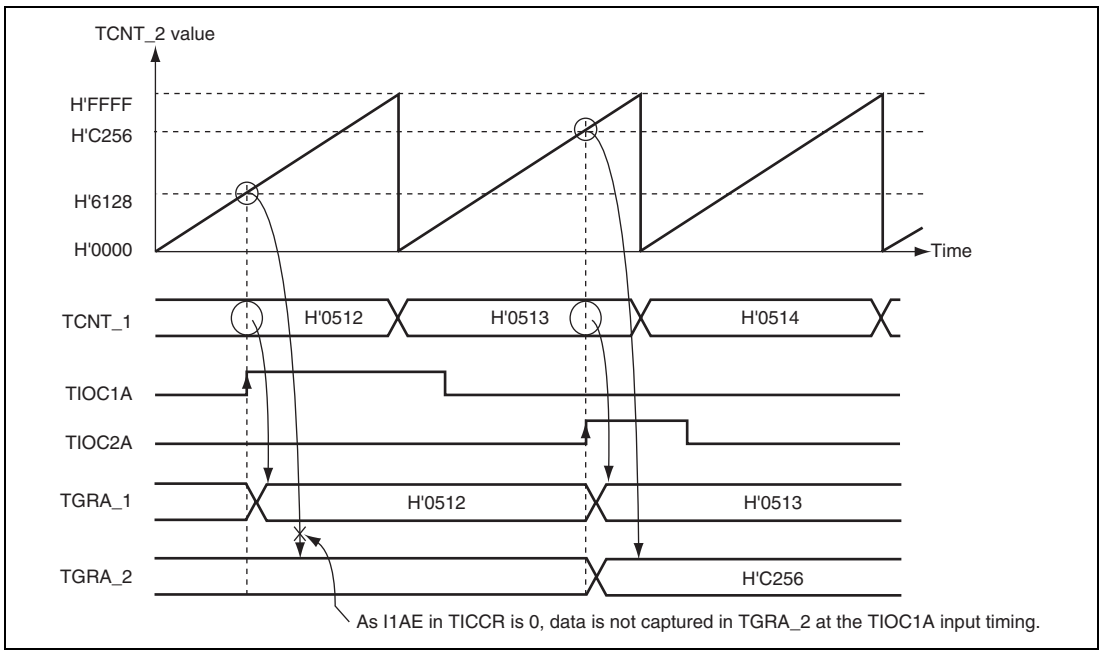


Figure 12.22 Cascaded Operation Example (b)

(c) Initialization

In complementary PWM mode, there are six registers that must be initialized. In addition, there is a register that specifies whether to generate dead time (it should be used only when dead time generation should be disabled).

Before setting complementary PWM mode with bits MD3 to MD0 in the timer mode register (TMDR), the following initial register values must be set.

TGRC_3 operates as the buffer register for TGRA_3, and should be set with 1/2 the PWM carrier cycle + dead time Td. The timer cycle buffer register (TCBR) operates as the buffer register for the timer cycle data register (TCDR), and should be set with 1/2 the PWM carrier cycle. Set dead time Td in the timer dead time data register (TDDR).

When dead time is not needed, the TDER bit in the timer dead time enable register (TDER) should be cleared to 0, TGRC_3 and TGRA_3 should be set to 1/2 the PWM carrier cycle + 1, and TDDR should be set to 1.

Set the respective initial PWM duty values in buffer registers TGRD_3, TGRC_4, and TGRD_4.

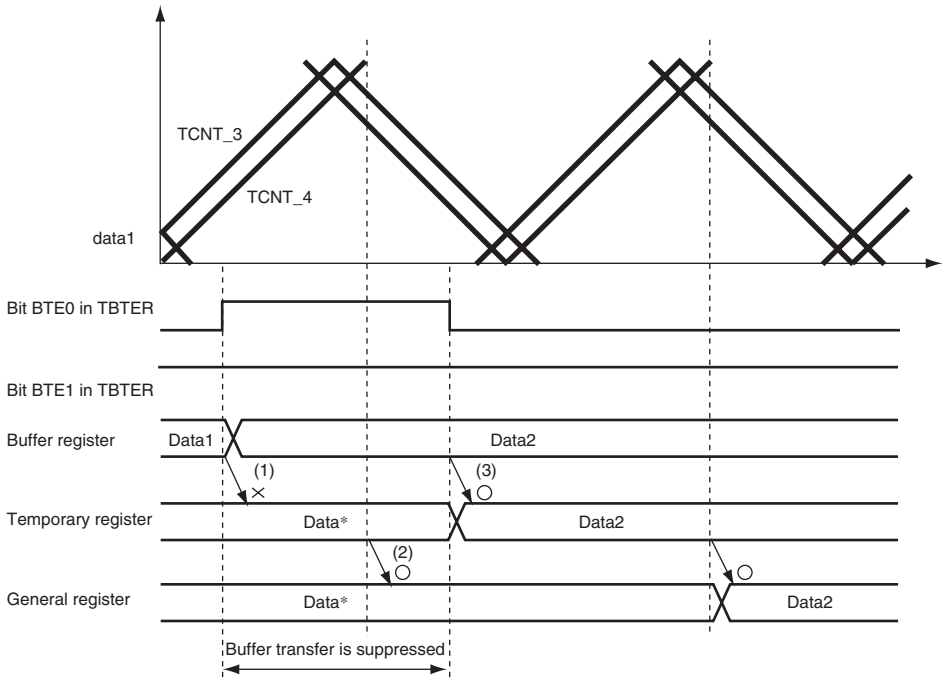
The values set in the five buffer registers excluding TDDR are transferred simultaneously to the corresponding compare registers when complementary PWM mode is set.

Set TCNT_4 to H'0000 before setting complementary PWM mode.

Table 12.56 Registers and Counters Requiring Initialization

Register/Counter	Set Value
TGRC_3	1/2 PWM carrier cycle + dead time Td (1/2 PWM carrier cycle + 1 when dead time generation is disabled by TDER)
TDDR	Dead time Td (1 when dead time generation is disabled by TDER)
TCBR	1/2 PWM carrier cycle
TGRD_3, TGRC_4, TGRD_4	Initial PWM duty value for each phase
TCNT_4	H'0000

Note: The TGRC_3 set value must be the sum of 1/2 the PWM carrier cycle set in TCBR and dead time Td set in TDDR. When dead time generation is disabled by TDER, TGRC_3 must be set to 1/2 the PWM carrier cycle + 1.



[Legend]

(1) No data is transferred from the buffer register to the temporary register in the buffer transfer-disabled period (bits BTE1 and BTE0 in TBTER are set to 0 and 1, respectively).
(2) Data is transferred from the temporary register to the general register even in the buffer transfer-disabled period.
(3) After buffer transfer is enabled, data is transferred from the buffer register to the temporary register.

Note: * When buffer transfer at the crest is selected.

Figure 12.70 Example of Operation when Buffer Transfer is Suppressed (BTE1 = 0 and BTE0 = 1)

(23) Operation when Error Occurs during Complementary PWM Mode Operation, and Operation is Restarted in Complementary PWM Mode

Figure 12.149 shows an explanatory diagram of the case where an error occurs in complementary PWM mode and operation is restarted in complementary PWM mode after re-setting (when operation is restarted using the cycle and duty settings at the time the counter was stopped).

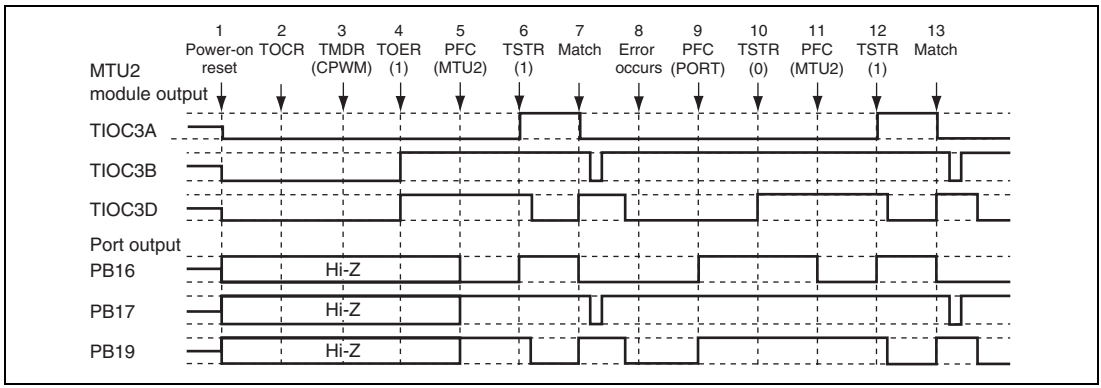


Figure 12.149 Error Occurrence in Complementary PWM Mode, Recovery in Complementary PWM Mode

1 to 10 are the same as in figure 12.147.

11. Set MTU2 output with the PFC.
12. Operation is restarted by TSTR.
13. The complementary PWM waveform is output on compare-match occurrence.

13.8.3 Conflict between TCNT Write and Increment

If a TCNT input clock pulse is generated during the T_2 state of a TCNT write cycle, the write takes priority and the counter is not incremented as shown in figure 13.13.

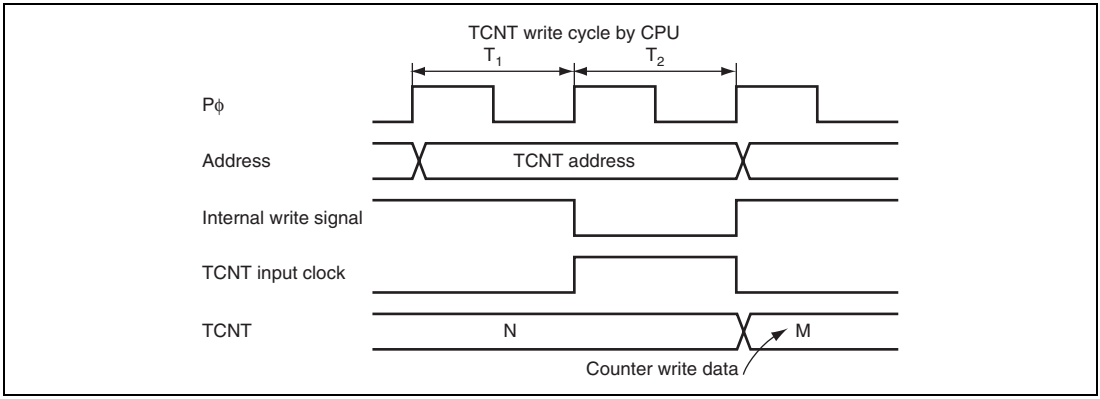


Figure 13.13 Conflict between TCNT Write and Increment

13.8.4 Conflict between TCOR Write and Compare Match

If a compare match event occurs during the T_2 state of a TCOR write cycle, the TCOR write takes priority and the compare match signal is inhibited as shown in figure 13.14.

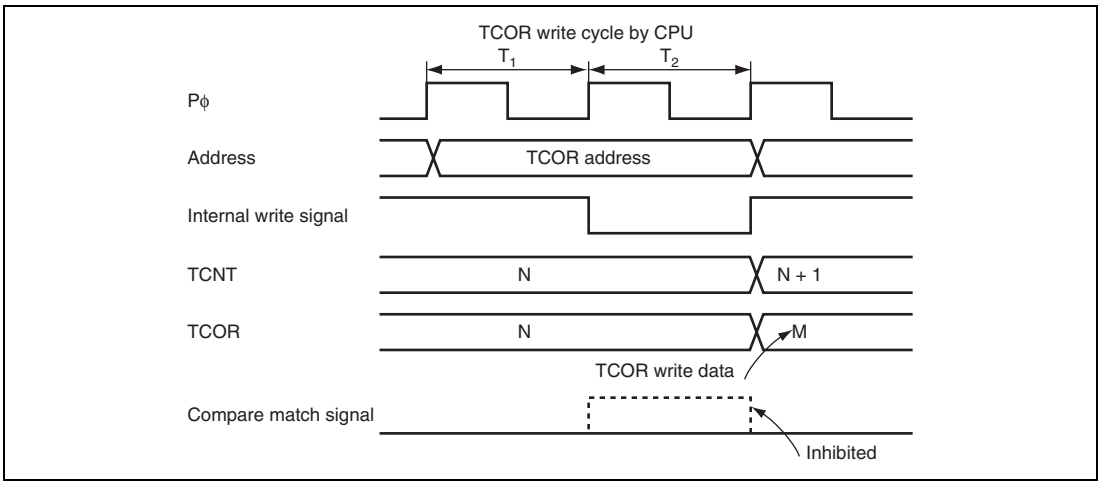
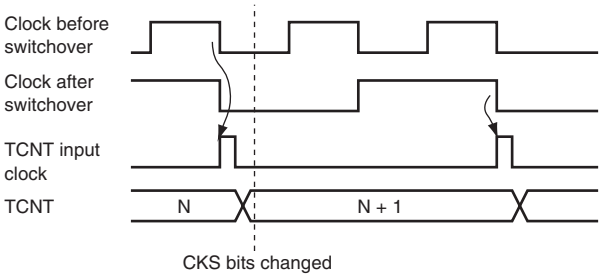
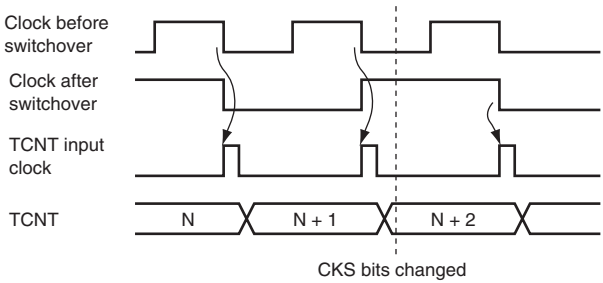
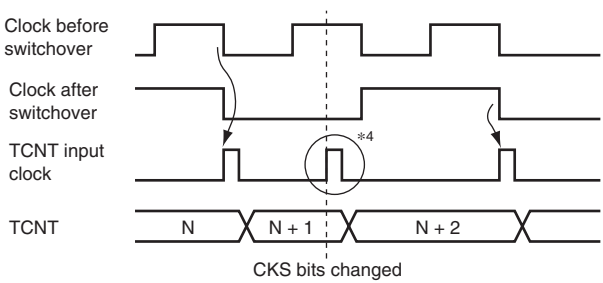


Figure 13.14 Conflict between TCOR Write and Compare Match

Table 13.5 Switching of Internal Clock and TCNT Operation

No.	Timing to Change CKS1 and CKS0 Bits	TCNT Clock Operation
1	Switching from low to low*1	
2	Switching from low to high*2	
3	Switching from high to low*3	

(1) Transmit/Receive Formats

The data length is fixed at eight bits. No parity bit can be added.

(2) Clock

An internal clock generated by the on-chip baud rate generator by the setting of the C/$\overline{A}$ bit in SCSMR and CKE[1:0] in SCSCR, or an external clock input from the SCK pin can be selected as the SCIF transmit/receive clock.

When the SCIF operates on an internal clock, it outputs the clock signal at the SCK pin. Eight clock pulses are output per transmitted or received character. When the SCIF is not transmitting or receiving, the clock signal remains in the high state. When only receiving, the clock signal outputs while the RE bit of SCSCR is 1 and the number of data in receive FIFO is more than the receive FIFO data trigger number.

(3) Transmitting and Receiving Data

- **SCIF Initialization (Clocked Synchronous Mode)**

Before transmitting, receiving, or changing the mode or communication format, the software must clear the TE and RE bits to 0 in the serial control register (SCSCR), then initialize the SCIF. Clearing TE to 0 initializes the transmit shift register (SCTSR). Clearing RE to 0, however, does not initialize the RDF, PER, FER, and ORER flags and receive data register (SCRDR), which retain their previous contents.

- Mailbox-0

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	NMC	0	0	MBC[2:0]			0	0	0	0	DLC[3:0]			
Initial value:	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Note: MBC[1] of MB0 is always "1".

- Mailbox-15 to 1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	NMC	ATX	DART	MBC[2:0]			0	0	0	0	DLC[3:0]			
Initial value:	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

NMC (New Message Control): When this bit is set to '0', the Mailbox of which the RXPR or RFPR bit is already set does not store the new message but maintains the old one and sets the UMSR correspondent bit. When this bit is set to '1', the Mailbox of which the RXPR or RFPR bit is already set overwrites with the new message and sets the UMSR correspondent bit.

Important: Please note that if a remote frame is overwritten with a data frame or vice versa could be that both RXPR and RFPR flags (together with UMSR) are set for the same Mailbox. In this case the RTR bit within the Mailbox Control Field should be relied upon.

NMC	Description
0	Overrun mode (Initial value)
1	Overwrite mode

ATX (Automatic Transmission of Data Frame): When this bit is set to '1' and a Remote Frame is received into the Mailbox DLC is stored. Then, a Data Frame is transmitted from the same Mailbox using the current contents of the message data and updated DLC by setting the corresponding TXPR automatically. The scheduling of transmission is still governed by ID priority or Mailbox priority as configured with the Message Transmission Priority control bit (MCR.2). In order to use this function, MBC[2:0] needs to be programmed to be B'001. When a transmission is performed by this function, the DLC (Data Length Code) to be used is the one that has been received. Application needs to guarantee that the DLC of the remote frame correspond to the DLC of the data frame requested.

Important: When ATX is used and MBC = B'001 the filter for the IDE bit cannot be used since ID of remote frame has to be exactly the same as that of data frame as the reply message.

19.6.5 Reconfiguration of Mailbox

When re-configuration of Mailboxes is required, the following procedures should be taken.

(1) Change configuration of transmit box

Two cases are possible.

- Change of ID, RTR, IDE, LAFM, Data, DLC, NMC, ATX, DART
  This change is possible only when MBC = B'000. Confirm that the corresponding TXPR is not set. The configuration (except MBC bit) can be changed at any time.
- Change from transmit to receive configuration (MBC)
  Confirm that the corresponding TXPR is not set. The configuration can be changed only in Halt or reset state. Please note that it might take longer for RCAN-ET to transit to halt state if it is receiving or transmitting a message (as the transition to the halt state is delayed until the end of the reception/transmission), and also RCAN-ET will not be able to receive/transmit messages during the Halt state.
  In case RCAN-ET is in the Bus Off state the transition to halt state depends on the configuration of the bit 6 of MCR and also bit and 14 of MCR.

(2) Change configuration (ID, RTR, IDE, LAFM, Data, DLC, NMC, ATX, DART) of receive box or Change receive box to transmit box

The configuration can be changed only in Halt Mode.

RCAN-ET will not lose a message if the message is currently on the CAN bus and RCAN-ET is a receiver. RCAN-ET will be moving into Halt Mode after completing the current reception. Please note that it might take longer if RCAN-ET is receiving or transmitting a message (as the transition to the halt state is delayed until the end of the reception/transmission), and also RCAN-ET will not be able to receive/transmit messages during the Halt Mode.

In case RCAN-ET is in the Bus Off state the transition to halt mode depends on the configuration of the bit 6 and 14 of MCR.

22.7.6 Influences on Absolute Precision

Adding capacitance results in coupling with GND, and therefore noise in GND may adversely affect absolute precision. Be sure to connect AVss, etc. to an electrically stable GND.

Care is also required to insure that filter circuits do not communicate with digital signals on the mounting board (i.e., acting as antennas).

22.7.7 Note on Usage in Scan Mode and Multi Mode

Starting conversion immediately after having stopped scan mode or multi mode operation may lead to erroneous results of conversion.

To perform continuous conversion in such cases, set ADST to 0, wait for at least the A/D conversion time for a single channel to elapse, and then start conversion (ADST = 1). (The A/D conversion time for a single channel will vary according to the settings of the ADC registers.)

Section 23 D/A Converter (DAC)

23.1 Features

- Resolution: 8 bits
- Input channels: 2
- Minimum conversion time: Max. 10 μs (with 20 pF load)
- Output voltage: 0 V to AVref
- D/A output hold function in software standby mode
- Module standby mode can be set

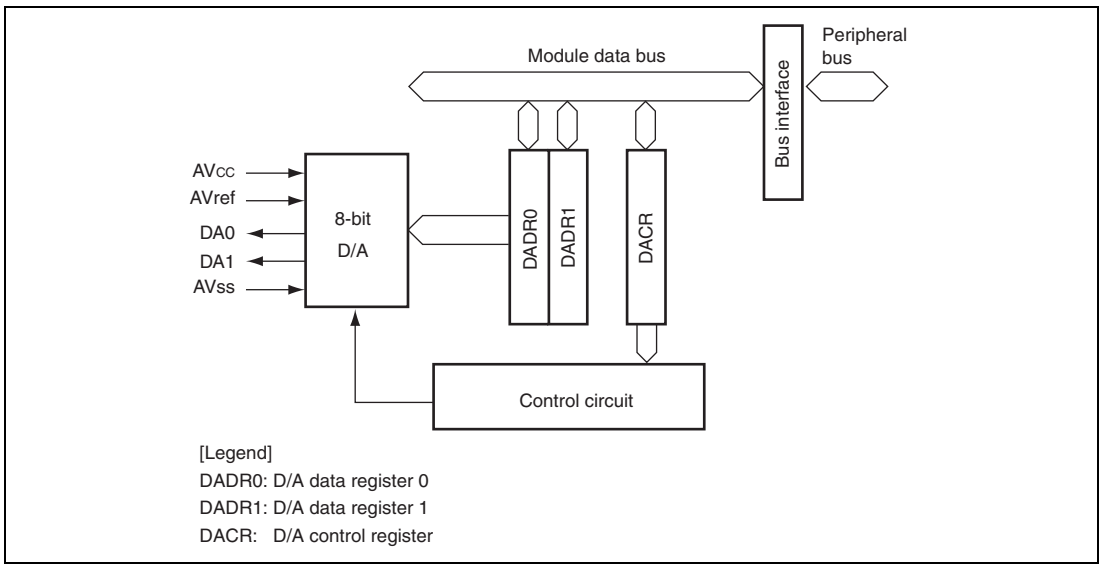


Figure 23.1 Block Diagram of D/A Converter

24.1.3 Port A Port Registers H and L (PAPRH and PAPRL)

PAPRH and PAPRL are 16-bit read-only registers in which bits PA31PR to PA0PR correspond to pins PA31 to PA0. PAPRH and PAPRL are always read as the states of the pins regardless of the PFC setting.

- Port A Port Register H (PAPRH)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PA31PR	PA30PR	PA29PR	PA28PR	PA27PR	PA26PR	PA25PR	PA24PR	PA23PR	PA22PR	PA21PR	PA20PR	PA19PR	PA18PR	PA17PR	PA16PR
Initial value:	PA31	PA30	PA29	PA28	PA27	PA26	PA25	PA24	PA23	PA22	PA21	PA20	PA19	PA18	PA17	PA16
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Port A Port Register L (PAPRL)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PA15PR	PA14PR	PA13PR	PA12PR	PA11PR	PA10PR	PA9PR	PA8PR	PA7PR	PA6PR	PA5PR	PA4PR	PA3PR	PA2PR	PA1PR	PA0PR
Initial value:	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	PA26MD [2:0]	000	R/W	PA26 Mode These bits control the function of the PA26/A26/ DACT3/PINT2B pin. 000: PA26 I/O (port) 001: A26 output (BSC) 010: DACT3 output (DMAC) 011: PINT2B input (INTC) 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	PA25MD [2:0]	000	R/W	PA25 Mode These bits control the function of the PA25/A25/ DACK3/PINT1B pin. 000: PA25 I/O (port) 001: A25 output (BSC) 010: DACK3 output (DMAC) 011: PINT1B input (INTC) 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	PA24MD [1:0]	00	R/W	PA24 Mode These bits control the function of the PA24/A24/ DREQ3/PINT0B pin. 00: PA24 I/O (port) 01: A24 output (BSC) 10: DREQ3 input (DMAC) 11: PINT0B input (INTC)

Register Name	Abbreviation	Number of Bits	Address	Module	Access Size
IEBus reception master address register 2	IEMA2	8	H'FFFF100A	IEB	8
IEBus receive control field register	IERCTL	8	H'FFFF100B		8
IEBus receive message length register	IERBFL	8	H'FFFF100C		8
IEBus lock address register 1	IELA1	8	H'FFFF100E		8
IEBus lock address register 2	IELA2	8	H'FFFF100F		8
IEBus general flag register	IEFLG	8	H'FFFF1010		8
IEBus transmit status register	IETSR	8	H'FFFF1011		8
IEBus transmit interrupt enable register	IEIET	8	H'FFFF1012		8
IEBus receive status register	IERSR	8	H'FFFF1014		8
IEBus receive interrupt enable register	IEIER	8	H'FFFF1015		8
IEBus clock select register	IECKSR	8	H'FFFF1018		8
IEBus transmit data buffer register 001 to 128	IETB001 to IETB128	8	H'FFFF1100 to H'FFFF117F		8
IEBus receive data buffer register 001 to 128	IERB001 to IERB128	8	H'FFFF1200 to H'FFFF127F		8
DMA transfer enable register 0	DREQER0	8	H'FFFF1600	INTC	8, 16, 32
DMA transfer enable register 1	DREQER1	8	H'FFFF1601		8
DMA transfer enable register 2	DREQER2	8	H'FFFF1602		8, 16
DMA transfer enable register 3	DREQER3	8	H'FFFF1603		8
Deep standby cancel source flag register	DSFR	16	H'FFFF1904	SYSTEM	16
Deep standby oscillation stabilization clock select register	DSCNT	8	H'FFFF1906		8
RAM retained area specification register	RAMKP	8	H'FFFF1907		8

31.3.2 Control Signal Timing

Table 31.6 Control Signal Timing

Conditions: $PV_{CC} = V_{CC}R = PLLV_{CC} = 3.0$ V to 3.6 V, $AV_{CC} = 3.0$ V to 3.6 V,
$PV_{CC} - 0.3$ V $\leq AV_{CC} \leq PV_{CC}$, $AV_{ref} = 3.0$ V to AV_{CC},
$PV_{SS} = V_{SS}R = PLLV_{SS} = AV_{SS} = 0$ V

		Bϕ = 60 MHz			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
$\overline{\text{RES}}$ pulse width	t_{RESW}	20*[2]	—	t_{cyc}	Figures 31.4, 31.5, and 31.8
$\overline{\text{RES}}$ setup time*[1]	t_{RESS}	200	—	ns	
$\overline{\text{MRES}}$ pulse width	t_{MRESW}	20*[3]	—	t_{cyc}	
$\overline{\text{MRES}}$ setup time*[1]	t_{MRESS}	200	—	ns	
NMI pulse width	t_{NMIW}	20*[4]	—	t_{cyc}	Figures 31.6 and 31.9
NMI setup time*[1]	t_{NMIS}	150	—	ns	
NMI hold time	t_{NMIH}	10	—	ns	
IRQ7 to IRQ0 pulse width	t_{IRQW}	20*[4]	—	t_{cyc}	
IRQ7 to IRQ0 setup time*[1]	t_{IRQS}	150	—	ns	
IRQ7 to IRQ0 hold time	t_{IRQH}	10	—	ns	
PINT7 to PINT0 setup time*[1]	t_{PINTS}	150	—	ns	

Notes: 1. The $\overline{\text{RES}}$, $\overline{\text{MRES}}$, NMI, IRQ7 to IRQ0 and PINT7 to PINT0 signals are asynchronous signals. When the setup time is satisfied, change of signal level is detected at the rising edge of the clock. If not, the detection can be delayed until the rising edge of the next clock.
2. In software standby mode, deep standby mode or when the clock multiplication ratio is changed, $t_{RESW} = t_{OSC2}$ (min).
3. In software standby mode or deep standby mode, $t_{MRESW} = t_{OSC2}$ (min).
4. In software standby mode or deep standby mode, $t_{NMIW}/t_{IRQW} = t_{OSC3}$ (min).

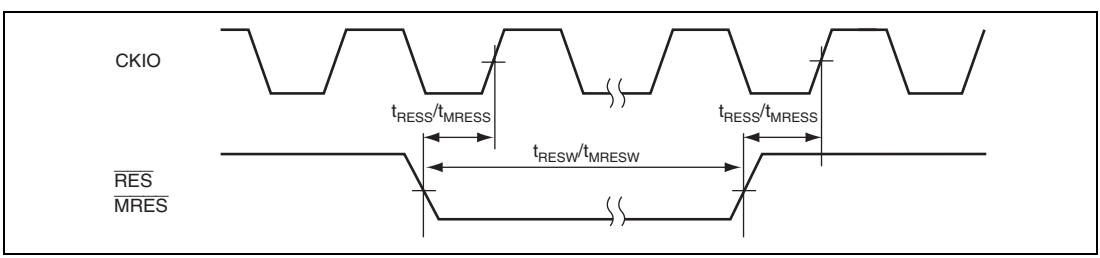
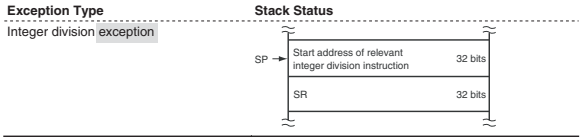
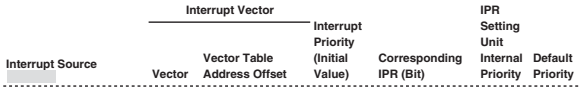
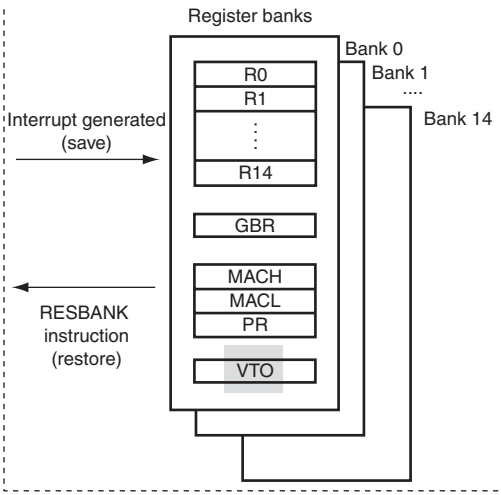


Figure 31.8 Reset Input Timing

Item	Page	Revision (See Manual for Details)
5.9 Stack Status after Exception Handling Ends Table 5.12 Stack Status After Exception Handling Ends	117	Table amended 
6.5 Interrupt Exception Handling Vector Table and Priority Table 6.4 Interrupt Exception Handling Vectors and Priorities	141 to 149	Table amended 
6.8 Register Banks Figure 6.10 Overview of Register Bank Configuration	158	Figure amended 
8.4.4 Notes	202	Description amended 1. Programs that access memory-mapped cache of the operand cache should be placed in a cache-disabled space. Programs that access memory-mapped cache of the instruction cache should be placed in a cache-disabled space, and in each of the beginning and the end of that, two or more read accesses to on-chip peripheral modules or external address space (cache-disabled address) should be executed.
9.4.8 SDRAM Refresh Control Register 1 (SDRFCNT1) Auto-Refresh Request Interval and DRFC Set Value:	227	Description amended DRFC = (Auto-refresh request interval / Bus clock cycle) – 1