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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2A
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, FIFO, I²C, IEBus, SCI, Serial Sound
Peripherals	DMA, POR, PWM, WDT
Number of I/O	104
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LFQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/ds72613rb120fpv

Figure 7.1 shows a block diagram of the UBC.

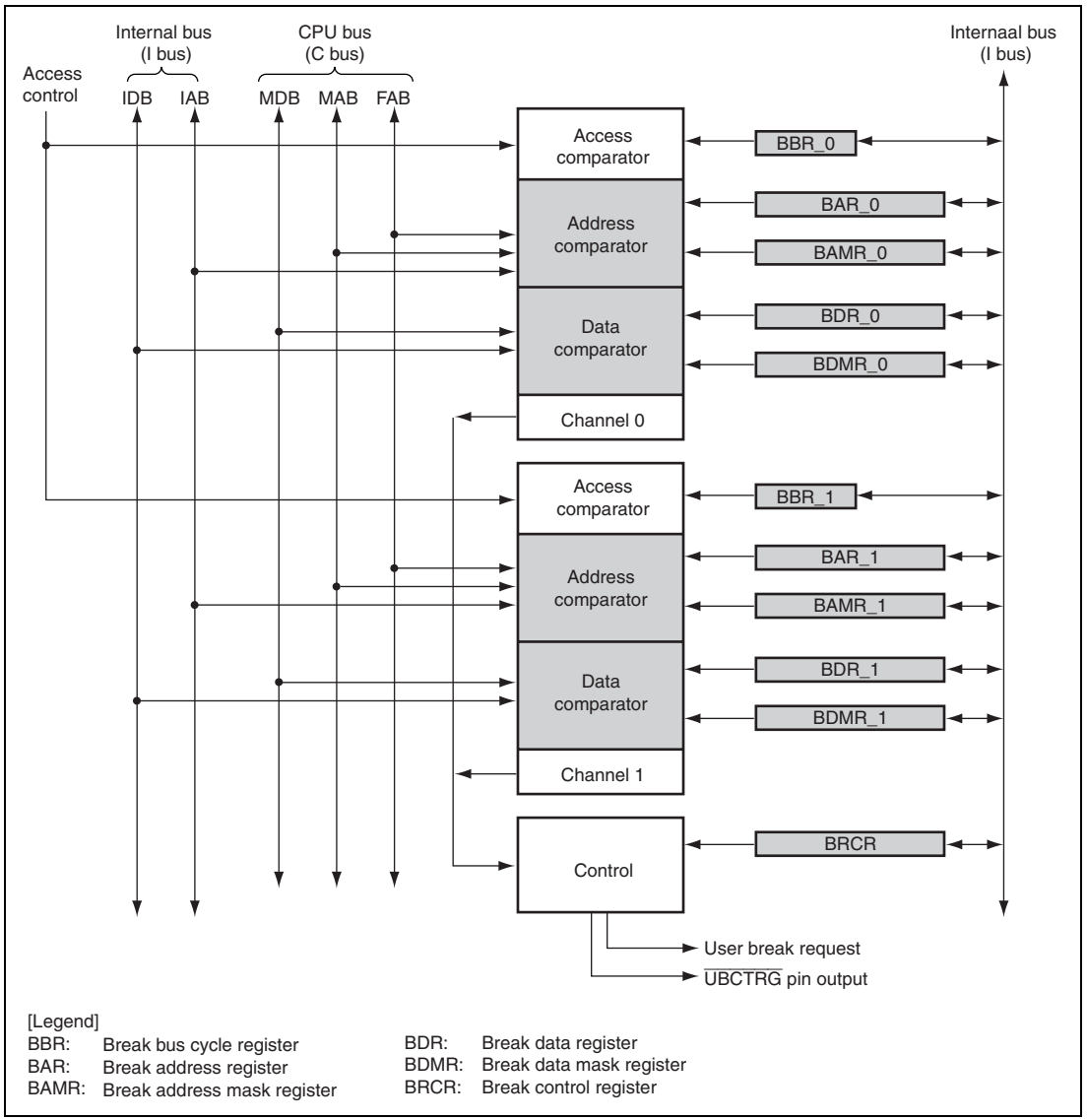


Figure 7.1 Block Diagram of UBC

2. Set this register so that DMA transfer is performed within the correctly aligned address boundaries for the transfer sizes listed below.
   - When the transfer size is set to 16 bits (SZSEL = "001"): (b0) = "0".
   - When the transfer size is set to 32 bits (SZSEL = "010"): (b1, b0) = (0, 0).
3. Only write to this register when single operand transfer is not in process on the corresponding channel (the corresponding DASTS bit in the DMA arbitration status register (DMASTS) is "0") and DMA transfer is disabled (DMST in the DMA activation control register (DMSCNT) or DEN in DMA control register B for the channel (DMCNTBn) is set to "0"). Operation is not guaranteed if this register is written to when both conditions are not satisfied.

11.3.4 DMA Reload Source Address Register (DMRSADR)

DMRSADR is used to set an address for reloading to the DMA current source address register (DMCSADRn).

To enable reloading, set the DMA source address reload function enable bit (SRLOD) in DMA control register A (DMCNTAn) for the channel to "1". In this case, set both the DMA current source address register (DMCSADRn) and DMA reload source address register (DMRSADRn).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RSA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RSA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RSA	Undefined	R/W	Holds source address bits A31 to A0 for reloading

Note: Set this register so that DMA transfer is performed within the correctly aligned address boundaries for the transfer sizes listed below.
- When the transfer size is set to 16 bits (SZSEL = "001"): (b0) = "0".
- When the transfer size is set to 32 bits (SZSEL = "010"): (b1, b0) = (0, 0).

Bit	Bit Name	Initial Value	R/W	Description
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17, 16	STRG[1:0]	00	R/W	Input Sense Mode Selection These bits specify input sense modes for DMA request signals input to the DMAC. The requesting source is that selected from among the possible sources by the DMA request source selection bits (DCTG). Select rising edge sense by setting these bits to "00" if the software trigger (DCTG = "000000") and pins DREQ0 to DREQ3 are selected as the source for DMA requests. Select falling edge sense by setting the bits to "10" when operation is with IIC3, SCIF, SSI, RCAN-ET, MTU2, ADC, or ROM-DEC (DCTG = "000101" to "100101"). Table 11.4 shows the relationships between DMA request sources and the possible input sense modes. 00: Rising edge 01: High level 10: Falling edge 11: Low level
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	BRLOD	0	R/W	DMA Byte Count Reload Function Enable This bit specifies whether to reload the byte counter or not when the DMA transfer end condition is detected. When this bit is cleared to "0", no reload is executed. When this bit is set to "1" and the DMA transfer end condition is detected, the DMA current byte counter register (DMCBCTn) is reloaded with the value in the DMA reload byte count register (DMRBCTn). 0: Byte count reload function disabled 1: Byte count reload function enabled

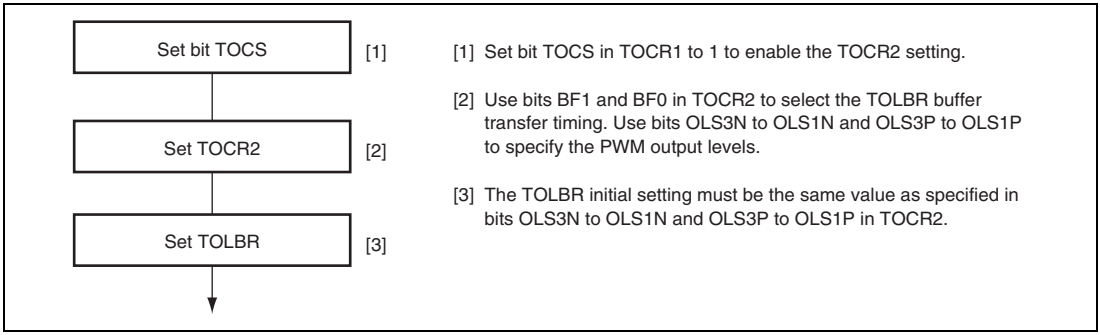


Figure 12.3 PWM Output Level Setting Procedure in Buffer Operation

12.3.22 Timer Gate Control Register (TGCR)

TGCR is an 8-bit readable/writable register that controls the waveform output necessary for brushless DC motor control in reset-synchronized PWM mode/complementary PWM mode. These register settings are ineffective for anything other than complementary PWM mode/reset-synchronized PWM mode.

Bit:	7	6	5	4	3	2	1	0
	—	BDC	N	P	FB	WF	VF	UF
Initial value:	1	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial value	R/W	Description
7	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
6	BDC	0	R/W	Brushless DC Motor This bit selects whether to make the functions of this register (TGCR) effective or ineffective. 0: Ordinary output 1: Functions of this register are made effective

- When TGR is an input capture register

  When input capture occurs, the value in TCNT is transferred to TGR and the value previously held in the timer general register is transferred to the buffer register.

  This operation is illustrated in figure 12.15.

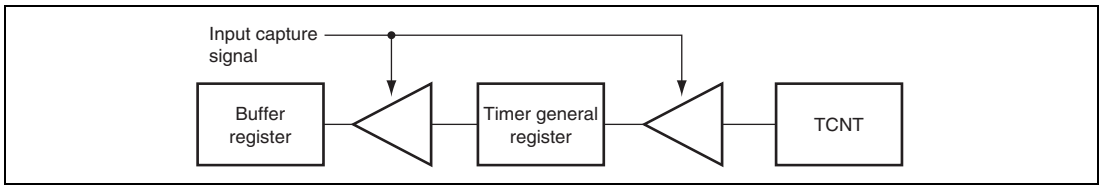


Figure 12.15 Input Capture Buffer Operation

(1) Example of Buffer Operation Setting Procedure

Figure 12.16 shows an example of the buffer operation setting procedure.

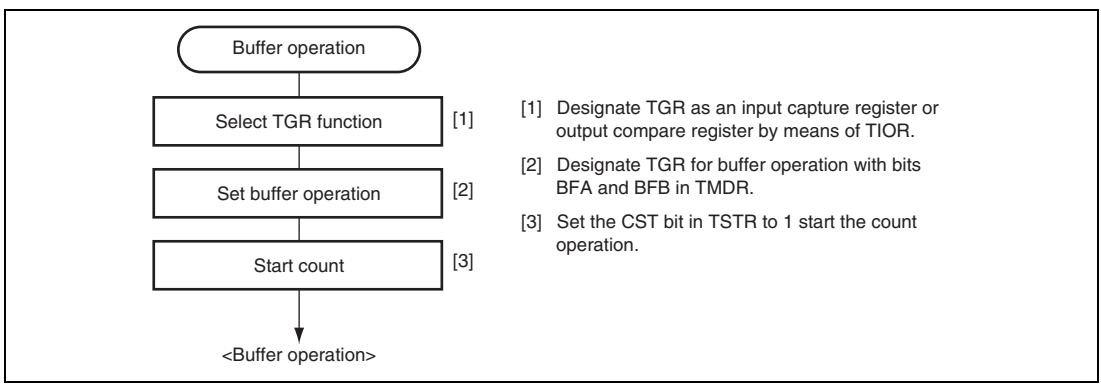


Figure 12.16 Example of Buffer Operation Setting Procedure

(j) 10. Complementary PWM Mode PWM Output Generation Method

In complementary PWM mode, 3-phase output is performed of PWM waveforms with a non-overlap time between the positive and negative phases. This non-overlap time is called the dead time.

A PWM waveform is generated by output of the output level selected in the timer output control register in the event of a compare-match between a counter and data register. While TCNTS is counting, data register and temporary register values are simultaneously compared to create consecutive PWM pulses from 0 to 100%. The relative timing of on and off compare-match occurrence may vary, but the compare-match that turns off each phase takes precedence to secure the dead time and ensure that the positive phase and negative phase on times do not overlap. Figures 12.46 to 12.48 show examples of waveform generation in complementary PWM mode.

The positive phase/negative phase off timing is generated by a compare-match with the solid-line counter, and the on timing by a compare-match with the dotted-line counter operating with a delay of the dead time behind the solid-line counter. In the T1 period, compare-match **a** that turns off the negative phase has the highest priority, and compare-matches occurring prior to **a** are ignored. In the T2 period, compare-match **c** that turns off the positive phase has the highest priority, and compare-matches occurring prior to **c** are ignored.

In normal cases, compare-matches occur in the order **a** → **b** → **c** → **d** (or **c** → **d** → **a'** → **b'**), as shown in figure 12.46.

If compare-matches deviate from the **a** → **b** → **c** → **d** order, since the time for which the negative phase is off is less than twice the dead time, the figure shows the positive phase is not being turned on. If compare-matches deviate from the **c** → **d** → **a'** → **b'** order, since the time for which the positive phase is off is less than twice the dead time, the figure shows the negative phase is not being turned on.

If compare-match **c** occurs first following compare-match **a**, as shown in figure 12.47, compare-match **b** is ignored, and the negative phase is turned off by compare-match **d**. This is because turning off of the positive phase has priority due to the occurrence of compare-match **c** (positive phase off timing) before compare-match **b** (positive phase on timing) (consequently, the waveform does not change since the positive phase goes from off to off).

Similarly, in the example in figure 12.48, compare-match **a'** with the new data in the temporary register occurs before compare-match **c**, but other compare-matches occurring up to **c**, which turns off the positive phase, are ignored. As a result, the negative phase is not turned on.

Thus, in complementary PWM mode, compare-matches at turn-off timings take precedence, and turn-on timing compare-matches that occur before a turn-off timing compare-match are ignored.

15.3.11 Hour Alarm Register (RHRAR)

RHRAR is an alarm register corresponding to the BCD coded hour counter RHRCNT of the RTC. When the ENB bit is set to 1, a comparison with the RHRCNT value is performed. From among RSECAR/RMINAR/RHRAR/RWKAR/RDAYAR/RMONAR/RCR3, the counter and alarm register comparison is performed only on those with ENB bits set to 1, and if each of those coincides, an alarm flag of RCR1 is set to 1.

The assignable range is from 00 through 23 + ENB bits (practically in BCD), otherwise operation errors occur.

The ENB bit in RHRAR is initialized by a power-on reset or in deep standby mode. The other bits are not initialized by a power-on reset or manual reset, or in deep standby and software standby modes.

Bit:	7	6	5	4	3	2	1	0
	ENB	—	10 hours		1 hour			
Initial value:	0	0	—	—	—	—	—	—
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

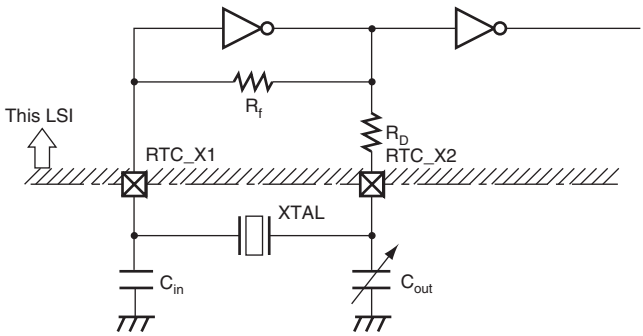
Bit	Bit Name	Initial Value	R/W	Description
7	ENB	0	R/W	When this bit is set to 1, a comparison with the RHRCNT value is performed.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	10 hours	Undefined	R/W	Ten's position of hours setting value
3 to 0	1 hour	Undefined	R/W	One's position of hours setting value

15.5.4 Crystal Oscillator Circuit for RTC

Crystal oscillator circuit constants (recommended values) for the RTC are shown in table 15.3, and the RTC crystal oscillator circuit in figure 15.6.

Table 15.3 Crystal Oscillator Circuit Constants (Recommended Values)

f_{osc}	C_{in}	C_{out}
32.768 kHz	10 to 22 pF	10 to 22 pF



Notes: 1. Select either the C_{in} or C_{out} side for frequency adjustment variable capacitor according to requirements such as frequency range, degree of stability, etc.
2. Built-in resistance value R_f (Typ value) = 10 MΩ, R_D (Typ value) = 400 kΩ
3. C_{in} and C_{out} values include floating capacitance due to the wiring. Take care when using a ground plane.
4. The crystal oscillation stabilization time may differ depending on the mounted circuit component constants, stray capacitance, and so forth, so a suitable value should be determined in consultation with the resonator manufacturer.
5. Place the crystal resonator and load capacitors C_{in} and C_{out} as close as possible to the chip. Make wiring length as short as possible. Do not allocate signal lines close to oscillation circuit.
(Correct oscillation may not be possible if there is externally induced noise in the RTC_X1 and RTC_X2 pins.)
6. Ensure that the wiring of the crystal oscillator connection pins (RTC_X1 and RTC_X2) is routed as far away as possible from the power lines (except GND) and signal lines.
7. When not using a crystal oscillation circuit for RTC, fix the RTC_X1 pin (pull-up, pull-down, connect to power supply, or connect to ground) and leave the RTC_X2 pin open.

Figure 15.6 Example of Connecting Crystal Oscillator Circuit for RTC

16.3.1 Receive Shift Register (SCRSR)

SCRSR receives serial data. Data input at the RxD pin is loaded into SCRSR in the order received, LSB (bit 0) first, converting the data to parallel form. When one byte has been received, it is automatically transferred to the receive FIFO data register (SCFRDR).

The CPU cannot read or write to SCRSR directly.

Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	—	—	—	—	—	—	—	—

16.3.2 Receive FIFO Data Register (SCFRDR)

SCFRDR is a 16-byte FIFO register that stores serial receive data. The SCIF completes the reception of one byte of serial data by moving the received data from the receive shift register (SCRSR) into SCFRDR for storage. Continuous reception is possible until 16 bytes are stored. The CPU can read but not write to SCFRDR. If data is read when there is no receive data in the SCFRDR, the value is undefined.

When SCFRDR is full of receive data, subsequent serial data is lost.

SCFRDR is initialized to an undefined value by a power-on reset or in deep standby mode.

Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R

Table 16.3 SCSMR Settings

		SCSMR Settings	
n	**Clock Source**	**CKS1**	**CKS0**
0	Pϕ	0	0
1	Pϕ/4	0	1
2	Pϕ/16	1	0
3	Pϕ/64	1	1

The bit rate error in asynchronous is given by the following formula:

$$\text{Error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N + 1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

Table 16.4 lists examples of SCBRR settings in asynchronous mode, and table 16.5 lists examples of SCBRR settings in clocked synchronous mode.

Table 16.4 Bit Rates and SCBRR Settings (Asynchronous Mode) (1)

	Pϕ (MHz)											
	5			6			6.144			7.3728		
Bit Rate (bit/s)	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**	**n**	**N**	**Error (%)**
110	2	88	–0.25	2	106	–0.44	2	108	0.08	2	130	–0.07
150	2	64	0.16	2	77	0.16	2	79	0.00	2	95	0.00
300	1	129	0.16	1	155	0.16	1	159	0.00	1	191	0.00
600	1	64	0.16	1	77	0.16	1	79	0.00	1	95	0.00
1200	0	129	0.16	0	155	0.16	0	159	0.00	0	191	0.00
2400	0	64	0.16	0	77	0.16	0	79	0.00	0	95	0.00
4800	0	32	–1.36	0	38	0.16	0	39	0.00	0	47	0.00
9600	0	15	1.73	0	19	–2.34	0	19	0.00	0	23	0.00
19200	0	7	1.73	0	9	–2.34	0	9	0.00	0	11	0.00
31250	0	4	0.00	0	5	0.00	0	5	2.40	0	6	5.33
38400	0	3	1.73	0	4	–2.34	0	4	0.00	0	5	0.00

16.4.2 Operation in Asynchronous Mode

In asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time.

The transmitting and receiving sections of the SCIF are independent, so full duplex communication is possible. The transmitter and receiver are 16-byte FIFO buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmitting and receiving.

Figure 16.2 shows the general format of asynchronous serial communication.

In asynchronous serial communication, the communication line is normally held in the mark (high) state. The SCIF monitors the line and starts serial communication when the line goes to the space (low) state, indicating a start bit. One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in that order.

When receiving in asynchronous mode, the SCIF synchronizes at the falling edge of the start bit. The SCIF samples each data bit on the eighth pulse of a clock with a frequency 16 times the bit rate. Receive data is latched at the center of each bit.

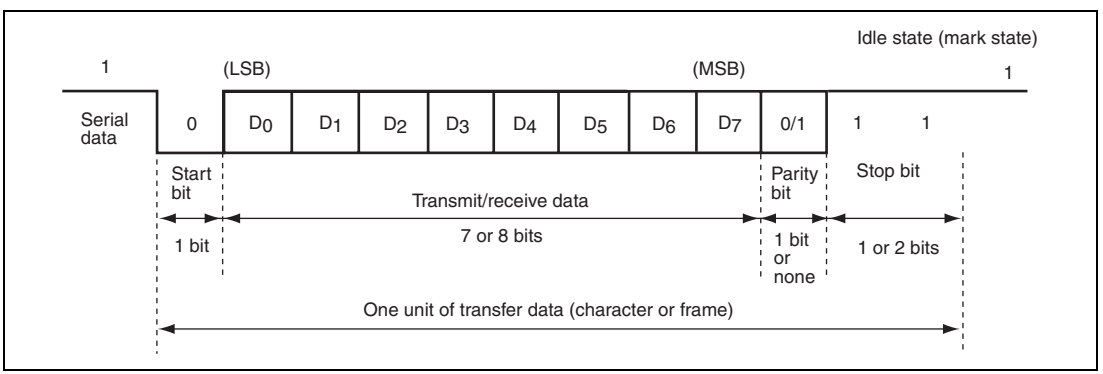


Figure 16.2 Example of Data Format in Asynchronous Communication (8-Bit Data with Parity and Two Stop Bits)

Table 17.3 Transfer Rate

Bit 3	Bit 2	Bit 1	Bit 0		Transfer Rate					
CKS3	CKS2	CKS1	CKS0	Clock	Pϕ = 16.7 MHz	Pϕ = 20.0 MHz	Pϕ = 25.0 MHz	Pϕ = 30.0 MHz	Pϕ = 33.3 MHz	Pϕ = 40 MHz
0	0	0	0	Pϕ/28	595 kHz	714 kHz	893 kHz	1071 kHz	1189 kHz	1430 kHz
			1	Pϕ/40	417 kHz	500 kHz	625 kHz	750 kHz	833 kHz	1000 kHz
		1	0	Pϕ/48	347 kHz	417 kHz	521 kHz	625 kHz	694 kHz	833 kHz
			1	Pϕ/64	260 kHz	313 kHz	391 kHz	469 kHz	520 kHz	625 kHz
	1	0	0	Pϕ/80	208 kHz	250 kHz	313 kHz	375 kHz	416 kHz	500 kHz
			1	Pϕ/100	167 kHz	200 kHz	250 kHz	300 kHz	333 kHz	400 kHz
		1	0	Pϕ/112	149 kHz	179 kHz	223 kHz	268 kHz	297 kHz	357 kHz
			1	Pϕ/128	130 kHz	156 kHz	195 kHz	234 kHz	260 kHz	313 kHz
1	0	0	0	Pϕ/112	149 kHz	179 kHz	223 kHz	268 kHz	297 kHz	357 kHz
			1	Pϕ/160	104 kHz	125 kHz	156 kHz	188 kHz	208 kHz	250 kHz
		1	0	Pϕ/192	86.8 kHz	104 kHz	130 kHz	156 kHz	173 kHz	208 kHz
			1	Pϕ/256	65.1 kHz	78.1 kHz	97.7 kHz	117 kHz	130 kHz	156 kHz
	1	0	0	Pϕ/320	52.1 kHz	62.5 kHz	78.1 kHz	93.8 kHz	104 kHz	125 kHz
			1	Pϕ/400	41.7 kHz	50.0 kHz	62.5 kHz	75.0 kHz	83.3 kHz	100 kHz
		1	0	Pϕ/448	37.2 kHz	44.6 kHz	55.8 kHz	67.0 kHz	74.3 kHz	89.3 kHz
			1	Pϕ/512	32.6 kHz	39.1 kHz	48.8 kHz	58.6 kHz	65.0 kHz	78.1 kHz

Note: The settings should satisfy external specifications.

Important: Although core of RCAN-ET is designed based on a 32-bit bus system, the whole RCAN-ET including MPI for the CPU has 16-bit bus interface to CPU. LongWord (32-bit) accesses are converted into two consecutive word accesses by the bus interface.

19.2.2 Functions of Each Block

(1) Micro Processor Interface (MPI)

The MPI allows communication between the Renesas CPU and RCAN-ET's registers/mailboxes to control the memory interface. It also contains the Wakeup Control logic that detects the CAN bus activities and notifies the MPI and the other parts of RCAN-ET so that the RCAN-ET can automatically exit the Sleep mode.

It contains registers such as MCR, IRR, GSR and IMR.

(2) Mailbox

The Mailboxes consists of RAM configured as message buffers and registers. There are 16 Mailboxes, and each mailbox has the following information.

<RAM>

- CAN message control (identifier, rtr, ide,etc)
- CAN message data (for CAN Data frames)
- Local Acceptance Filter Mask for reception

<Registers>

- CAN message control (dlc)
- 3-bit wide Mailbox Configuration, Disable Automatic Re-Transmission bit, Auto-Transmission for Remote Request bit, New Message Control bit

19.3.2 Message Control Field

STDID[10:0]: These bits set the identifier (standard identifier) of data frames and remote frames.

EXTID[17:0]: These bits set the identifier (extended identifier) of data frames and remote frames.

RTR (Remote Transmission Request bit): Used to distinguish between data frames and remote frames. This bit is overwritten by received CAN Frames depending on Data Frames or Remote Frames.

Important: Please note that, when ATX bit is set with the setting MBC = B'001, the RTR bit will never be set. When a Remote Frame is received, the CPU can be notified by the corresponding RFPR set or IRR[2] (Remote Frame Request Interrupt), however, as RCAN-ET needs to transmit the current message as a Data Frame, the RTR bit remains unchanged. In case of overrun condition, the message received is discarded. Consequently, when a remote frame is causing overrun (UMSR is set) into a Mailbox configured with ATX = 1/NMC = 0, the transmission of the corresponding data frame is not carried out.

Important: In order to support automatic answer to remote frame when MBC = B'001 is used and ATX = 1 the RTR flag must be programmed to zero to allow data frame to be transmitted.

Note: when a Mailbox is configured to send a remote frame request the DLC used for transmission is the one stored into the Mailbox.

RTR	Description
0	Data frame
1	Remote frame

IDE (Identifier Extension bit): Used to distinguish between the standard format and extended format of CAN data frames and remote frames.

IDE	Description
0	Standard format
1	Extended format

19.8 CAN Bus Interface

A bus transceiver IC is necessary to connect this LSI to a CAN bus. A Renesas HA13721 transceiver IC and its compatible products are recommended. As the CRx and CTx pins use 3 V, an external level shifter is necessary. Figure 19.13 shows a sample connection diagram.

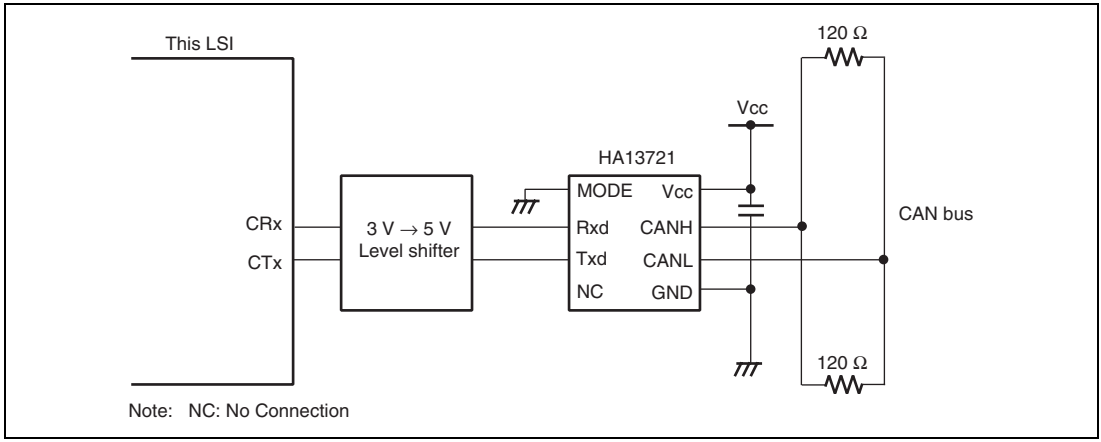


Figure 19.13 High-Speed Interface Using HA13721

(7) Parity bit

The parity bit is used to confirm that transfer data occurs with no errors.

The parity bit is added to respective data of the master address, slave address, control, message length, and data bits.

Even parity is used. When the number of bits having the value 1 is odd, the parity bit is 1. When the number of bits having the value 1 is even, the parity bit is 0.

(8) Acknowledge bit

In normal communications (single unit to single unit communications), the acknowledge bit is added in the following positions to confirm that data is correctly accepted.

- At the end of the slave address field
- At the end of the control field
- At the end of the message length field
- At the end of the data field

The acknowledge bit is defined below.

- 0: indicates that the transfer data is acknowledged. (ACK)
- 1: indicates that the transfer data is not acknowledged. (NAK)

Note that the acknowledge bit is ignored in the case of broadcast communications.

(a) Acknowledge bit at the End of the Slave Address Field

The acknowledge bit at the end of the slave address field becomes NAK in the following cases and transfer is stopped.

- When the parity of the master address or slave address bits is incorrect
- When a timing error (an error in bit format) occurs
- When there is no slave unit

Register Abbreviation	Bits 31/ 23/15/7	Bits30/ 22/14/6	Bits 29/ 21/13/5	Bits28/ 20/12/4	Bits 27/ 19/11/3	Bits26/ 18/10/2	Bits 25/ 17/9/1	Bits24/ 16/8/0	Module
SSITDR_0									SSI
SSIRDR_0									
SSICR_1	—	—	—	DMEN	UIEN	OIEN	IIEN	DIEN	
	CHNL1	CHNL0	DWL2	DWL1	DWL0	SWL2	SWL1	SWL0	
	SCKD	SWSD	SCKP	SWSP	SPDP	SDTA	PDTA	DEL	
	—	CKDV2	CKDV1	CKDV0	MUEN	—	TRMD	EN	
SSISR_1	—	—	—	DMRQ	UIRQ	OIEN	IIRQ	DIRQ	
	—	—	—	—	—	—	—	—	
	—	—	—	—	—	—	—	—	
	—	—	—	—	CHNO1	CHNO0	SWNO	IDST	
SSITDR_1									
SSIRDR_1									
ICCR1_0	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0	IIC3
ICCR2_0	BBSY	SCP	SDAO	SDAOP	SCL	—	IICRST	—	
ICMR_0	MLS	WAIT	—	—	BCWP	BS2	BC1	BC0	
ICIER_0	TIE	TEIE	RIE	NAKIE	STIE	ACKE	ACKBR	ACKBT	
ICSR_0	TDRE	TEND	RDRF	NACKF	STOP	AL_OVE	AAS	ADZ	
SAR_0	SVA6	SVA5	SVA4	SVA3	SVA2	SVA1	SVA0	FS	
ICDRT_0									
ICDRR_0									
NF2CYC_0	—	—	—	—	—	—	—	NF2CYC	
ICCR1_1	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0	
ICCR2_1	BBSY	SCP	SDAO	SDAOP	SCL	—	IICRST	—	

Register Abbreviation	Bits 31/ 23/15/7	Bits30/ 22/14/6	Bits 29/ 21/13/5	Bits28/ 20/12/4	Bits 27/ 19/11/3	Bits26/ 18/10/2	Bits 25/ 17/9/1	Bits24/ 16/8/0	Module
MB[1 to 15]. MSG_DATA[5]					MSG_DATA_5				RCAN-ET
MB[1 to 15]. MSG_DATA[6]					MSG_DATA_6				
MB[1 to 15]. MSG_DATA[7]					MSG_DATA_7				
MB[1 to 15]. CONTROL1H	—	—	NMC	ATX	DART	MBC2	MBC1	MBC0	
MB[1 to 15]. CONTROL1L	—	—	—	—	DLC3	DLC2	DLC1	DLC0	
MCR_1	MCR15	MCR14	—	—	—	TST2	TST1	TST0	
	MCR7	MCR6	MCR5	—	—	MCR2	MCR1	MCR0	
GSR_1	—	—	—	—	—	—	—	—	
	—	—	GSR5	GSR4	GSR3	GSR2	GSR1	GSR0	
BCR1_1	TSG1_3	TSG1_2	TSG1_1	TSG1_0	—	TSG2_2	TSG2_1	TSG2_0	
	—	—	SJW1	SJW0	—	—	—	BSP	
BCR0_1	—	—	—	—	—	—	—	—	
	BRP7	BRP6	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	
IRR_1	—	—	IRR13	IRR12	—	—	IRR9	IRR8	
	IRR7	IRR6	IRR5	IRR4	IRR3	IRR2	IRR1	IRR0	
IMR_1	IMR15	IMR14	IMR13	IMR12	IMR11	IMR10	IMR9	IMR8	
	IMR7	IMR6	IMR5	IMR4	IMR3	IMR2	IMR1	IMR0	
TEC_1/REC_1	TEC7	TEC6	TEC5	TEC4	TEC3	TEC2	TEC1	TEC0	
	REC7	REC6	REC5	REC4	REC3	REC2	REC1	REC0	
TXPR1_1	TXPR1_15	TXPR1_14	TXPR1_13	TXPR1_12	TXPR1_11	TXPR1_10	TXPR1_9	TXPR1_8	
	TXPR1_7	TXPR1_6	TXPR1_5	TXPR1_4	TXPR1_3	TXPR1_2	TXPR1_1	TXPR1_0	
TXPR0_1	TXPR0_15	TXPR0_14	TXPR0_13	TXPR0_12	TXPR0_11	TXPR0_10	TXPR0_9	TXPR0_8	
	TXPR0_7	TXPR0_6	TXPR0_5	TXPR0_4	TXPR0_3	TXPR0_2	TXPR0_1	—	
TXCR0_1	TXCR0_15	TXCR0_14	TXCR0_13	TXCR0_12	TXCR0_11	TXCR0_10	TXCR0_9	TXCR0_8	
	TXCR0_7	TXCR0_6	TXCR0_5	TXCR0_4	TXCR0_3	TXCR0_2	TXCR0_1	—	
TXACK0_1	TXACK0_15	TXACK0_14	TXACK0_13	TXACK0_12	TXACK0_11	TXACK0_10	TXACK0_9	TXACK0_8	
	TXACK0_7	TXACK0_6	TXACK0_5	TXACK0_4	TXACK0_3	TXACK0_2	TXACK0_1	—	
ABACK0_1	ABACK0_15	ABACK0_14	ABACK0_13	ABACK0_12	ABACK0_11	ABACK0_10	ABACK0_9	ABACK0_8	
	ABACK0_7	ABACK0_6	ABACK0_5	ABACK0_4	ABACK0_3	ABACK0_2	ABACK0_1	—	
RXPR0_1	RXPR0_15	RXPR0_14	RXPR0_13	RXPR0_12	RXPR0_11	RXPR0_10	RXPR0_9	RXPR0_8	
	RXPR0_7	RXPR0_6	RXPR0_5	RXPR0_4	RXPR0_3	RXPR0_2	RXPR0_1	RXPR0_0	
RFPR0_1	RFPR0_15	RFPR0_14	RFPR0_13	RFPR0_12	RFPR0_11	RFPR0_10	RFPR0_9	RFPR0_8	
	RFPR0_7	RFPR0_6	RFPR0_5	RFPR0_4	RFPR0_3	RFPR0_2	RFPR0_1	RFPR0_0	

Section 31 Electrical Characteristics

31.1 Absolute Maximum Ratings

Table 31.1 lists the absolute maximum ratings.

Table 31.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage (I/O)		PV_{CC}	–0.3 to 4.6	V
Power supply voltage (Internal)		$V_{CC}R$		
Power supply voltage (PLL)		$PLLV_{CC}$		
Analog power supply voltage		AV_{CC}	–0.3 to 4.6	V
Analog reference voltage		AV_{ref}	–0.3 to AV_{CC} +0.3	V
Input voltage	Analog input pin	V_{AN}	–0.3 to AV_{CC} +0.3	V
	PC22 to PC25, PD15, PD16	V_{in}	–0.3 to 5.5	V
	Other pins	V_{in}	–0.3 to PV_{CC} +0.3	V
Operating temperature		T_{opr}	–20 to +70 (Regular specifications)	°C
			–40 to +85 (Wide-range specifications)	
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

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