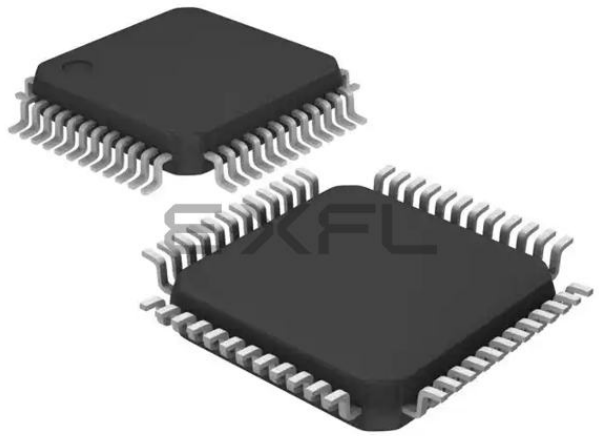
Renesas Electronics America Inc - UPD78F0401GA-GAM-AX Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	30
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0401ga-gam-ax

[MEMO]

(3/3)

Item \ Part Number			78K0/LF3													
			μPD78F047x					μPD78F048x					μPD78F049x				
			80 Pins													
Flash memory (KB)			16	24	32	48	60	16	24	32	48	60	16	24	32	48	60
RAM (KB)			0.75	1	1	2	2	0.75	1	1	2	2	0.75	1	1	2	2
Power supply voltage			V_{DD} = 1.8 to 5.5 V														
Regulator			Provided														
Minimum instruction execution time			0.2 μs (10 MHz: V_{DD} = 2.7 to 5.5 V)/ 0.4 μs (5 MHz: V_{DD} = 1.8 to 5.5 V)														
Clock	Main	High-speed system clock	10 MHz: V_{DD} = 2.7 to 5.5 V/5 MHz: V_{DD} = 1.8 to 5.5 V														
		Internal high-speed oscillation clock	8 MHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Subclock		32.768 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
	Internal low-speed oscillation clock		240 kHz (TYP.): V_{DD} = 1.8 to 5.5 V														
Port	Total		62														
Timer	16 bits (TM0)		1 ch														
	8 bits (TM5)		3 ch														
	8 bits (TMH)		3 ch														
	RTC		1 ch														
	WDT		1 ch														
Serial interface	3-wire CSI/UART[Note1]		1 ch														
	Automatic transmit/ receive 3-wire CSI		1 ch														
	UART supporting LIN-bus[Note2]		1 ch														
LCD	Type		External resistance division and internal resistance division are switchable.														
	Segment signal		40 (36)[Note3]										32 (28)[Note3]				
	Common signal		4 (8)[Note3]														
10-bit successive approximation type A/D			–					8 ch									
16-bit ΔΣ type A/D			–										3 ch				
Interrupt	External		7														
	Internal		20					21					22				
Key interrupt			8 ch														
Reset	$\overline{\text{RESET}}$ pin		Provided														
	POC		1.59 V ±0.15 V (Time for rising up to 1.8 V : 3.6 ms (MAX.))														
	LVI		The detection level of the supply voltage is selectable in 16 steps.														
	WDT		Provided														
Clock output/ Buzzer output			Provided														
Remote controller receiver			Provided														
MCG			Provided														
On-chip debug function			Provided														
Operating ambient temperature			T_A = –40 to +85°C														

Notes 1. Select either of the functions of these alternate-function pins.

2. The LIN-bus supporting UART pins can be changed to the Automatic transmit/receive 3-wire CSI/UART pins (pin numbers 75 and 76).

3. The values in parentheses are the number of signal outputs when 8com is used.

Table 3-6. Special Function Register List (1/4)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulatable Bit Unit			After Reset
				1 Bit	8 Bits	16 Bits	
FF00H	Receive buffer register 6	RXB6	R	–	√	–	FFH
FF01H	Port register 1	P1	R/W	√	√	–	00H
FF02H	Port register 2	P2	R/W	√	√	–	00H
FF03H	Port register 3	P3	R/W	√	√	–	00H
FF04H	Port register 4	P4	R/W	√	√	–	00H
FF05H	Transmit buffer register 6	TXB6	R/W	–	√	–	FFH
FF06H	A/D conversion result register[Note]	ADCR	R	–	–	√	0000H
FF07H	A/D conversion result register (H) [Note]	ADCRH	R	–	√	–	00H
FF0AH	Port register 10	P10	R/W	√	√	–	00H
FF0BH	Port register 11	P11	R/W	√	√	–	00H
FF0CH	Port register 12	P12	R/W	√	√	–	00H
FF0EH	Port register 14	P14	R/W	√	√	–	00H
FF0FH	Port register 15	P15	R/W	√	√	–	00H
FF10H	16-bit timer counter 00	TM00	R	–	–	√	0000H
FF11H							
FF12H	16-bit timer capture/compare register 000	CR000	R/W	–	–	√	0000H
FF13H							
FF14H	16-bit timer capture/compare register 010	CR010	R/W	–	–	√	0000H
FF15H							
FF16H	8-bit timer counter 50	TM50	R	–	√	–	00H
FF17H	8-bit timer compare register 50	CR50	R/W	–	√	–	00H
FF18H	8-bit timer H compare register 00	CMP00	R/W	–	√	–	00H
FF19H	8-bit timer H compare register 10	CMP10	R/W	–	√	–	00H
FF1AH	8-bit timer H compare register 01	CMP01	R/W	–	√	–	00H
FF1BH	8-bit timer H compare register 11	CMP11	R/W	–	√	–	00H
FF20H	Port function register 1	PF1	R/W	√	√	–	00H
FF21H	Port mode register 1	PM1	R/W	√	√	–	FFH
FF22H	Port mode register 2	PM2	R/W	√	√	–	FFH
FF23H	Port mode register 3	PM3	R/W	√	√	–	FFH
FF24H	Port mode register 4	PM4	R/W	√	√	–	FFH
FF2AH	Port mode register 10	PM10	R/W	√	√	–	FFH
FF2BH	Port mode register 11	PM11	R/W	√	√	–	FFH
FF2CH	Port mode register 12	PM12	R/W	√	√	–	FFH
FF2EH	Port mode register 14	PM14	R/W	√	√	–	FFH
FF2FH	Port mode register 15	PM15	R/W	√	√	–	FFH
FF30H	Internal high-speed oscillation trimming register	HIOTRM	R/W	–	√	–	10H
FF31H	Pull-up resistor option register 1	PU1	R/W	√	√	–	00H
FF33H	Pull-up resistor option register 3	PU3	R/W	√	√	–	00H
FF34H	Pull-up resistor option register 4	PU4	R/W	√	√	–	00H
FF3AH	Pull-up resistor option register 10	PU10	R/W	√	√	–	00H
FF3BH	Pull-up resistor option register 11	PU11	R/W	√	√	–	00H

Note μPD78F041x only.

4.2.6 Port 11

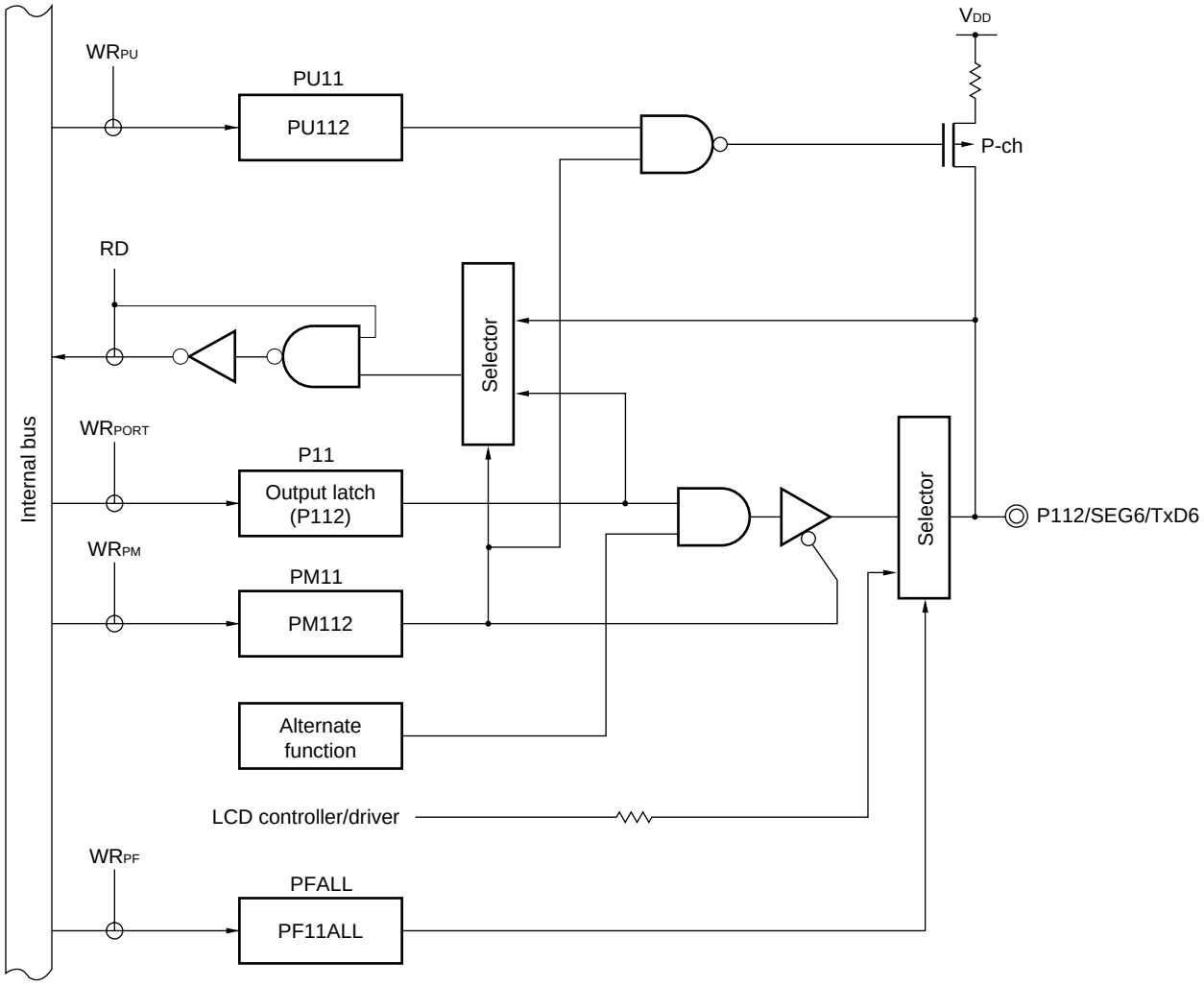
Port 11 is a 2-bit I/O port with an output latch. Port 11 can be set to the input mode or output mode in 1-bit units using port mode register 11 (PM11). When the P112, P113 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 11 (PU11).

This port can also be used for segment output and serial interface data I/O.

Reset signal generation sets port 11 to input mode.

Figures 4-9 and 4-10 show a block diagram of port 11.

Figure 4-9. Block Diagram of P112



P11: Port register 11
PU11: Pull-up resistor option register 11
PM11: Port mode register 11
PFALL: Port function register ALL
RD: Read signal
WR××: Write signal

(3) Internal low-speed oscillation clock (clock for watchdog timer)

- **Internal low-speed oscillator**

  This circuit oscillates a clock of f_{RL} = 240 kHz (TYP.). After a reset release, the internal low-speed oscillation clock always starts operating.

  Oscillation can be stopped by using the internal oscillation mode register (RCM) when "internal low-speed oscillator can be stopped by software" is set by option byte.

  The internal low-speed oscillation clock cannot be used as the CPU clock. The following hardware operates with the internal low-speed oscillation clock.

  - Watchdog timer
  - 8-bit timer H1 (if f_{RL}, $f_{RL}/2^7$ or $f_{RL}/2^9$ is selected as the count clock)
  - LCD controller/driver (if $f_{RL}/2^3$ is selected as the LCD source clock)

Remark f_{RL}: Internal low-speed oscillation clock frequency

5.2 Configuration of Clock Generator

The clock generator includes the following hardware.

Table 5-1. Configuration of Clock Generator

Item	Configuration
Control registers	Clock operation mode select register (OSCCTL) Processor clock control register (PCC) Internal oscillation mode register (RCM) Main OSC control register (MOC) Main clock mode register (MCM) Oscillation stabilization time counter status register (OSTC) Oscillation stabilization time select register (OSTS) Internal high-speed oscillation trimming register (HIOTRM)
Oscillators	X1 oscillator XT1 oscillator Internal high-speed oscillator Internal low-speed oscillator

(4) Internal oscillation mode register (RCM)

This register sets the operation mode of internal oscillator.

RCM can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 80H[Note 1].

Figure 5-4. Format of Internal Oscillation Mode Register (RCM)

Address: FFA0H After reset: 80H[Note 1] R/W[Note 2]

Symbol	<7>	6	5	4	3	2	<1>	<0>
RCM	RSTS	0	0	0	0	0	LSRSTOP	RSTOP

RSTS	Status of internal high-speed oscillator
0	Waiting for accuracy stabilization of internal high-speed oscillator
1	Stability operating of internal high-speed oscillator

LSRSTOP	Internal low-speed oscillator oscillating/stopped
0	Internal low-speed oscillator oscillating
1	Internal low-speed oscillator stopped

RSTOP	Internal high-speed oscillator oscillating/stopped
0	Internal high-speed oscillator oscillating
1	Internal high-speed oscillator stopped

Notes 1. The value of this register is 00H immediately after a reset release but automatically changes to 80H after internal high-speed oscillator has been stabilized.

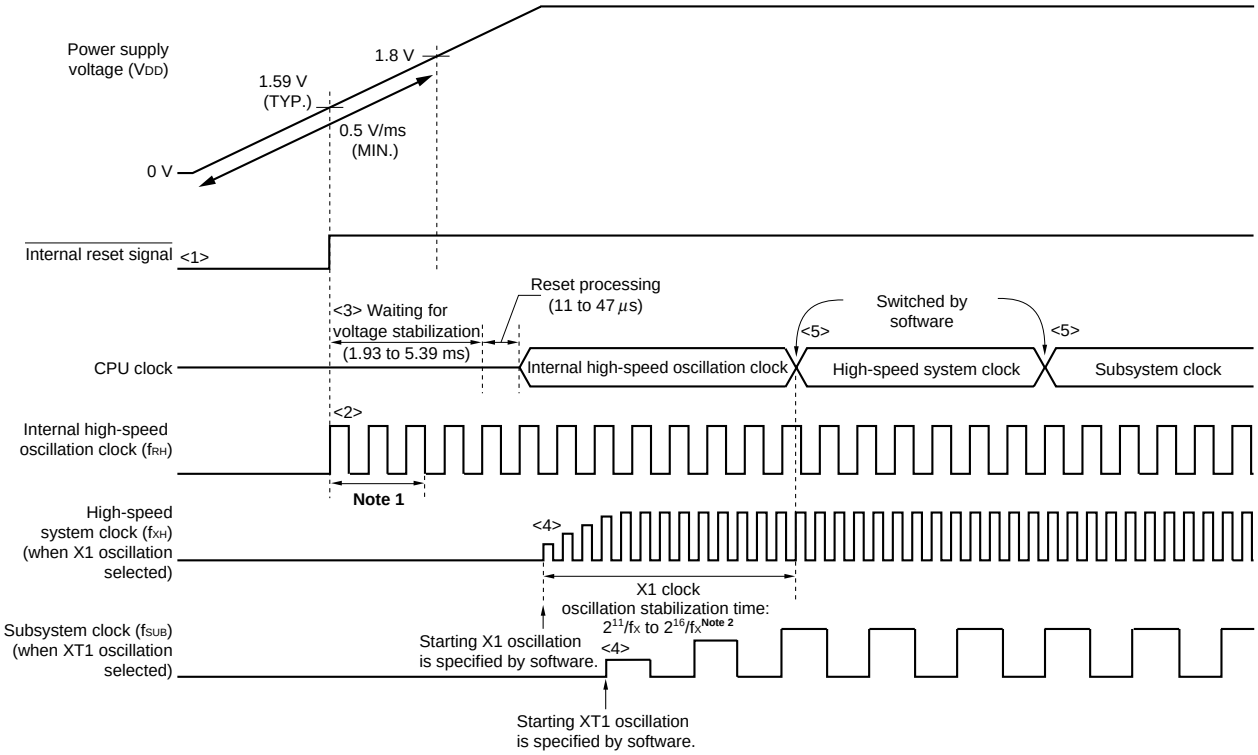
2. Bit 7 is read-only.

Caution When setting RSTOP to 1, be sure to confirm that the CPU operates with a clock other than the internal high-speed oscillation clock. Specifically, set under either of the following conditions.

- **When MCS = 1 (when CPU operates with the high-speed system clock)**
- **When CLS = 1 (when CPU operates with the subsystem clock)**

In addition, stop peripheral hardware that is operating on the internal high-speed oscillation clock before setting RSTOP to 1.

Figure 5-13. Clock Generator Operation When Power Supply Voltage Is Turned On (When 1.59 V POC Mode Is Set (Option Byte: POCMODE = 0))



<1> When the power is turned on, an internal reset signal is generated by the power-on-clear (POC) circuit.

<2> When the power supply voltage exceeds 1.59 V (TYP.), the reset is released and the internal high-speed oscillator automatically starts oscillation.

<3> When the power supply voltage rises with a slope of 0.5 V/ms (MIN.), the CPU starts operation on the internal high-speed oscillation clock after the reset is released and after the stabilization times for the voltage of the power supply and regulator have elapsed, and then reset processing is performed.

<4> Set the start of oscillation of the X1 or XT1 clock via software (see **(1)** in **5.6.1 Example of controlling high-speed system clock** and **(1)** in **5.6.3 Example of controlling subsystem clock)**.

<5> When switching the CPU clock to the X1 or XT1 clock, wait for the clock oscillation to stabilize, and then set switching via software (see **(3)** in **5.6.1 Example of controlling high-speed system clock** and **(3)** in **5.6.3 Example of controlling subsystem clock**).

Notes 1. The internal voltage stabilization time includes the oscillation accuracy stabilization time of the internal high-speed oscillation clock.

2. When releasing a reset (above figure) or releasing STOP mode while the CPU is operating on the internal high-speed oscillation clock, confirm the oscillation stabilization time for the X1 clock using the oscillation stabilization time counter status register (OSTC). If the CPU operates on the high-speed system clock (X1 oscillation), set the oscillation stabilization time when releasing STOP mode using the oscillation stabilization time select register (OSTS).

Cautions 1. If the voltage rises with a slope of less than 0.5 V/ms (MIN.) from power application until the voltage reaches 1.8 V, input a low level to the $\overline{\text{RESET}}$ pin from power application until the voltage reaches 1.8 V, or set the 2.7 V/1.59 V POC mode by using the option byte (POCMODE = 1) (see Figure 5-14). By doing so, the CPU operates with the same timing as <2> and thereafter in Figure 5-13 after reset release by the $\overline{\text{RESET}}$ pin.

2. It is not necessary to wait for the oscillation stabilization time when an external clock input from the EXCLK pin is used.

5.6.7 Condition before changing CPU clock and processing after changing CPU clock

Condition before changing the CPU clock and processing after changing the CPU clock are shown below.

Table 5-6. Changing CPU Clock

CPU Clock		Condition Before Change	Processing After Change
Before Change	After Change		
Internal high-speed oscillation clock	X1 clock	Stabilization of X1 oscillation • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time	• Internal high-speed oscillator can be stopped (RSTOP = 1).
	External main system clock	Enabling input of external clock from EXCLK pin • MSTOP = 0, OSCSEL = 1, EXCLK = 1	
X1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator • RSTOP = 0	X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).
Internal high-speed oscillation clock	XT1 clock	Stabilization of XT1 oscillation • OSCSELS = 1 • After elapse of oscillation stabilization time	Operating current can be reduced by stopping internal high-speed oscillator (RSTOP = 1).
X1 clock			X1 oscillation can be stopped (MSTOP = 1).
External main system clock			External main system clock input can be disabled (MSTOP = 1).
XT1 clock	Internal high-speed oscillation clock	Oscillation of internal high-speed oscillator and selection of internal high-speed oscillation clock as main system clock • RSTOP = 0, MCS = 0	XT1 oscillation can be stopped (OSCSELS = 0).
	X1 clock	Stabilization of X1 oscillation and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 0 • After elapse of oscillation stabilization time • MCS = 1	
	External main system clock	Enabling input of external clock from EXCLK pin and selection of high-speed system clock as main system clock • MSTOP = 0, OSCSEL = 1, EXCLK = 1 • MCS = 1	

(2) Capture/compare control register 00 (CRC00)

CRC00 is the register that controls the operation of CR000 and CR010.

Changing the value of CRC00 is prohibited during operation (when TMC003 and TMC002 = other than 00).

CRC00 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CRC00 to 00H.

Figure 6-6. Format of Capture/Compare Control Register 00 (CRC00)

Address: FFBCH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CRC00	0	0	0	0	0	CRC002	CRC001	CRC000

CRC002	CR010 operating mode selection
0	Operates as compare register
1	Operates as capture register

CRC001	CR000 capture trigger selection
0	Captures on valid edge of TI010 pin
1	Captures on valid edge of TI000 pin by reverse phase[Note]
The valid edge of the TI010 and TI000 pin is set by PRM00. If ES001 and ES000 are set to 11 (both edges) when CRC001 is 1, the valid edge of the TI000 pin cannot be detected.	

CRC000	CR000 operating mode selection
0	Operates as compare register
1	Operates as capture register
If TMC003 and TMC002 are set to 11 (clear & start mode entered upon a match between TM00 and CR000), be sure to set CRC000 to 0.	

Note When the valid edge is detected from the TI010 pin, the capture operation is not performed but the INTTM000 signal is generated as an external interrupt signal.

Caution To ensure that the capture operation is performed properly, the capture trigger requires a pulse two cycles longer than the count clock selected by prescaler mode register 00 (PRM00).

<4> When the 8-bit timer counter Hn and the CMP1n register match, an inactive level is output and the compare register to be compared with 8-bit timer counter Hn is changed from the CMP1n register to the CMP0n register. At this time, 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<5> By performing procedures <3> and <4> repeatedly, a pulse with an arbitrary duty can be obtained.

<6> To stop the count operation, set TMHEn = 0.

If the setting value of the CMP0n register is N, the setting value of the CMP1n register is M, and the count clock frequency is f_{CNT}, the PWM pulse output cycle and duty are as follows.

- PWM pulse output cycle = (N + 1)/f_{CNT}
- Duty = (M + 1)/(N + 1)

Cautions 1. The set value of the CMP1n register can be changed while the timer counter is operating. However, this takes a duration of three operating clocks (signal selected by the CKSn2 to CKSn0 bits of the TMHMDn register) from when the value of the CMP1n register is changed until the value is transferred to the register.

2. Be sure to set the CMP1n register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMP1n register).

3. Make sure that the CMP1n register setting value (M) and CMP0n register setting value (N) are within the following range.

00H ≤ CMP1n (M) < CMP0n (N) ≤ FFH

Remarks 1. For the setting of the output pin, see **8.3 (3) Port mode register 3 (PM3)**.

2. For details on how to enable the INTTMHn signal interrupt, see **CHAPTER 17 INTERRUPT FUNCTIONS**.

3. n = 0 to 2, however, TOH0 and TOH1 only for TOHn

Figure 12-9. Format of A/D Port Configuration Register 0 (ADPC0)

Address: FF8FH After reset: 08H R/W

Symbol	7	6	5	4	3	2	1	0
ADPC0	0	0	0	0	0	ADPC02	ADPC01	ADPC00

ADPC02	ADPC01	ADPC00	Digital I/O (D)/analog input (A) switching					
			P25 /ANI5	P24 /ANI4	P23 /ANI3	P22 /AN2	P21 /ANI1	P20 /ANI0
0	0	0	A	A	A	A	A	A
0	0	1	A	A	A	A	A	D
0	1	0	A	A	A	A	D	D
0	1	1	A	A	A	D	D	D
1	0	0	A	A	D	D	D	D
1	0	1	A	D	D	D	D	D
1	1	0	D	D	D	D	D	D
Other than above			Setting prohibited					

Cautions 1. Set the channel used for A/D conversion to the input mode by using port mode register 2 (PM2).

2. Do not set the pin set by ADPC0 as digital I/O by ADS, ADDS1, or ADDS0.

3. If data is written to ADPC0, a wait cycle is generated. Do not write data to ADPC0 when the CPU is operating on the subsystem clock and the peripheral hardware clock is stopped. For details, see CHAPTER 29 CAUTIONS FOR WAIT.

4. If pins ANI0/P20/SEG21 to ANI5/P25/SEG16 are set to segment output via the PF2 register, output is set to segment output, regardless of the ADPC0 setting.

(2) Asynchronous serial interface reception error status register 6 (ASIS6)

This register indicates an error status on completion of reception by serial interface UART6. It includes three error flag bits (PE6, FE6, OVE6).

This register is read-only by an 8-bit memory manipulation instruction.

Reset signal generation, or clearing bit 7 (POWER6) or bit 5 (RXE6) of ASIM6 to 0 clears this register to 00H. 00H is read when this register is read. If a reception error occurs, read ASIS6 and then read receive buffer register 6 (RXB6) to clear the error flag.

Figure 14-6. Format of Asynchronous Serial Interface Reception Error Status Register 6 (ASIS6)

Address: FF53H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ASIS6	0	0	0	0	0	PE6	FE6	OVE6

PE6	Status flag indicating parity error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If the parity of transmit data does not match the parity bit on completion of reception

FE6	Status flag indicating framing error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If the stop bit is not detected on completion of reception

OVE6	Status flag indicating overrun error
0	If POWER6 = 0 or RXE6 = 0, or if ASIS6 register is read
1	If receive data is set to the RXB6 register and the next reception operation is completed before the data is read.

Cautions 1. The operation of the PE6 bit differs depending on the set values of the PS61 and PS60 bits of asynchronous serial interface operation mode register 6 (ASIM6).

2. For the stop bit of the receive data, only the first stop bit is checked regardless of the number of stop bits.

3. If an overrun error occurs, the next receive data is not written to receive buffer register 6 (RXB6) but discarded.

4. If data is read from ASIS6, a wait cycle is generated. Do not read data from ASIS6 when the CPU is operating on the subsystem clock and the peripheral hardware clock is stopped. For details, see CHAPTER 29 CAUTIONS FOR WAIT.

14.4.3 Dedicated baud rate generator

The dedicated baud rate generator consists of a source clock selector and an 8-bit programmable counter, and generates a serial clock for transmission/reception of UART6.

Separate 8-bit counters are provided for transmission and reception.

(1) Configuration of baud rate generator

- Base clock

  The clock selected by bits 3 to 0 (TPS63 to TPS60) of clock selection register 6 (CKSR6) is supplied to each module when bit 7 (POWER6) of asynchronous serial interface operation mode register 6 (ASIM6) is 1. This clock is called the base clock and its frequency is called f_{XCLK6}. The base clock is fixed to low level when POWER6 = 0.

- Transmission counter

  This counter stops operation, cleared to 0, when bit 7 (POWER6) or bit 6 (TXE6) of asynchronous serial interface operation mode register 6 (ASIM6) is 0.

  It starts counting when POWER6 = 1 and TXE6 = 1.

  The counter is cleared to 0 when the first data transmitted is written to transmit buffer register 6 (TXB6).

  If data are continuously transmitted, the counter is cleared to 0 again when one frame of data has been completely transmitted. If there is no data to be transmitted next, the counter is not cleared to 0 and continues counting until POWER6 or TXE6 is cleared to 0.

- Reception counter

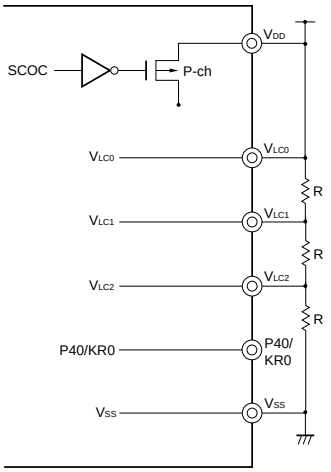
  This counter stops operation, cleared to 0, when bit 7 (POWER6) or bit 5 (RXE6) of asynchronous serial interface operation mode register 6 (ASIM6) is 0.

  It starts counting when the start bit has been detected.

  The counter stops operation after one frame has been received, until the next start bit is detected.

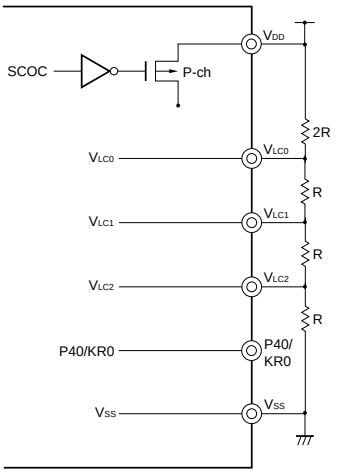
Figure 15-24. Examples of LCD Drive Power Connections (External Resistance Division Method) (2/2)

(e) 1/3 bias method
(MDSET1, MDSET0 = 0, 0)
(example of V_{DD} = 5 V, V_{LC0} = 5 V)



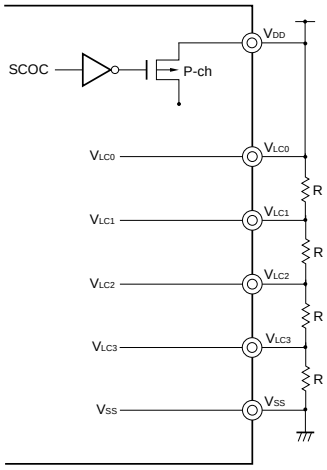
$V_{LC0} = V_{DD}$

(f) 1/3 bias method
(MDSET1, MDSET0 = 0, 0)
(example of V_{DD} = 5 V, V_{LC0} = 3 V)



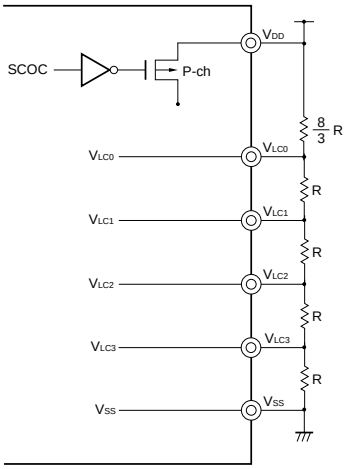
$V_{LC0} = \frac{3}{5} V_{DD}$

(g) 1/4 bias method
(MDSET1, MDSET0 = 0, 0)
(example of V_{DD} = 5 V, V_{LC0} = 5 V)



$V_{LC0} = V_{DD}$

(h) 1/4 bias method
(MDSET1, MDSET0 = 0, 0)
(example of V_{DD} = 5 V, V_{LC0} = 3 V)



$V_{LC0} = \frac{3}{5} V_{DD}$

Figure 16-8. Timing of Manchester Code Generator Mode (LSB First) (2/4)

(2) Transmit timing (MC0OLV = 0, total transmit bit length = 8 bits)

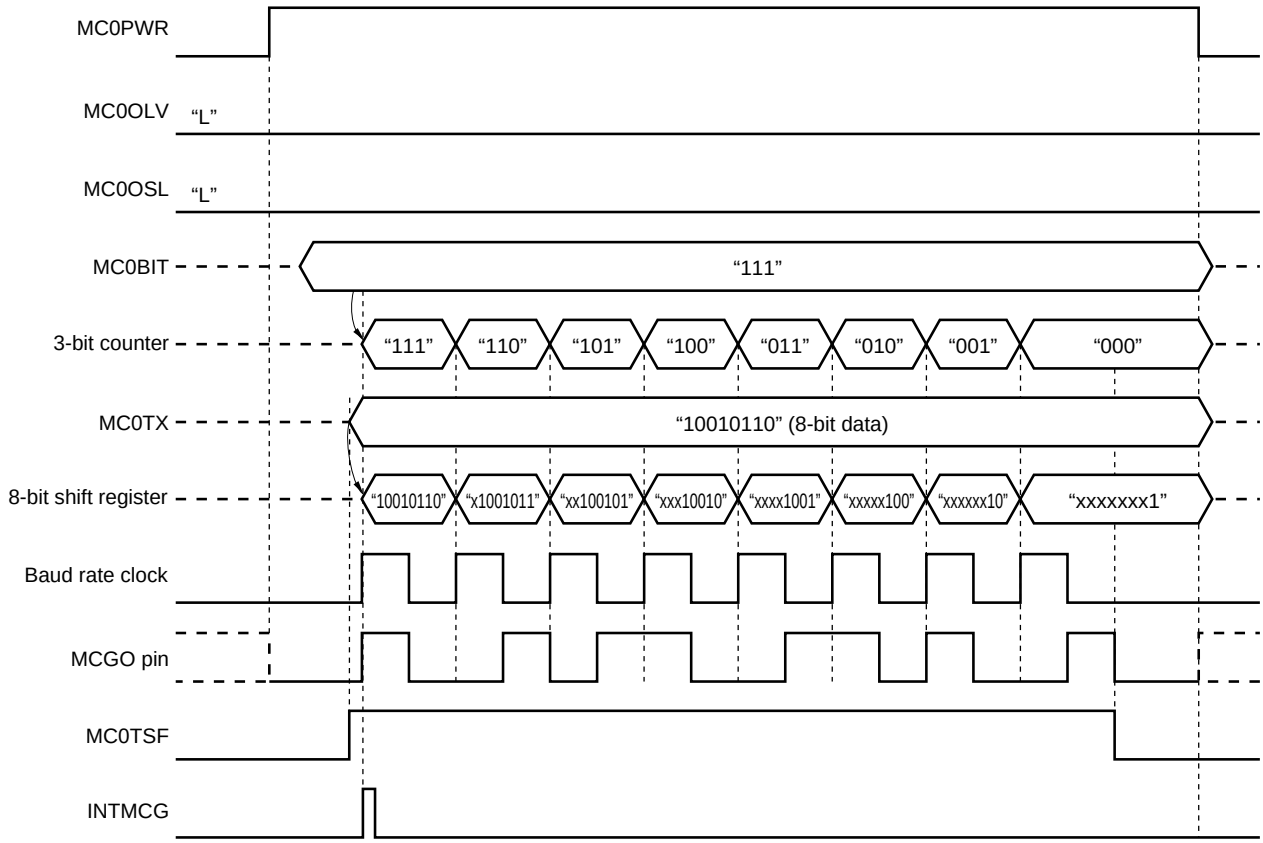


Figure 20-2. Timing of Reset by $\overline{\text{RESET}}$ Input

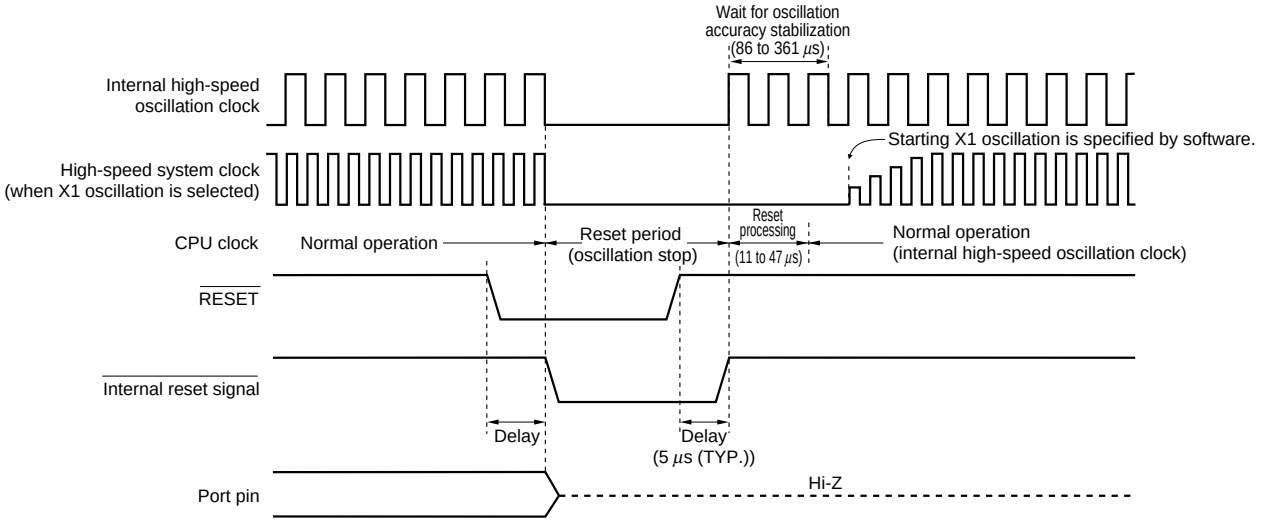
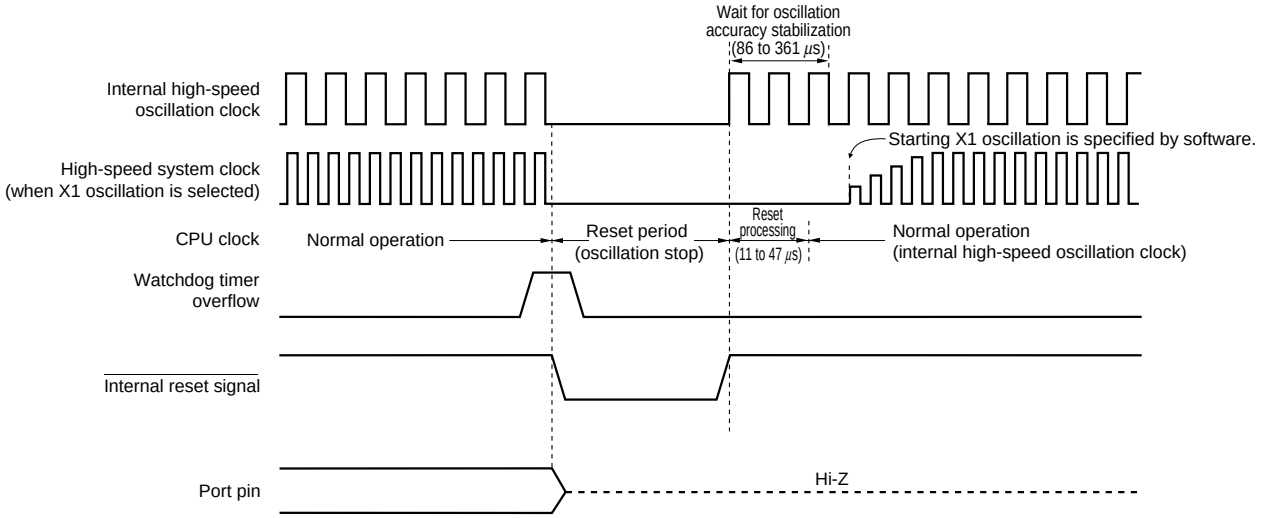


Figure 20-3. Timing of Reset Due to Watchdog Timer Overflow



Caution A watchdog timer internal reset resets the watchdog timer.

Instruction Group	Mnemonic	Operands	Bytes	Clocks		Operation	Flag
				Note 1	Note 2		Z AC CY
Call/return	**CALL**	!addr16	3	7	–	(SP – 1) ← (PC + 3)H, (SP – 2) ← (PC + 3)L, PC ← addr16, SP ← SP – 2	
	CALLF	!addr11	2	5	–	(SP – 1) ← (PC + 2)H, (SP – 2) ← (PC + 2)L, PC15 – 11 ← 00001, PC10 – 0 ← addr11, SP ← SP – 2	
	CALLT	[addr5]	1	6	–	(SP – 1) ← (PC + 1)H, (SP – 2) ← (PC + 1)L, PCH ← (00000000, addr5 + 1), PCL ← (00000000, addr5), SP ← SP – 2	
	BRK		1	6	–	(SP – 1) ← PSW, (SP – 2) ← (PC + 1)H, (SP – 3) ← (PC + 1)L, PCH ← (003FH), PCL ← (003EH), SP ← SP – 3, IE ← 0	
	RET		1	6	–	PCH ← (SP + 1), PCL ← (SP), SP ← SP + 2	
	RETI		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
	RETB		1	6	–	PCH ← (SP + 1), PCL ← (SP), PSW ← (SP + 2), SP ← SP + 3	R R R
Stack manipulate	**PUSH**	PSW	1	2	–	(SP – 1) ← PSW, SP ← SP – 1	
		rp	1	4	–	(SP – 1) ← rpH, (SP – 2) ← rpL, SP ← SP – 2	
	POP	PSW	1	2	–	PSW ← (SP), SP ← SP + 1	R R R
		rp	1	4	–	rpH ← (SP + 1), rpL ← (SP), SP ← SP + 2	
	MOVW	SP, #word	4	–	10	SP ← word	
		SP, AX	2	–	8	SP ← AX	
		AX, SP	2	–	8	AX ← SP	
Unconditional branch	**BR**	!addr16	3	6	–	PC ← addr16	
		$addr16	2	6	–	PC ← PC + 2 + jdisp8	
		AX	2	8	–	PCH ← A, PCL ← X	
Conditional branch	**BC**	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 1	
	BNC	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if CY = 0	
	BZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 1	
	BNZ	$addr16	2	6	–	PC ← PC + 2 + jdisp8 if Z = 0	

Notes 1. When the internal high-speed RAM area is accessed or for an instruction with no data access

2. When an area except the internal high-speed RAM area is accessed

Remarks 1. One instruction clock cycle is one cycle of the CPU clock (fCPU) selected by the processor clock control register (PCC).

2. This clock cycle applies to the internal ROM program.

(2) Manchester code generator

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					250	kbps

(3) Serial interface

(T_A = –40 to +85°C, 1.8 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = AV_{SS} = 0 V)

(a) UART6 (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

(b) UART0 (Dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					625	kbps

LCD Characteristics

(1) Resistance division method

(a) Static display mode (T_A = –40 to +85°C, 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)[Note 3]

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	**Note 3**			V_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ

(b) 1/3 bias method (T_A = –40 to +85°C, 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)[Note 3]

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	**Note 3**			V_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ

(c) 1/2 bias method (T_A = –40 to +85°C, 1.8 V ≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)[Note 3]
1/4 bias method (T_A = –40 to +85°C, 4.5 V ≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)[Note 3]

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
LCD drive voltage	V_{LCD}	**Note 3**			V_{DD}	V
LCD divider resistor[Note 1]	R_{LCD}		60	100	150	kΩ
LCD output resistor[Note 2] (Common)	R_{ODC}				40	kΩ
LCD output resistor[Note 2] (Segment)	R_{ODS}				200	kΩ

Notes 1. Internal resistance division method only.

2. The output resistor is a resistor connected between one of the V_{LC0}, V_{LC1}, V_{LC2} and V_{SS} pins, and either of the SEG and COM pins.

3. Set VAON based on the following conditions.

<When set to the static display mode>
- When 2.0V≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/3 bias method>
- When 2.5V≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method>
- When 2.7V≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8V≤ V_{LCD} ≤ V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/4 bias method>
- When 4.5V≤ V_{LCD} ≤ V_{DD} ≤ 5.5 V: VAON = 0